National Semiconductor

PRELIMINARY

DM75/85X432 128 x 4, DM75/85X433 128 x 5, No-Fall-Through FIFO Memories

General Description

The device is a first-in-first-out (FIFO) sequential memory organized as 128 words by either 4 or 5 bits. Data words written into the device are later read from a separate bus in the same order as entered but at an independent rate. Write and read operations may occur concurrently and at any time with respect to each other. The FIFO is a no-fall-through (NFT) type in which new input data becomes available for output in less time than the minimum write/read cycle period.

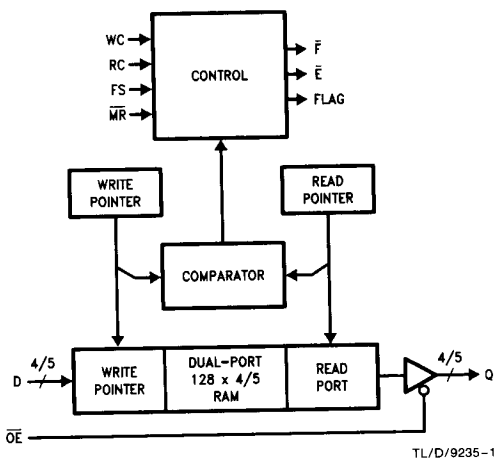
Features

- 128 x 4/5 bit FIFO memory
- No fall-through delay (first word propagates to output in less than one cycle period)
- 35 MHz write and 50 MHz read clock frequencies
- Totally independent asynchronous write and read clocks
- 16 mA TRI-STATE® data outputs for bus drive capability
- Status outputs indicate full, empty and partially-filled conditions
- 18/20 pin 0.3" wide DIP package
- TTL I/O signal levels
- Single +5V supply

Applications

- Data rate translator for computer peripheral controller, eg. disc, tape, printer, graphic display, etc.
- Data rate translator for telecommunications or data communications controller (including local area network)
- ADC or DAC interface buffer for real-time DSP
- Real-time data acquisition buffer
- Variable length shift register for real-time signal delay
- Variable length pipeline register for multiprocessing, DSP, graphics, image analysis, etc.

Block and Connection Diagrams



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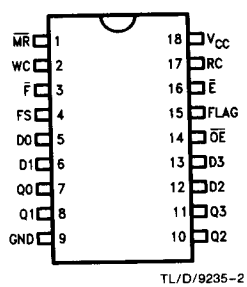
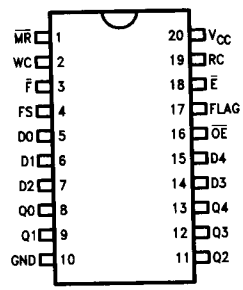
Dual-In-Line Package



TL/D/9235-2

Order Number DM75/85X432J or DM85X432N
See NS Package Number J18A or N18A



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Order Number DM75/85X433J or DM85X433N
See NS Package Number J20A or N20A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, V_{CC}	7V
Input Voltage	7V
Off-State Output Voltage	5.5V
Storage Temperature	−65°C to +150°C
ESD Susceptibility (Note 4)	To Be Determined

Electrical Characteristics Over Operating Conditions DM75/DM85X432/433

Symbol	Parameter	Conditions		Guaranteed Limits		Units
				Min	Max	
V_{IL}	Low-Level Input Voltage				0.8	V
V_{IH}	High-Level Input Voltage			2		V
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
I_{IL}	Low-Level Input Current	V_{CC} = Max, V_I = 0.45V			−0.4	mA
I_{IH}	High-Level Input Current	V_{CC} = Max, V_I = 2.4V			50	μA
I_I	Maximum Input Current	V_{CC} = Max, V_I = 5.5V			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IL} = 0.8V, V_{IH} = 2V	I_{OL} = 16 mA for Q Outputs I_{OL} = 4 mA for $\overline{F}$, $\overline{E}$ and FLAG Outputs		0.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IL} = 0.8V, V_{IH} = 2V	I_{OH} = −2.6 mA for Q Outputs I_{OL} = −0.6 mA for $\overline{F}$, $\overline{E}$ and FLAG Outputs	2.4		V
I_{OS}	Output Short-Circuit Current (Note 1)	V_{CC} = Max, V_O = 0V		−30	−80	mA
I_{OZH}	High Voltage Off-State Output Current	V_{CC} = 5.5V, V_{OH} = 2.7V			20	μA
I_{OZL}	Low Voltage Off-State Output Current	V_{CC} = 5.5V, V_{OL} = 0.4V			−20	μA
I_{CC}	Supply Current	V_{CC} = Max, Inputs Low, Outputs Open			265	mA

Note 1: Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Operating Conditions (Note 3)

Symbol	Parameter	DM75X432/433		DM85X432/433		Units
		Min	Max	Min	Max	
V_{CC}	Supply Voltage	4.5	5.5	4.75	5.25	V
T_A	Operating Free-Air Temperature (Note 2)	−55	+125	0	+70	°C
t_{WWH}	WC Pulse Width High			10		ns
t_{WWL}	WC Pulse Width Low			15		ns
t_{SDW}	Input Data Setup			15		ns
t_{HDW}	Input Data Hold Time			0		ns
t_{WRH}	RC Pulse Width High			10		ns
t_{WRL}	RC Pulse Width Low			10		ns
t_{WM}	Master Reset Pulse Width					ns
t_{RMW}	Reset Recovery Time					ns

Note 2: Ambient Temperature.

Note 3: Since the FIFO is a very high speed device, care must be taken in the design of the hardware. Proper device grounding and supply decoupling are crucial to the correct operation of the FIFO.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor

Switching Characteristics Over Operating Conditions

Symbol	Parameter	Initial Conditions	DM75X432/433		DM85X432/433		Units
			Min	Max	Min	Max	
f_{WC}	Write Frequency					35	MHz
f_{RC}	Read Frequency					35	MHz
t_{PRQ}	RC to Data Output					20	ns
t_{PWF}	WC Rising to $\overline{F}$ Low	127 Words				15	ns
t_{PWE}	WC Rising to $\overline{E}$ High	Empty				15	ns
t_{PRE}	RC Rising to $\overline{E}$ Low	1 Word				15	ns
t_{PRF}	RC Rising to $\overline{F}$ High	Full				15	ns
t_{PWI}	WC Rising to FLAG High					20	ns
t_{PRI}	RC Rising to FLAG Low					20	ns
t_{SRW}	RC Rising Before WC	Full					ns
t_{SWR}	WC Rising Before RC	Empty					ns
t_{PDQ}	Transparent D to Q	Empty, WC = Low				30	ns
t_{PWQ}	WC Falling to Q	Empty				30	ns
t_{PMF}	MR to $\overline{F}$ High	Full				30	ns
t_{PME}	MR to $\overline{E}$ Low					30	ns
t_{PMI}	MR to FLAG Low					30	ns
t_{PZX}	Output Enable					20	ns
t_{PXZ}	Output Disable					20	ns

Pin Description

V_{CC} +5V supply.

D_0–$D_{3/4}$ 4/5-bit data input bus.

Q_0–$Q_{3/4}$ 4/5-bit data output bus (TRI-STATE non-inverted).

WC **Write Clock Input**—latches in a data word from D-bus on a low-to-high transition (except when FIFO is full). Data enters the memory while WC is low.

RC **Read Clock Input**—presents next data word onto Q-bus on a low-to-high transition (except when FIFO is empty).

$\overline{E}$ **Empty Status Output**—goes low when last word is read from FIFO (or when FIFO is reset); goes high when first word is written into an empty FIFO.

$\overline{F}$ **Full Status Output**—goes low when FIFO becomes full following a write; goes high when a read cycle creates a vacancy (or when FIFO is reset).

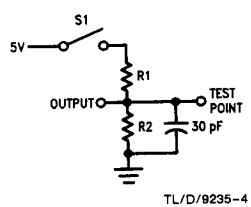
FLAG **Intermediate Status Flag Output**—high while FIFO is at least ¼ filled (32 or more words remaining in memory) if the FS input is low, or while FIFO is at least 3/4 filled (96 or more words) if FS is high; otherwise FLAG remains low.

FS **Flag Select Input**—selects FIFO word-count threshold for FLAG output (32 if low, 96 if high).

$\overline{MR}$ **Master Reset Input**—resets the FIFO to the empty state (internal pointers reset to zero) while low (level sensitive).

$\overline{OE}$ **Output Enable Input**—when low, enables output on the Q data bus; disables when high.

Standard Test Load



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I_{OL}	R1	R2
16 mA	300Ω	600Ω
4 mA	1100Ω	2200Ω

Input Pulse Amplitude = 3V

Input Rise and Fall Time (10%–90%) = 2.5 ns

t_{PHZ} measurement made at V_{OH} − 0.5V, t_{PLZ} measurement made at V_{OL} + 0.5V, all other measurements made at 1.5V.

Functional Description

The NFT FIFO is implemented using a 128 X 4/5-bit RAM with separate write and read ports. The write port is addressed by the write pointer and the read port by the read pointer. While the WC input is low, a data word on the D inputs is written into the write port of the RAM. The write pointer (initially zero) is incremented on the rising edge of WC, thus concluding a write cycle.

The RAM contents addressed by the read pointer (also initially zero) are presented on the Q outputs whenever the $\overline{OE}$ input is low (Q bus outputs are disabled when $\overline{OE}$ is high). Thus the first word may appear on the Q outputs as it is being written. The rising edge of RC increments the read pointer which then accesses the next data word from the RAM's read port. (Each pointer automatically wraps around from the last to the first RAM location.)

When the value of the read pointer becomes equal to the write pointer due to a read cycle, then the FIFO is empty, ie. any data words which had been written have also been read. When the value of the write pointer exceeds the read pointer by 128 due to a write cycle, then the FIFO is full, ie. the next RAM location into which data should be written contains the oldest word that has not yet been read.

The $\overline{E}$ and $\overline{F}$ status outputs indicate the empty and full conditions, respectively. Initially (following a reset) $\overline{F}$ is high. When WC is brought high at the end of any write cycle, $\overline{F}$ would go low if the FIFO becomes full; otherwise it remains high (without glitches). When the FIFO is full, $\overline{F}$ remains low until a vacant RAM location is made available resulting from a read operation (or the Master Reset is activated). $\overline{F}$ goes high after the rising edge of RC which creates the first vacancy.

Writing is inhibited while $\overline{F}$ is low. If WC is brought low while $\overline{F}$ was still low, new data would not begin to be written into the RAM until after a read cycle causes $\overline{F}$ to go high (WC must then remain low long enough to complete the write cycle). Any low-to-high transitions on WC while $\overline{F}$ is low are ignored (write pointer not incremented).

Initially (followinig a reset) the $\overline{E}$ output is low. $\overline{E}$ remains low while the FIFO is empty until the first write cycle is completed. $\overline{E}$ goes high after the rising edge of WC concluding the first write cycle. When RC is brought high at the end of any read cycle, $\overline{E}$ would go low if the FIFO becomes emtpy, otherwise it remains high (without glitches).

Reading is inhibited while $\overline{E}$ is low. Any low-to-high transitions on RC while $\overline{E}$ is low are ignored (read pointer not incremented). While the FIFO is empty, the Q outputs (if enabled) would either be in an indetermined state if WC is high, or would reflect D input data as it is written into the memory if WC is low.

The FIFO is reset to the empty state (write and read pointers reset to zero) while the $\overline{MR}$ input is low. WC and RC inputs are ignored and may be in either state during a reset. If WC is low following a reset, it should remain low long enough to complete the write cycle.

The FS input selects the waveform to appear on the FLAG output. When FS is low, then the FLAG output indicates when the FIFO is at least one quarter filled (i.e., when the write pointer value exceeds the read pointer by at least 32). When FS is high, then FLAG indicates when the FIFO is at least three quarters filled (write pointer exceeds read pointer by at least 96). The FLAG output remains stable (without glitches) except following the write or read cycle which changes the FIFO's status with respect to the selected threshold.

It is recommended that the FS input be changed only while the FIFO is empty or full. If FS is changed while the FIFO contains between 32 and 96 words, the FLAG output may not change to reflect the accurate status until a threshold is crossed.

FLAG Output Truth Table:

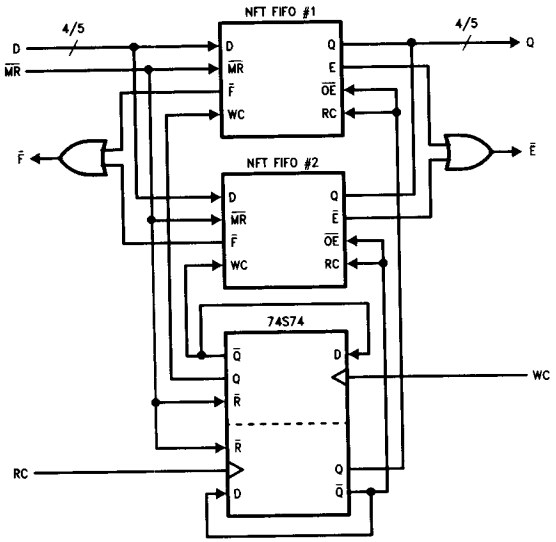
# Words Stored	FLAG Output	
	FS = L	FS = H
0–31	L	L
32–95	H	L
96–128	H	H

FIFO buffers wider than 4 or 5 bits can be implemented by connecting multiple chips in parallel. The $\overline{E}$, $\overline{F}$ and FLAG status information can be taken from any one of the chips since there is no fall-through delay which may otherwise cause output skew between chips.

FIFO buffers deeper than 128 words could also be implemented by connecting the D and Q lines of multiple devices in parallel and alternating the WC and RC clocks between each of the devices in turn (the $\overline{OE}$ input of each device must then be connected to its own RC input). For example, a 256 x 4/5 FIFO buffer could be implemented using two FIFO chips plus a dual D-type flip-flop (eg. 74S74) as shown in the diagram, "External Cascading". Cascading more than two devices (depth greater than 256) requires more sophisticated logic to generate the alternating WC and RC clocks; registered programmable logic devices may be useful for this. Note that when cascading in this manner, there are no additional delays introduced. Also, the threshold boundaries for the FLAG output are proportional to the number of devices cascaded.

Functional Description (Continued)

External Cascading (256 x 4/5 FIFO)



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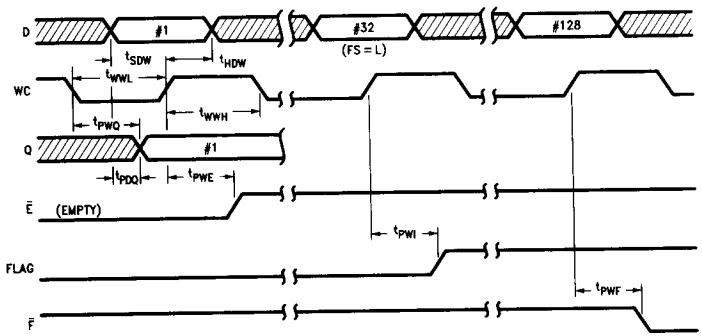
Write Cycle Timing



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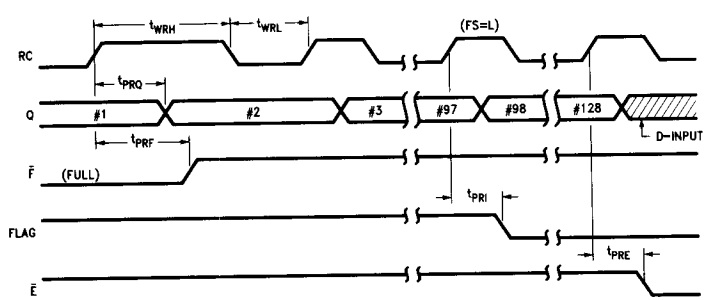
Read Cycle Timing



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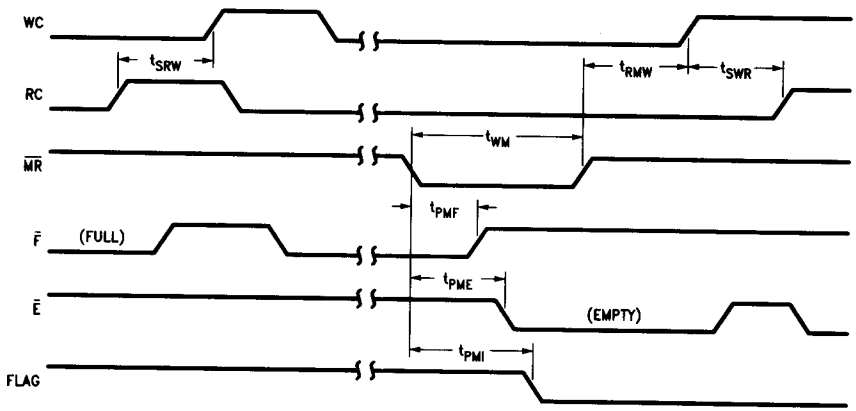
Functional Description (Continued)

Reset and Miscellaneous Timing



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