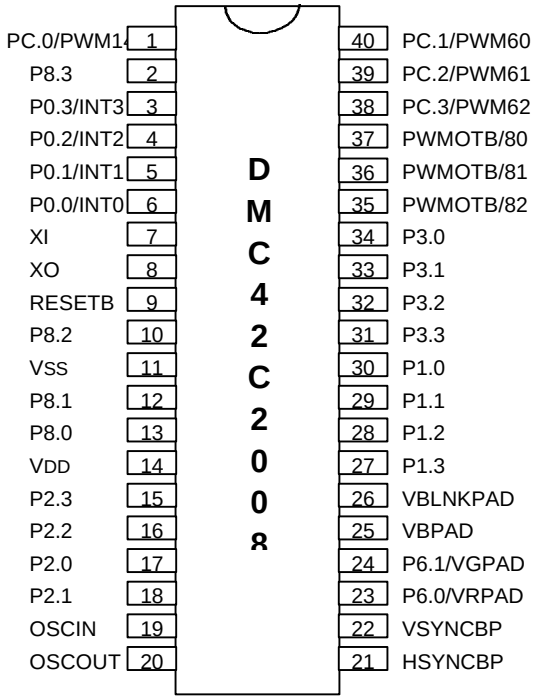
4Bit Single Chip Microcontroller **DMC42C2008**

DESCRIPTION

The DMC42C2008 is a 4-bit single chip micro-computer with 8K bytes ROM, and is manufactured with CMOS silicon gate technology.
The DMC42C2008 includes peripherals such as 8-bit Timer/Event Counters, 4-bit A/D Converter, 14-bit PWM, 8-bit PWM, 6-bit PWM, Watchdog Timer, 4-ch External Interrupts and OSD controller.
It provides the hardware features, architectural enhancements and instructions that are necessary to make it a powerful and cost effective controller for applications requiring up to 64K bytes of program-mable memory.

PIN CONFIGURATION



FEATURE

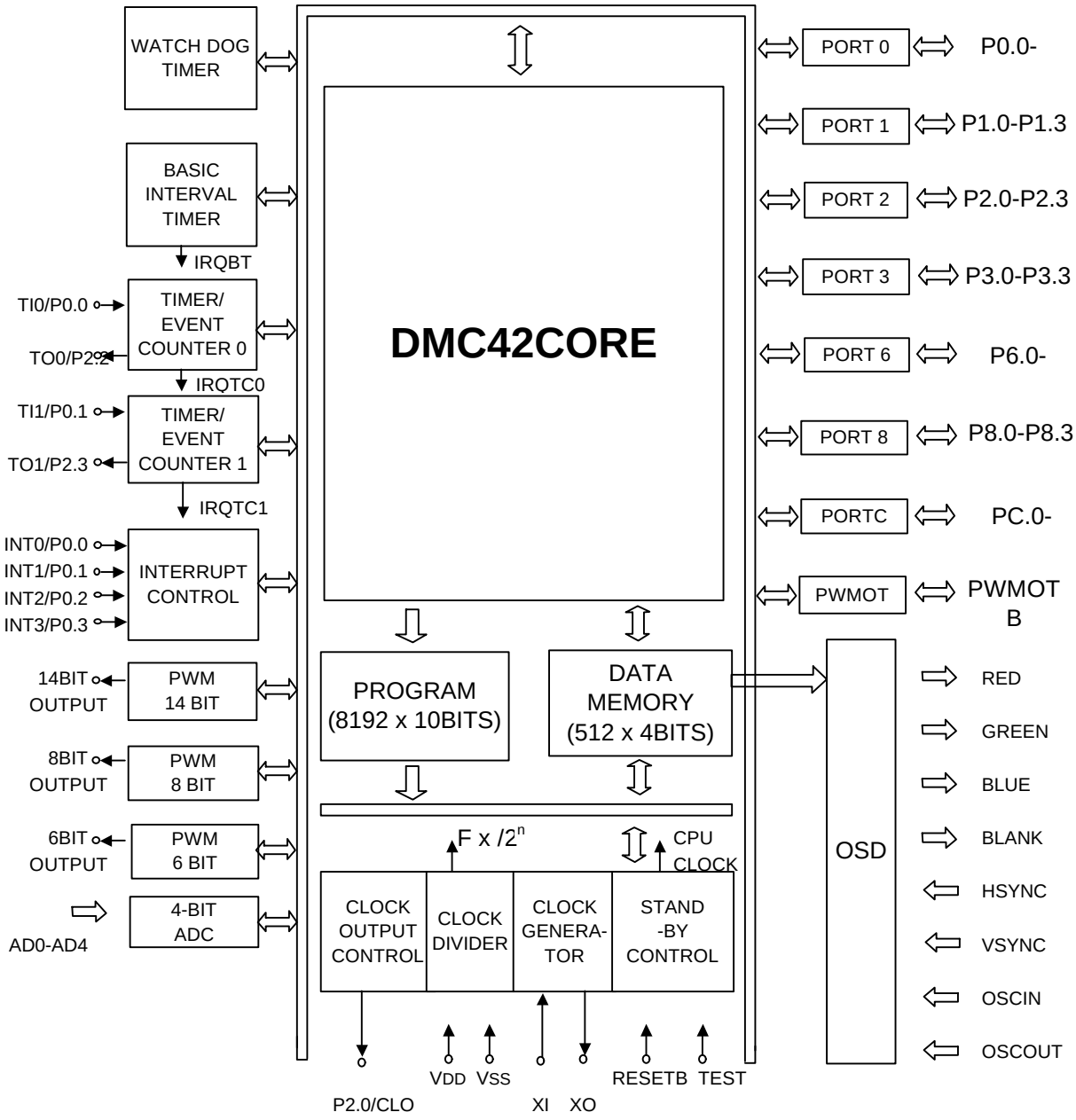
- Memory Mapped I/O
- Program Memory : 8192 x 10 bits
- Data Memory : 512 x 4 bits
- Instructions
  - Various Bit Manipulation
  - 8 bit Data Transfer, Compare, Arithmatic
  - 7 bit Relative Branch
  - 1 byte Absolute Call
- Instruction cycle times
  - Main (XI = 4.19MHz)
    . 15.3 us (XI/64 = 65.5KHz)
    . 1.91 us (XI/8 = 524.0KHz)
    . 0.95 us (XI/4 = 1.05MHz)
- 4 Register Bank
- General Register
  - 8 x 4 bit x 4 Banks
- Accumulator
  - Bit Accumulator (CY), 4 bit Accumulator (A), 8 bit Accumulator (XA)
- Multiple Vectored Interrupt Source
  - External Interrupts : 4
  - Internal Interrupts : 3
  - Vsync Interrupts : 1
- Watch timer
  - fast mode : 3.91 msec
  - normal mode : 0.5 sec
  - buzzer output : 1, 2, 4 KHz
- Basic interval timer
  - 8 kinds of period
  - Used stabilization wait timer to wake up Stop mode
- Two 8-bit timer / event counters

- 4 Bit A/D Converter
  Programmable Comparator Input
  AFC Input Signal Detection Circuit
- PWM
  - 14 Bits PWM Output x 1Ch
  - 8 Bits PWM Output x 3Ch
  - 6 Bits PWM Output x 3Ch
- 29 I/O Pins
  - CMOS I/O Pins : 22
    (Digital CMOS Levels Schmitt Triggered)
  - PWM Pins : 7
- Power saving mode
  - STOP : Main clock, CPU clock stop
  - STBY : Only CPU clock stop
    Main clock operation
- Package : 40 DIP

OSD CONTROLLER SPEC.

- Character ROM ; 12 x 16 x 96 bits
- Video RAM ; 120 x 10 Bits
- OSD Clock ; 4MHz ~ 7MHz
- Character Number ; 96
- Display Capacity ; 20 Columns x 6 Lines
  (120 Character)
- Character Size ; 16 Kinds (4 x 4 Kinds)
  - Horizontal 1T, 2T, 3T, 4T/Dots
  - Vertical 1H, 2H, 3H, 4H/Dots
- Character Color ; 8 Colors
  Black, Blue, Green, Red,
  Magenta, Yellow, White,
  Cyan
- Display Mode ; 3 Modes
  Character, Fringe,
  Background
- Background Color ; 8 Colors
  - Character Background Area Mode
  - All TV Display Area Mode
- OSD Oscillator Control Modes ;
  (Always Oscillate, Oscillates
  Only in the Display Period
  LC Oscillator)
- Display Position ; 1'st line, 2'nd line
  Variable
- Structure of Character
  12 (Width) x 16 (Height) dots
- Vsync Interrupt

BLOCK DIAGRAM



PROGRAM MEMORY (ROM)

	CONTENTS
0000H	VECTOR ADDRESS AREA
001FH	
0020H	ZERO-PAGE CALL AREA
002FH	
0060H	**8K Byte**
1FFFH	

VECTOR ADDRESS

	Prioty	INTERRUPT SUORCE	
0000H	0	RESET	Reset Signal
0002H	1	IRQBT	Basic Interval Timer
0004H	2	IRQ0	External interrupt 0
0006H	3	IRQ1	External interrupt 1
0008H	4	IRQTC0	Timer Event Counter 0
000AH	5	IRQTC1	Timer Event Counter 1
000CH	6	IRQ2	External interrupt 2
000EH			
0010H	8	IRQ3	External interrupt 3
0012H			
0014H	10	IRQAD	8 bit ADC
0016H			
0018H	12	IRQWT	Watch Timer
001AH			
001CH			
001EH	15	-	reserved

DATA MEMORY (RAM)

		DIRECT	INDIRECT			STACK	GENERAL REGISTER	
		m	@HL		@DE @DL			
	$00 PAGE0 (256 Byte) $FF			**MP=0**		**SPS=0**	**RB=0 RB=2**	**RB=1 RB=4**
	$00 PAGE1 (256 Byte) $FF	**MB=0**	**MB=0**	**MP=1**		**SPS=1**		
BANK 0 (1K)	$00 PAGE2 (256 Byte) $FF			**MP=2**		**SPS=2**	**200~27F OSD RAM**	
	$00 PAGE3 (256 Byte) $FF	**I/O MEMORY**		**MP=3**				

; Usable

I/O ADDRESS MAP

ADDRESS	Hardware Module Name				R/W	Addressing Unit			REMARKS	INITIAL
	b3	b2	b1	b0		1 bit	4 bit	8bit		VALUE
318H	Stack pointer low (SPL)				R/W			O	Stack pointer low	E
319H	Stack pointer high (SPH)				R/W			O	stack pointer high	F
31AH	SP3	SP2	SP1	SP0	R/W			O	Stack Page Select Low (SPSL)	0
31BH	-	-	SP5	SP4	R/W			O	Stack Page Select High (SPSh)	0
31CH	AC		IS1	IS0	R/W	O	O	O	Psw low (PSWL)	0
31DH	CY	Z	OV	T					Psw high (PSWH)	0
320H	T/E counter mode register 0				W	320H.3		O	Clock source select. counter	00
321H	(TMOD0)								start (ch0)	
322H	T/E counter register 0				R				readable count value (ch0)	00
323H	(TMCNT0)									
324H	T/E reference register 0				W				count reference register (ch0)	FF
325H	(TMREF0)									
326H	T/E counter mode register 1				W	326H.3			clock source select. counter start	00
327H	(TMOD1)								(ch1)	
328H	T/E counter register 1				R				readable count value (ch1)	00
329H	(TMCNT1)									
32AH	T/E reference register 1				W				count reference register (ch1)	FF
32BH	(TMREF1)									
332H	Basic Timer mode register(BMOD)				R/W	332H.3			clock select, Bit start	0
334H	Basic interval timer count				R				readable count register	00
335H	register(BITCNT)									
336H	Watch timer mode register				R/W	336H.3			clock/buzzer select. bit3	00
337H	(WMOD)								readable	
338H	Watch dog timer mode register				W				clock source sel. timer EN/DIS	00
	(WDTM)									
339H				WDTF	R				WDT flag	0
340H	Pwm mode register0(PWMOD0)				R/W				6.14bit pwm counter EN/DIS	0
342H	Pwm0 data register high				W			O	14bit pwm data register high	00
343H	(PWMODH)									
344H	Pwm0 data register low				W			O	14bit pwm data register low	00
345H	(PWMODL)									
346H	Pwm channel start mode register				W			O	6bit*6ch, 14bit pwm start EN/DIS	00
347H	(PWMSM)									
348H	Pwm60 data register (PWMDR0)				W			O	6bit pwm channel 0 data register	00
349H										
34AH	Pwm61 data register (PWMDR1)				W			O	6bit pwm channel 1 data register	00
34BH										
34CH	Pwm62 data register (PWMDR2)				W			O	6bit pwm channel 2 data register	00
34DH										
354H	PWM3	PWM2	PWM1	PWM0	W			O	pwm output enable mode	00
355H		PWM6	PWM5	PWM4					register (PWM0 = 14bit)	
358H	Pwm mode register 1 (PWMOD1)				W		O		8bit pwm control	
35AH	Pwm80 data register (PWMDR80)				W			O	8bit pwm channel 0 data register	00
35BH										

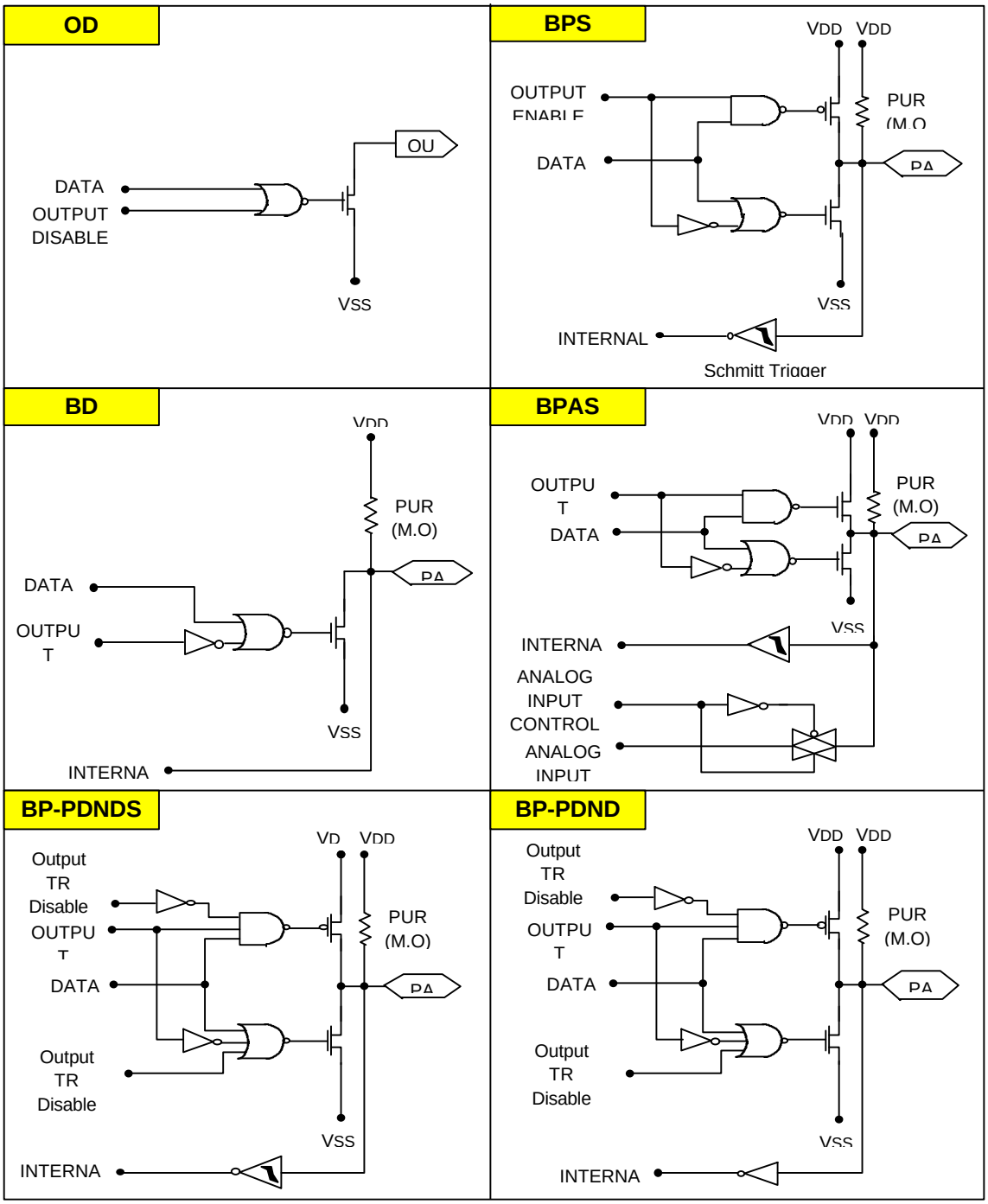
ADDRESS	Hardware Module Name				R/W	Addressing Unit			REMARKS	INITIAL
	b3	b2	b1	b0		1 bit	4 bit	8bit		VALUE
35CH	Pwm81 data register (PWMDR81)				W			O	8bit pwm channel 1 data register	00
35DH										
35EH	Pwm82 data register (PWMDR82)				W			O	8bit pwm channel 2 data register	00
35FH										
360H	1'st line horizontal display mode				W			O	1'st line horizontal position set.	00
361H	register (HDPM1)								000000h-111111h	
362H	1'st line vertical display mode				W			O	1'st line vertical position set.	00
363H	register (VDPM1)								000000h-111111h	
364H	H/V character size mode				W			O	1, 2, 3, 4Tc/dot	00
365H	register (HVSMOD)								1, 2, 3, 4H/dot	
366H	Display mode & background color				W			O	dspon, R/G/B control	00
367H	register (DBCM)									
368H					W		O		osd out enable	0
36AH	I/O polarity control register				W			O	Y(BLK), R/G/B output, H/Vsync	00
36BH	(POLCON)								control	
36CH	2'nd line horizontal display mode				W			O	2'nd line horizoncal position set.	00
36DH	register (HDPM2)								000011h-111111h	
36EH	2'nd line vertical display mode				W			O	2'nd line vertical position set.	00
36FH	register (VDPM2)								000000h-111111h	
380H	Adc4 mode register (ADCM4)				W			O	Reference voltage setting. start	00
381H										
382H	Adc4 output latch (ADCOL4)				R		O		conversion data	0
3A0H	Power control register						O		system clock select, idle, stop	00
	(PCON)				R/W				mode	
3A2H	Operating mode register (SCMOD)				R/W	O			main/sub system clock select	0
3A4H	Clock output mode register				W		O		cpu clock output select, clock	00
	(CLOMD)								out EN/DIS	
3B2H	Power on flag (PONF)				P/W	3B2H.0		O	power on reset flag	0
3C2H	IME				R/W	3C2H.3		O	Interrupt priorty select, IME flag.	00
3C3H	IPSR3	IPSR2	IPSR1	IPSR0						
3C4H	External interrupt mode register0				W		O		external interrupt 0 edge	00
	(IMOD0)								detection	
3C5H	External interrupt mode register1				W		O		external interrupt 1 edge	00
	(IMOD1)								detection	
3C6H	External interrupt mode register2				W		O		external interrupt 2 edge	00
	(IMOD2)								detection	
3C7H	External interrupt mode register3				W		O		external interrupt 3 edge	00
	(IMOD3)								detection	
3D8H	IE2	IRQ2	IEBT	IRQBT	R/W	O	O		Interrupt EN/IRQ flag	0
3D9H			IEWT	IRQWT	R/W	O	O		Interrupt EN/IRQ flag	0
3DAH					R/W	O	O		Interrupt EN/IRQ flag	0
3DBH	IETC1	IRQTC1	IETC0	IRQTC0	R/W	O	O		Interrupt EN/IRQ flag	0
3DCH	IE1	IRQ1	IE0	IRQ0	R/W	O	O		Interrupt EN/IRQ flag	0
3DDH					R/W	O	O		Interrupt EN/IRQ flag	0
3DEH			IE3	IRQ3	R/W	O	O		Interrupt EN/IRQ flag	0

ADDRESS	Hardware Module Name				R/W	Addressing Unit			REMARKS	INITIAL VALUE
	b3	b2	b1	b0		1 bit	4 bit	8bit		
3E0H	PW03	PW02	PW01	PW00	W			O	port 0, 1 mode register (PMGA)	00
3E1H	PW13	PW12	PW11	PW10						
3E2H	PW23	PW22	PW21	PW20	W			O	port 2, 3 mode register (PMGB)	00
3E3H	PW33	PW32	PW31	PW30						
3E6H	PW63	PW62	PW61	PW60	W			O	port 6, 7 mode register (PMGD)	00
3E7H	PW73	PW72	PW71	PW70						
3E8H	PW83	PW82	PW81	PW80	W			O	port 8, 9 mode register (PMGE)	00
3E9H	PW93	PW92	PW91	PW90						
3ECH	PWC3	PWC2	PWC1	PWC0	W			O	port c, d mode register (PMGG)	00
3EDH	PWD3	PWD2	PWD1	PWD0						
3F0H	PORT0 (R0)				R/W	O	O		R0 Port Data Regiter	0
3F1H	PORT1 (R1)				R/W	O	O		R1 Port Data Regiter	0
3F2H	PORT2 (R2)				R/W	O	O		R2 Port Data Regiter	0
3F3H	PORT3 (R3)				R/W	O	O		R3 Port Data Regiter	0
3F6H	PORT6 (R6)				R/W	O	O		R6 Port Data Regiter	0
3F8H	PORT8 (R8)				R/W	O	O		R8 Port Data Regiter	0
3FCH	PORTC (RC)				R/W	O	O		RC Port Data Regiter	0

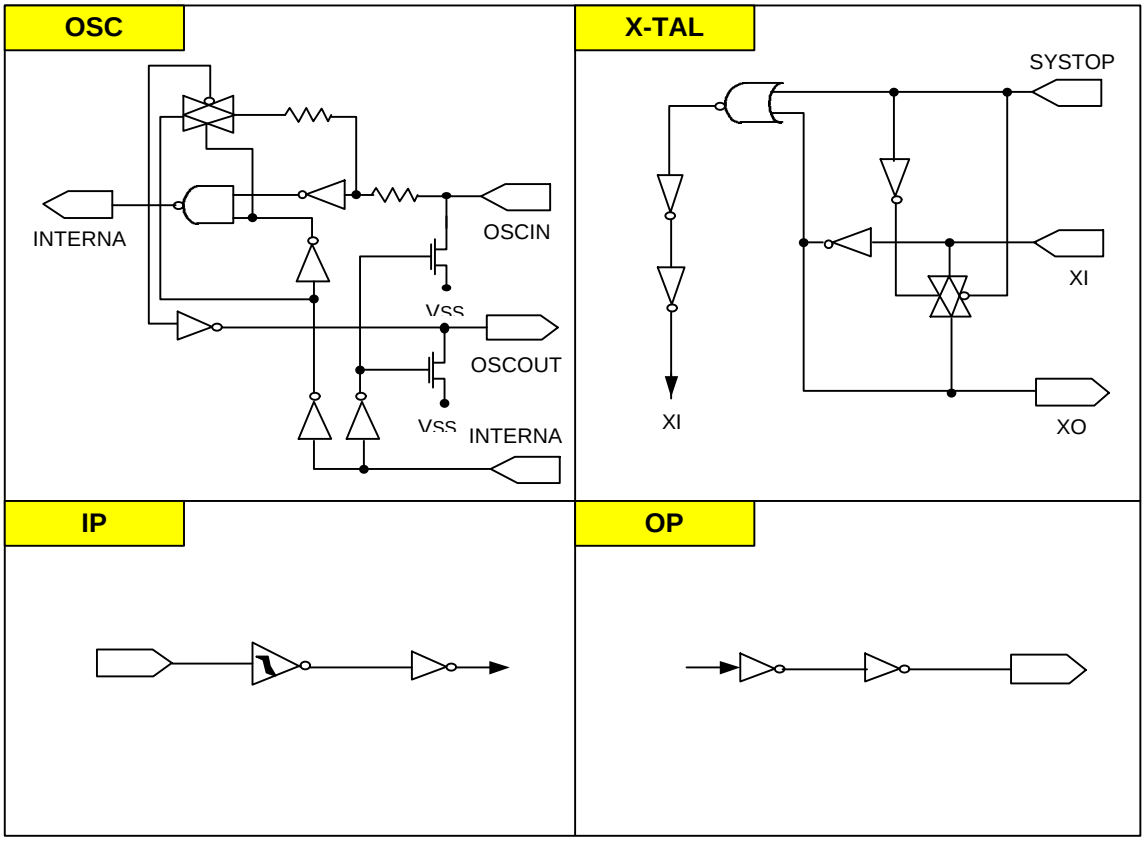
PIN DESCRIPTION

PIN SYMBOL	SHARED PIN	I/O	FUNCTION	RESET	PORT TYPE
P0.0	INT0/TI0 EPA11	I/O	* External Interrupt Input Port by means of The Rising/Falling Edge Detection * Event Pulse Input Port for the Timer/Ever Counter 1bit Data Input Port (EXCEPT ; INT2, INT3) (PORT0)	INPUT PUR(M.O)	BPS
P0.1	INT0/TI1 EPA12				
P0.2	INT2 EPA13				
P0.3	INT3 CEX				
P1.0-P1.3	EPD0---EPD3	I/O	* 4 bit I/O Port (PORT1)	INPUT, PUR(M.O)	BPS
P2.0	CLO	I/O	* Clock Output Port (PORT2)	INPUT, PUR(M.O)	BPS
P2.1	COMPIN	I/O	* Compare Analog Input * 4 bit I/O Port (PORT2)	INPUT PUR(M.O)	BPAS
P2.2	---	I/O	* 4 bit I/O Port (PORT2)	INPUT PUR(M.O)	BPS
P2.3	---				
P3.0-P3.3	EPA4---EPA7	I/O	* 4 bit I/O Port (PORT3)	INPUT, PUR(M.O)	BP-PDND
P6.0	---	I/O	* OSD Red, Green, Output Port (PORT6)	INPUT PUR(M.O)	BP-PDNDS
P6.1	EPD4				
P8.0-P8.2	EPA8--EPA10	I/O	* 4 bit I/O Port	INPUT PUR(M.O)	BPS
P8.3					
PC.0	PWM14 EPA0	O	PWM14 Output Port Push Pull (PORTC)	HIGH LEVEL	OP
PC.1-PC.3	PWM6 EPA1---EPA3	O	PWM6 Output Port Open Drain (PORTC)	HIGH LEVEL	OD
PWMOT80	PWM8	O	Only PWM8 Output Port Open Drain (PWMOTB)	HIGH LEVEL	OD
PWMOT81	PWM8				
PWMOT82	PWM8				
HSYNC	---	I	OSD Horizontal Signal Input Port	INPUT	IP
VSYNC	VPPOEX	I	OSD Vertical Signal Input Port	INPUT	IP
VBPAD	---	O	Video Blue Signal Output Port	HIGH LEVEL	OP
VBLKPAD	---	O	Video Blank Signal Output Port	HIGH LEVEL	OP
XI	---	I	Main Oscillator Input		
XO	---	O	Main Oscillator Output		
OSCIN	---	I	OSD Oscillator Input		
OSCOUT	---	O	OSD Oscillator Output		
RESETB	---	I	Reset Port		

I/O CIRCUITS



NOTE) PUR : Pull-Up Resistor
M.O : Mask Option


OSC
INTERNA
OSCIN
VSS
OSCOUT
VSS
INTERNA
X-TAL
SYSTOP
XI
XI
XO
IP
OP

ABSOLUTE MAXIMUM RATINGS

(T_A = 0¡É to 70¡É, V_{DD} = 5V ±10%, fx = 4.19MHz)

PARAMETER	SYMBOL	CONDITION	RATING	UNIT
Supply Voltage	V_{DD}	-	-0.3 to +7.0	V
Input Voltage	V_I	All I/O ports	-0.3 to V_{DD}+0.3	V
Output Voltage	V_O	All I/O ports	-0.3 to V_{DD}+0.3	V
Output Current High	I_{OH}	One I/O port active	-10	mA
		All I/O ports active	-100	
Output Current Low	I_{OL}	One I/O port active	20	mA
		All I/O ports active	200	
Operating Temperature	T_A	Industrial	-40 to +85	¡É
		Commercial	0 to +70	
Storage Temperature	T_{stg}	-	-55 to +125	¡É

* Exceeding beyond those listed values under "Absolute Maximum Ratings" may cause permanent damage to the device.

DC ELECTRICAL CHARACTERISTICS

(V_{SS} = 0, V_{DD} = 5V ±10%, T_A = 25¡É, f_X = 4.19MHz)

PARAMETER	SYMBOL	TEST CONDITION			LIMIT MIN.	LIMIT TYP.	LIMIT MAX.	UNIT
High Level Input Voltage	V_{IH1}	Port 0, 1, 2, 6, 8, HSYNC, VSYNC, RESETB (Schmitt Input)			0.8	-	V_{DD}	V
	V_{IH2}	XI, OSCIN			V_{DD} -	-	V_{DD}	
	V_{IH3}	Port 3			0.7	-	V_{DD}	
Low Level Input Voltage	V_{IL1}	Port 0, 1, 2, 6, 8, HSYNC, VSYNC, RESETB (Schmitt Input)			0	-	0.2	V
	V_{IL2}	XI, OSCIN			0	-	0.4	
	V_{IL3}	Port 3			0	-	0.3	
High Level Output Voltage	V_{OH}	Port 0, 1, 2, 3, 6, 8, PC0, VBPAD, VBLKPAD (I_{OH} = - 0.75mA)			V_{DD} - 0.4	-	-	V
Low Level Output Voltage	V_{OL}	Port 0, 1, 2, 3, 6, 8, PC0, VBPAD, VBLKPAD (I_{OL} = 1mA)			-	-	0.4	V
		Open Drain	PC1, PC2, PC3, PWMOT8 (0 ~ 2) (I_{OL} = 0.75mA)		-	-	0.4	
			PC1, PC2, PC3, PWMOT8 (0 ~ 2) (I_{OL} = 10mA)		-	-	2	
High Level Input Leakage Current	I_{IH}	All Pin Except XI, OSCIN			-	1.2	3	uA
		XI, OSCIN			-	5	15	
Low Level Input Leakage Current	I_{IL}	All Pin Except XI, OSCIN			-	-1.2	-3	
		XI, OSCIN			-	-5	-15	
Supply Current	I_{DD1}	Main Clock (XI) = 4.19MHz	Dynamic Mode	V_{DD} = 5V ±10%	-	-	10	mA
			Idle Mode		-	-	5	

DC ELECTRICAL CHARACTERISTICS

(V_{SS} = 0, V_{DD} = 5V ±10%, T_A = 25¡É, f_X = 4.19MHz)

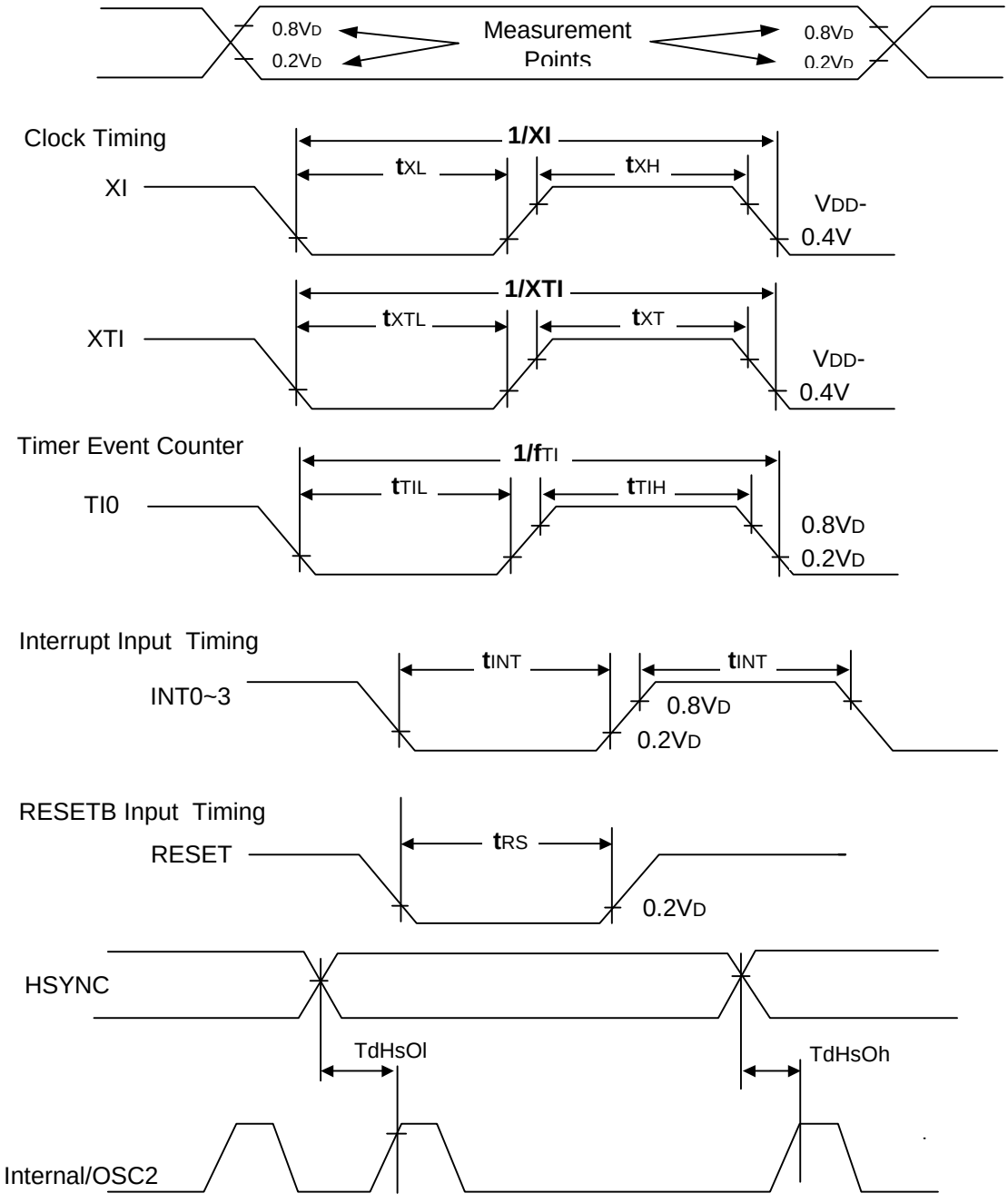
PARAMETER	SYMBOL	TEST CONDITION			LIMIT			UNIT
					MIN.	TYP.	MAX.	
Supply Current	I_{DD2}	Main Clock (XI) = 2MHz	Dynamic Mode	V_{DD} = 3V ±10%	-	-	2	mA
			Idle Mode		-	-	1	
	I_{DD3}	Main Clock (XI) = 4.19MHz	Stop Mode	V_{DD} = 5V ±10%	-	-	5	uA
					-	-	3	
Internal Pull-up Resistor (M.O)	R_{PU}	All Ports VI or VO = 0V, VDD = 5V			-	-	40	Kohm
Pull-up Resistor	R_{L1}	V_I = 0V, V_{DD} = 5V ±10% RESETB			20	-	60	

AC ELECTRICAL CHARACTERISTICS

(T_A = -40 to +85¡É, V_{DD} = 2.7 to 6.0V)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Cycle Time	t_{CY}	V_{DD} = 4.5 to 6.0V	0.95	-	64	uS
		V_{DD} = 2.7 to 3.3V	3.8	-	64	uS
TI Input Frequency	f_{TI}	V_{DD} = 4.5 to 6.0V	0	-	1	MHz
		V_{DD} = 2.7 to 3.3V	0	-	275	KHz
TI Input High, Low Level Width	t_{TIH}	V_{DD} = 4.5 to 6.0V	0.48	-	-	uS
	t_{TIL}	V_{DD} = 2.7 to 3.3V	1.8	-	-	uS
INT 0 ~ 4 Input Level High, Low	t_{INTH}		5	-	-	uS
	t_{INTL}		5	-	-	uS
RESETB Low Level	t_{RSL}		5	-	-	uS
Hsync Start to Vosc Stop	TdHsOl		1TpC	2TpV		
Hsync End to Vosc Start	TdHsOh			1TpV		

AC Timing Measurement Points (Except XI and XTI)



On-Screen-Display

RAM DATA RETENTION CHARACTERISTICS (in STOP Mode)

(TA = -40 to +85¡É)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Data Retention Supply Voltage	VDDDR		2.0	-	6.0	V
Data Retention Supply Current	IDDDR	VDDDR = 2.0V	-	0.1	10	uA
Release Signal Set Time	tSREL		0	-	-	uS
Oscillation Stabilization Wait Time	tWAIT	When released by RESETB	-	2^{17}/fx	-	mS
		When released by interrupt Signal	-	NOTE 1)	-	mS

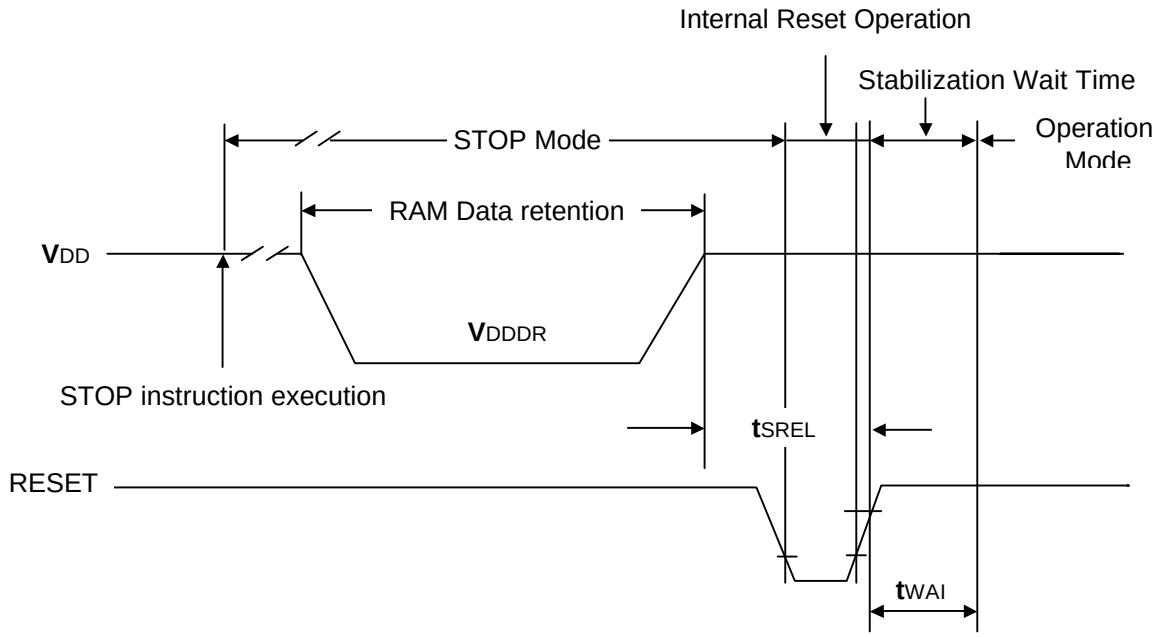
NOTE 1) Depends on the setting of the basic interval timer mode register.
(refer to the table below)

(fx = 4.19MHz)

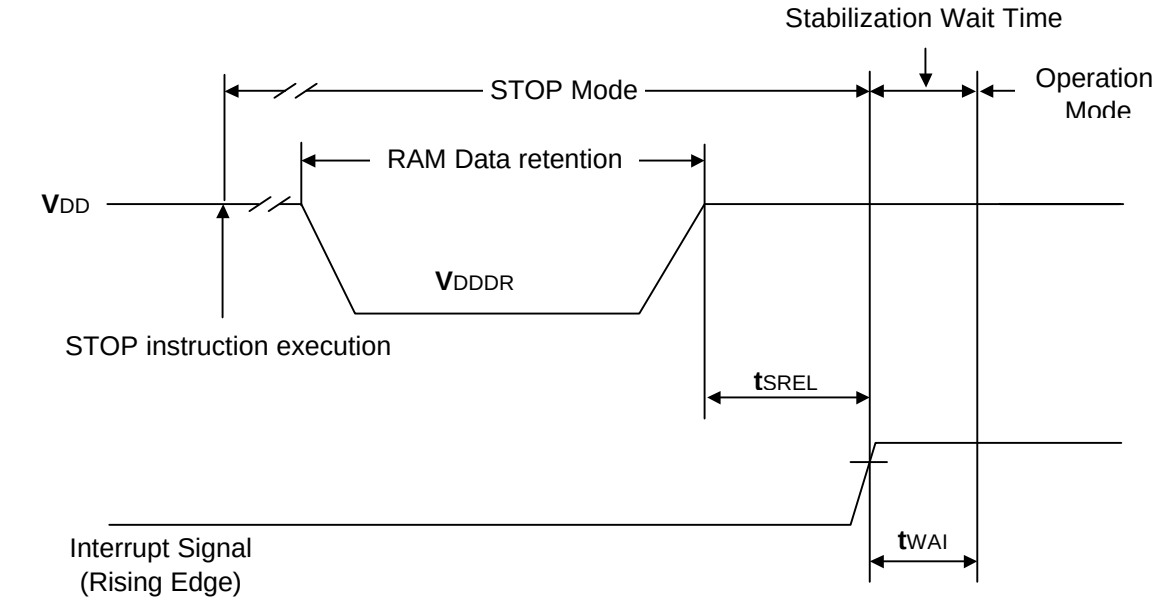
BMOD2	BMOD1	BMOD0	Oscillation Stabilization
0	0	0	2^{20}/fx (Approximately 250ms)
0	1	1	2^{17}/fx (Approximately 31.3ms)
1	0	0	2^{15}/fx (Approximately 7.82ms)
1	0	1	2^{13}/fx (Approximately 1.95ms)

RAM DATA RETENTION TIMING

When STOP mode is released by RESETB input



When STOP mode is released by interrupt signal

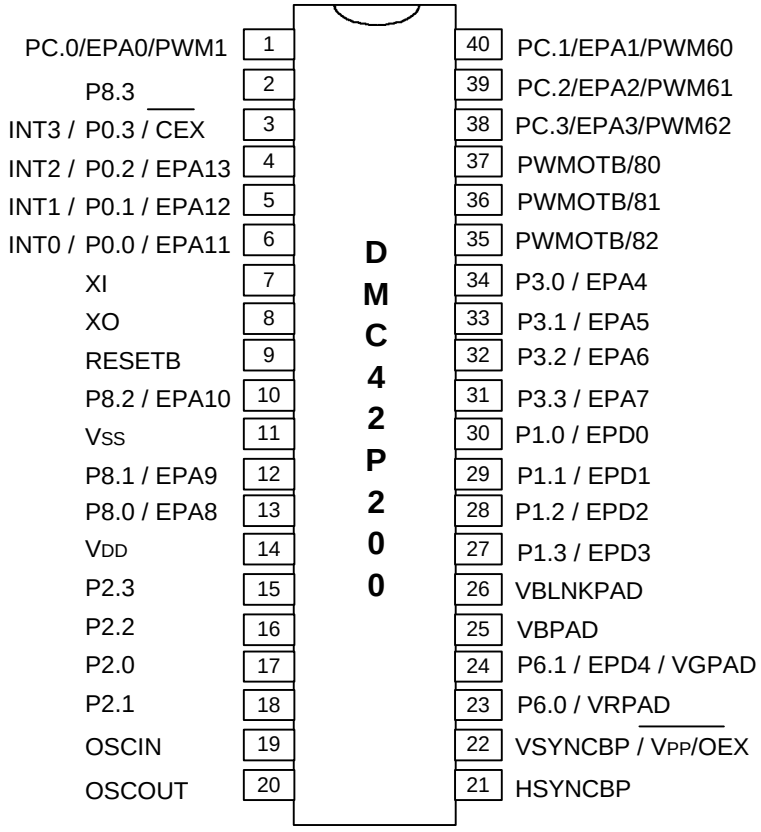


DMC42P2008

DESCRIPTION

The DMC42P2008 is a system evaluation LSI having a build in One-Time-Programming circuit.
A programming and verification for the internal EPROM is achieved by using a adaptor socket.
The function of this device is exactly same as the DMC42C2008 with programming of internal EPROM.
The DMC42P2008 is the OTP version of the DMC42C2008 with replacement of MASK to EPROM as as an internal ROM.

PIN CONFIGURATIONS



DEVICE OPERATION

The operational modes of the DMC42P2008 are listed in Table 1.
A single 5V power supply is required in the read mode.
All inputs are TTL levels except for V_{PP} / $\overline{OEX}$.

V_{PP} = 12.5±0.5V

PINS / MODE	$\overline{CEX}$	V_{PP} / $\overline{OEX}$	V_{DD}	OUTPU
READ	V_{IL}	V_{IL}	5.0V	D_{OUT}
PROGRAM	V_{IL}	V_{PP}	6.0V	D_{IN}
VERIFY	V_{IL}	V_{IL}	6.0V	D_{OUT}
PROGRAM INHIBIT	V_{IH}	V_{PP}	6.0V	High Z

TABLE 1. Operating Modes

PIN NAME	MODE	
	EPROM MODE	USER MODE
TEST	V_{IL}	V_{IH}
RESETB	V_{IL}	V_{IH} / V_{II}

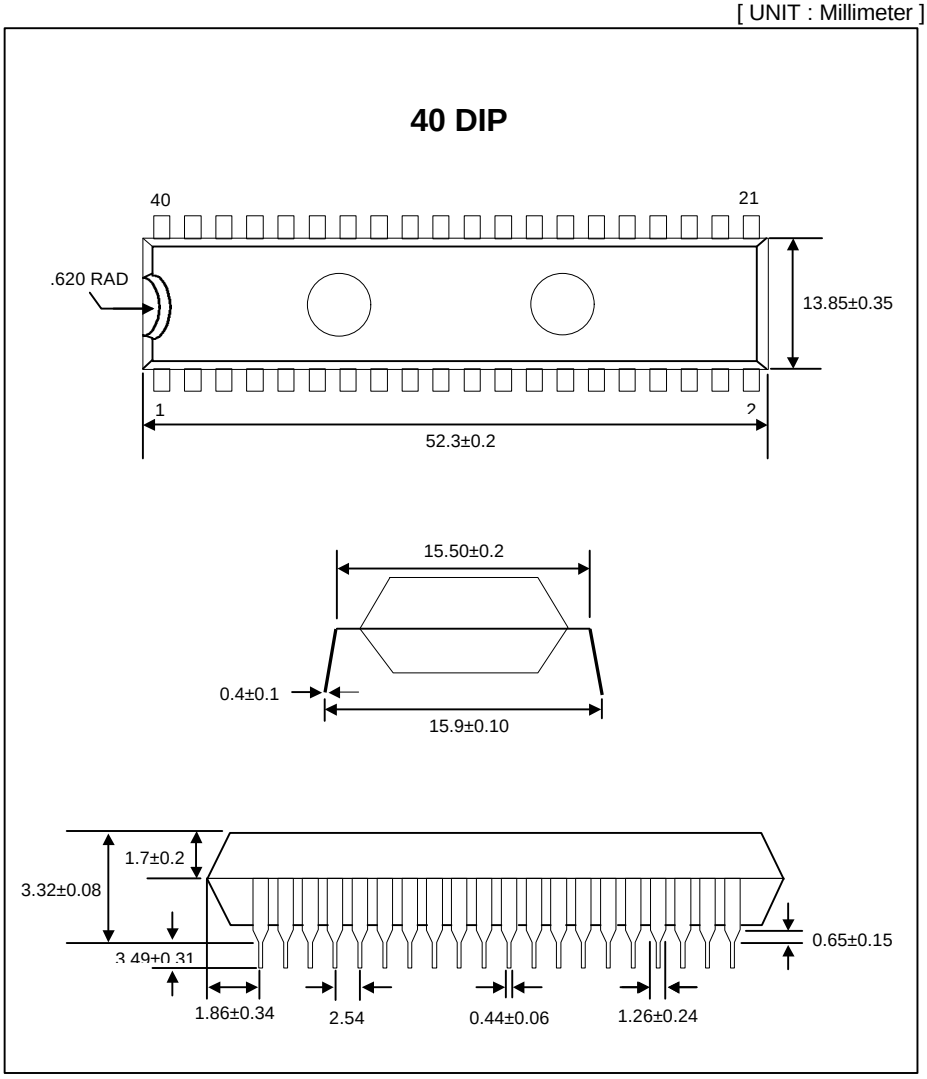
TABLE 2. The modes of DMC42P2008

DC PROGRAMMING CHARACTERISTICS

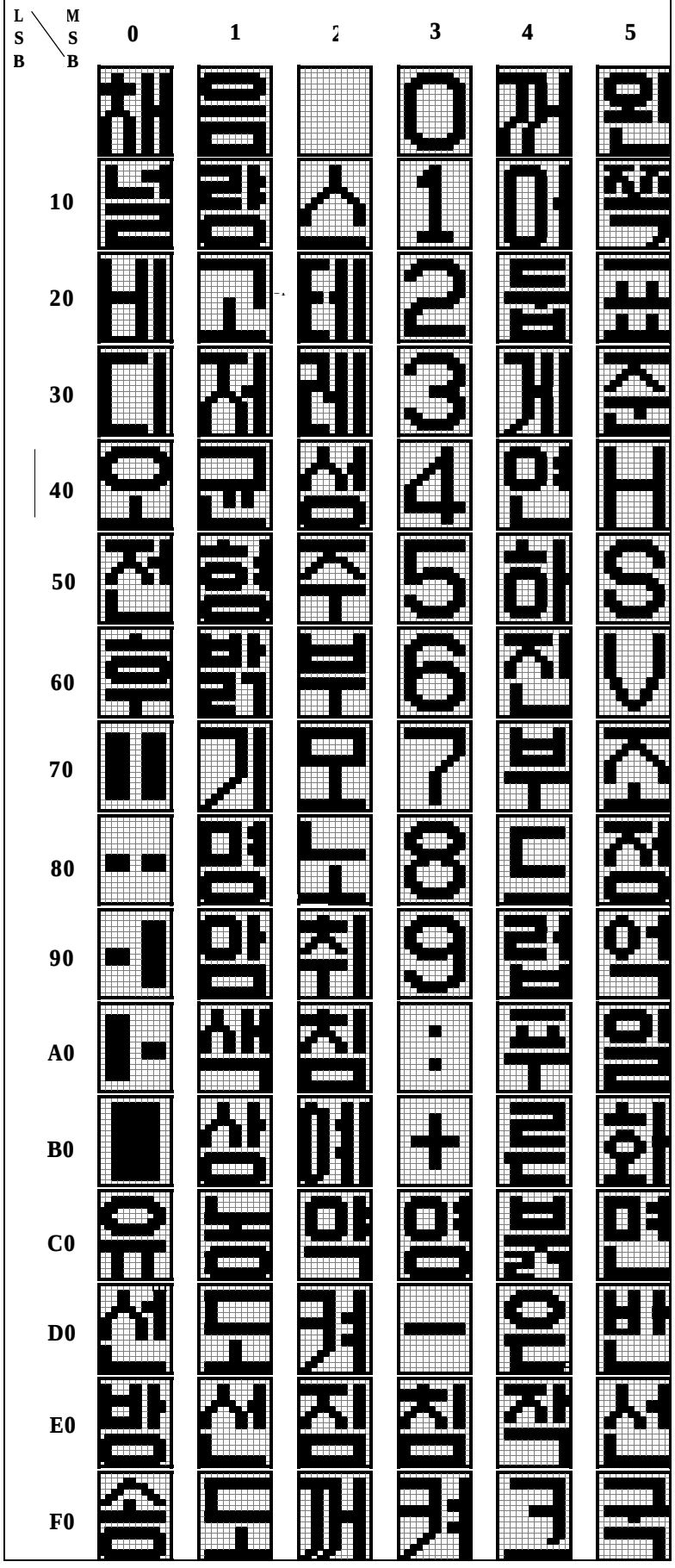
PARAMETER	SYMBO	TEST CONDITION	LIMIT		UNIT
			MIN.	MAX.	
Input Low Voltage	V_{IL}		-0.1	0.8	V
Input High Voltage	V_{IH}		2.0	V_{DD}	V
Output Low Voltage during Verify	V_{OL}	I_{OL} = 2.1mA	-	0.45	V
Output High Voltage during Verify	V_{OH}	I_{OH} = -400uA	2.4	-	V
Quick-pulse Programming	V_{PP}		12.5	13.0	V
Quick-pulse Programming	V_{DD}		6.0	6.5	V

PACKAGE DIMENSION

[UNIT : Millimeter]



STANDARD FORMAT (I)



STANDARD FORMAT(II)