HN58C1001 Series

1M EEPROM (128-kword × 8-bit)
Ready/$\overline{\text{Busy}}$ and $\overline{\text{RES}}$ function

REJ03C0145-0800Z
(Previous ADE-203-028G (Z) Rev.7.0)
Rev. 8.00
Nov. 27. 2003

Description

Renesas Technology's HN58C1001 is an electrically erasable and programmable ROM organized as 131072-word × 8-bit. It has realized high speed, low power consumption and high reliability by employing advanced MNOS memory technology and CMOS process and circuitry technology. It also has a 128-byte page programming function to make the write operations faster.

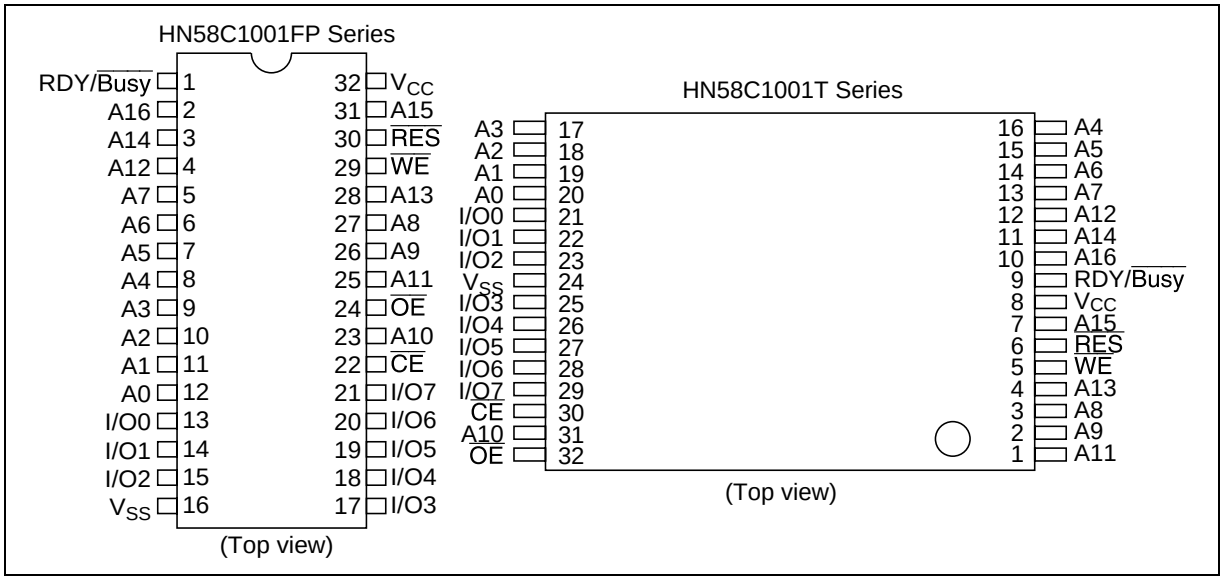
Features

- Single supply: 5.0 V ± 10%
- Access time: 150 ns (max)
- Power dissipation
  - Active: 20 mW/MHz, (typ)
  - Standby: 110 µW (max)
- On-chip latches: address, data, $\overline{\text{CE}}$, $\overline{\text{OE}}$, $\overline{\text{WE}}$
- Automatic byte write: 10 ms (max)
- Automatic page write (128 bytes): 10 ms (max)
- $\overline{\text{Data}}$ polling and RDY/$\overline{\text{Busy}}$
- Data protection circuit on power on/off
- Conforms to JEDEC byte-wide standard
- Reliable CMOS with MNOS cell technology
- 10^4 erase/write cycles (in page mode)
- 10 years data retention
- Software data protection
- Write protection by $\overline{\text{RES}}$ pin
- There are also lead free products.

Ordering Information

Type No.	Access time	Package
HN58C1001FP-15	150 ns	525 mil 32-pin plastic SOP (FP-32D)
HN58C1001T-15	150 ns	32-pin plastic TSOP (TFP-32DA)
HN58C1001FP-15E	150 ns	525 mil 32-pin plastic SOP (FP-32DV) Lead free
HN58C1001T-15E	150 ns	32-pin plastic TSOP (TFP-32DAV) Lead free

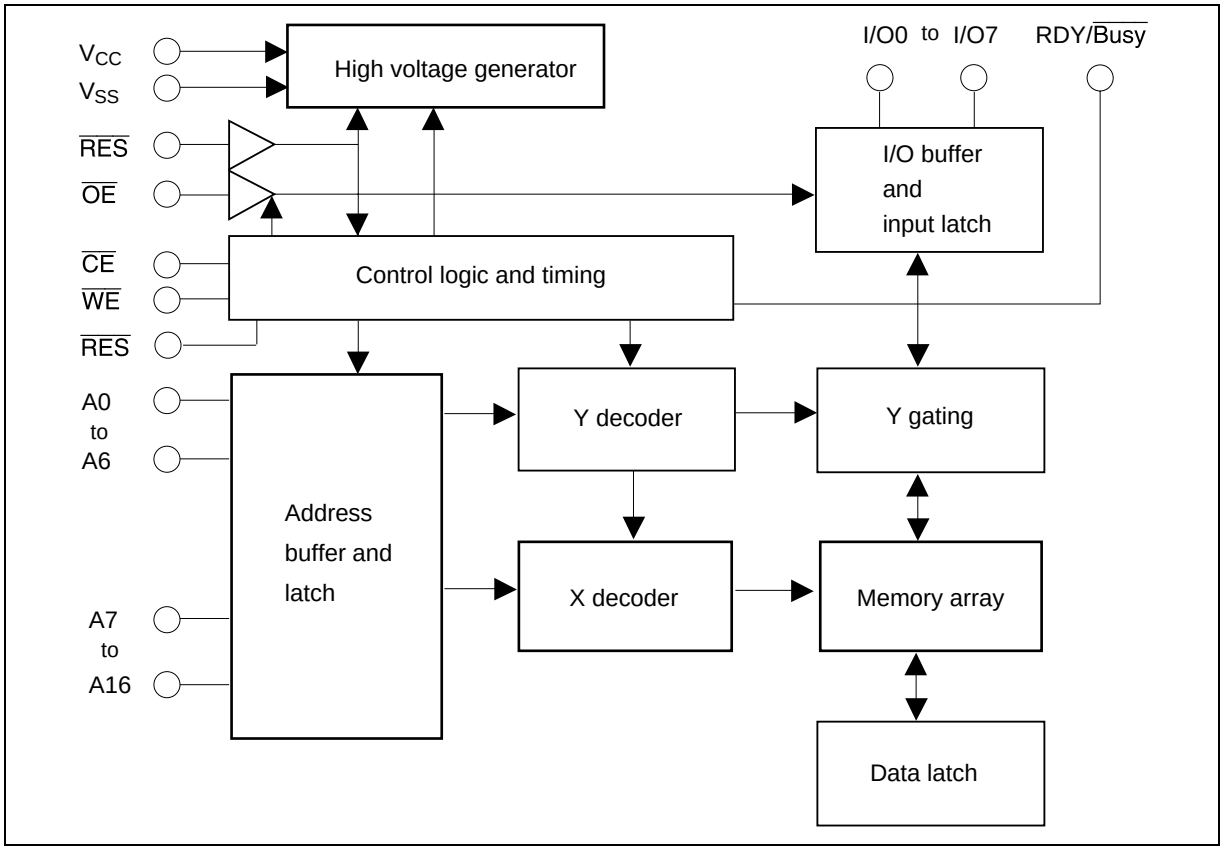
Pin Arrangement



Pin Description

Pin name	Function
A0 to A16	Address input
I/O0 to I/O7	Data input/output
$\overline{OE}$	Output enable
$\overline{CE}$	Chip enable
$\overline{WE}$	Write enable
V_{CC}	Power supply
V_{SS}	Ground
RDY/$\overline{Busy}$	Ready busy
$\overline{RES}$	Reset

Block Diagram



Operation Table

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RES}$	RDY/$\overline{Busy}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	V_H*[1]	High-Z	Dout
Standby	V_{IH}	×*[2]	×	×	High-Z	High-Z
Write	V_{IL}	V_{IH}	V_{IL}	V_H	High-Z to V_{OL}	Din
Deselect	V_{IL}	V_{IH}	V_{IH}	V_H	High-Z	High-Z
Write Inhibit	×	×	V_{IH}	×	—	—
	×	V_{IL}	×	×	—	—
$\overline{Data}$ Polling	V_{IL}	V_{IL}	V_{IH}	V_H	V_{OL}	Dout (I/O7)
Program reset	×	×	×	V_{IL}	High-Z	High-Z

Notes: 1. Refer to the recommended DC operating conditions.
2. × : Don't care

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage relative to V_{SS}	V_{CC}	–0.6 to +7.0	V
Input voltage relative to V_{SS}	Vin	–0.5*[1] to +7.0	V
Operating temperature range*[2]	Topr	0 to +70	°C
Storage temperature range	Tstg	–55 to +125	°C

Notes: 1. Vin min = –3.0 V for pulse width ≤ 50 ns
2. Including electrical characteristics and data retention

Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input voltage	V_{IL}	–0.3*[1]	—	0.8	V
	V_{IH}	2.2	—	V_{CC} + 0.3	V
	V_H	V_{CC} – 0.5	—	V_{CC} + 1.0	V
Operating temperature	Topr	0	—	+70	°C

Note: 1. V_{IL} (min): –1.0 V for pulse width ≤ 50 ns

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5.0V ± 10%)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	I_{LI}	—	—	2*[1]	µA	V_{CC} = 5.5 V, Vin =5.5 V
Output leakage current	I_{LO}	—	—	2	µA	V_{CC} = 5.5 V, Vout = 5.5/0.4 V
Standby V_{CC} current	I_{CC1}	—	—	20	µA	$\overline{CE}$ = V_{CC}
	I_{CC2}	—	—	1	mA	$\overline{CE}$ = V_{IH}
Operating V_{CC} current	I_{CC3}	—	—	15	mA	Iout = 0 mA, Duty = 100%, Cycle = 1 µs, V_{CC} = 5.5 V
		—	—	50	mA	Iout = 0 mA, Duty = 100%, Cycle = 150 ns, V_{CC} = 5.5 V
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –400 µA

Notes: 1. I_{LI} on $\overline{RES}$: 100 µA (max)

Capacitance (Ta = +25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance*[1]	Cin	—	—	6	pF	Vin = 0 V
Output capacitance*[1]	Cout	—	—	12	pF	Vout = 0 V

Note: 1. This parameter is periodically sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5.0 V ± 10%)

Test Conditions

- Input pulse levels: 0.4 V to 2.4 V
  0 V to V_{CC} ($\overline{RES}$ pin)
- Input rise and fall time: ≤ 20 ns
- Output load: 1TTL Gate +100 pF
- Reference levels for measuring timing: 0.8 V, 2.0 V

Read Cycle

		HN58C1001-15			
Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Test conditions**
Address to output delay	t_{ACC}	—	150	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{CE}$ to output delay	t_{CE}	—	150	ns	$\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{OE}$ to output delay	t_{OE}	10	75	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Address to output hold	t_{OH}	0	—	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{OE}$ ($\overline{CE}$) high to output float*[1]	t_{DF}	0	50	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{RES}$ low to output float*[1]	t_{DFR}	0	350	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{RES}$ to output delay	t_{RR}	0	450	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}

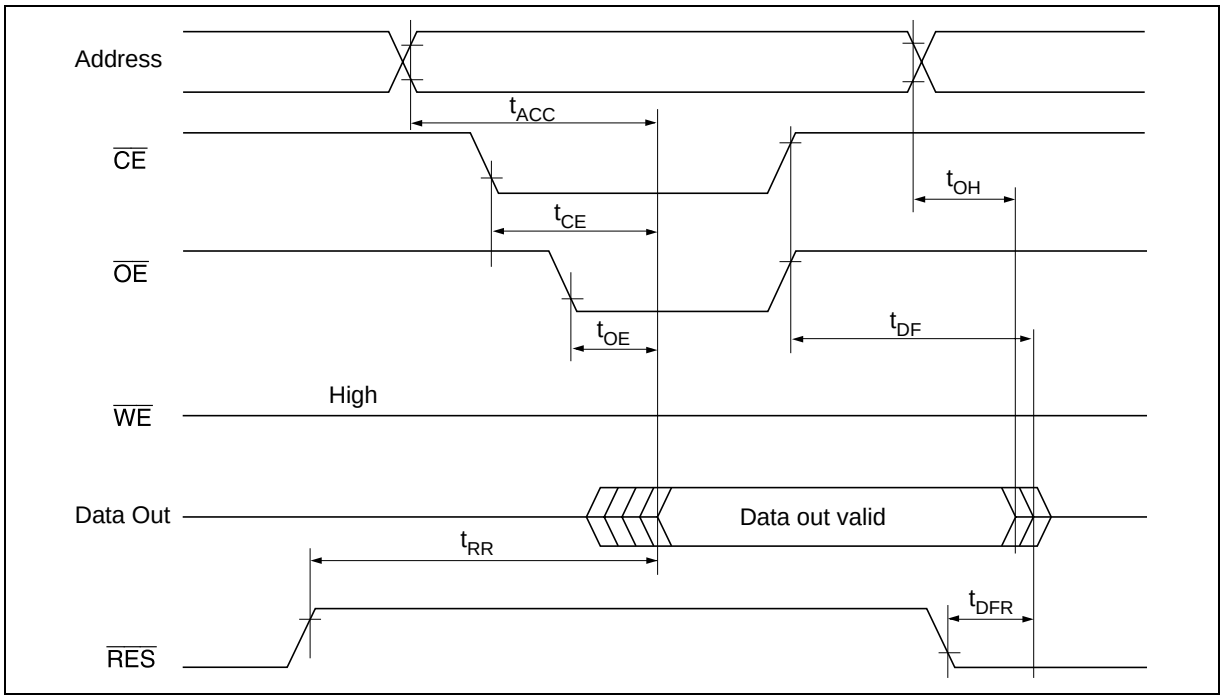
Write Cycle

Parameter	Symbol	Min*[2]	Typ	Max	Unit	Test conditions
Address setup time	t_{AS}	0	—	—	ns	
Address hold time	t_{AH}	150	—	—	ns	
$\overline{CE}$ to write setup time ($\overline{WE}$ controlled)	t_{CS}	0	—	—	ns	
$\overline{CE}$ hold time ($\overline{WE}$ controlled)	t_{CH}	0	—	—	ns	
$\overline{WE}$ to write setup time ($\overline{CE}$ controlled)	t_{WS}	0	—	—	ns	
$\overline{WE}$ hold time ($\overline{CE}$ controlled)	t_{WH}	0	—	—	ns	
$\overline{OE}$ to write setup time	t_{OES}	0	—	—	ns	
$\overline{OE}$ hold time	t_{OEH}	0	—	—	ns	
Data setup time	t_{DS}	100	—	—	ns	
Data hold time	t_{DH}	10	—	—	ns	
$\overline{WE}$ pulse width ($\overline{WE}$ controlled)	t_{WP}	250	—	—	ns	
$\overline{CE}$ pulse width ($\overline{CE}$ controlled)	t_{CW}	250	—	—	ns	
Data latch time	t_{DL}	300	—	—	ns	
Byte load cycle	t_{BLC}	0.55	—	30	µs	
Byte load window	t_{BL}	100	—	—	µs	
Write cycle time	t_{WC}	—	—	10*[3]	ms	
Time to device busy	t_{DB}	120	—	—	ns	
Write start time	t_{DW}	150*[4]	—	—	ns	
Reset protect time	t_{RP}	100	—	—	µs	
Reset high time*[5]	t_{RES}	1	—	—	µs	

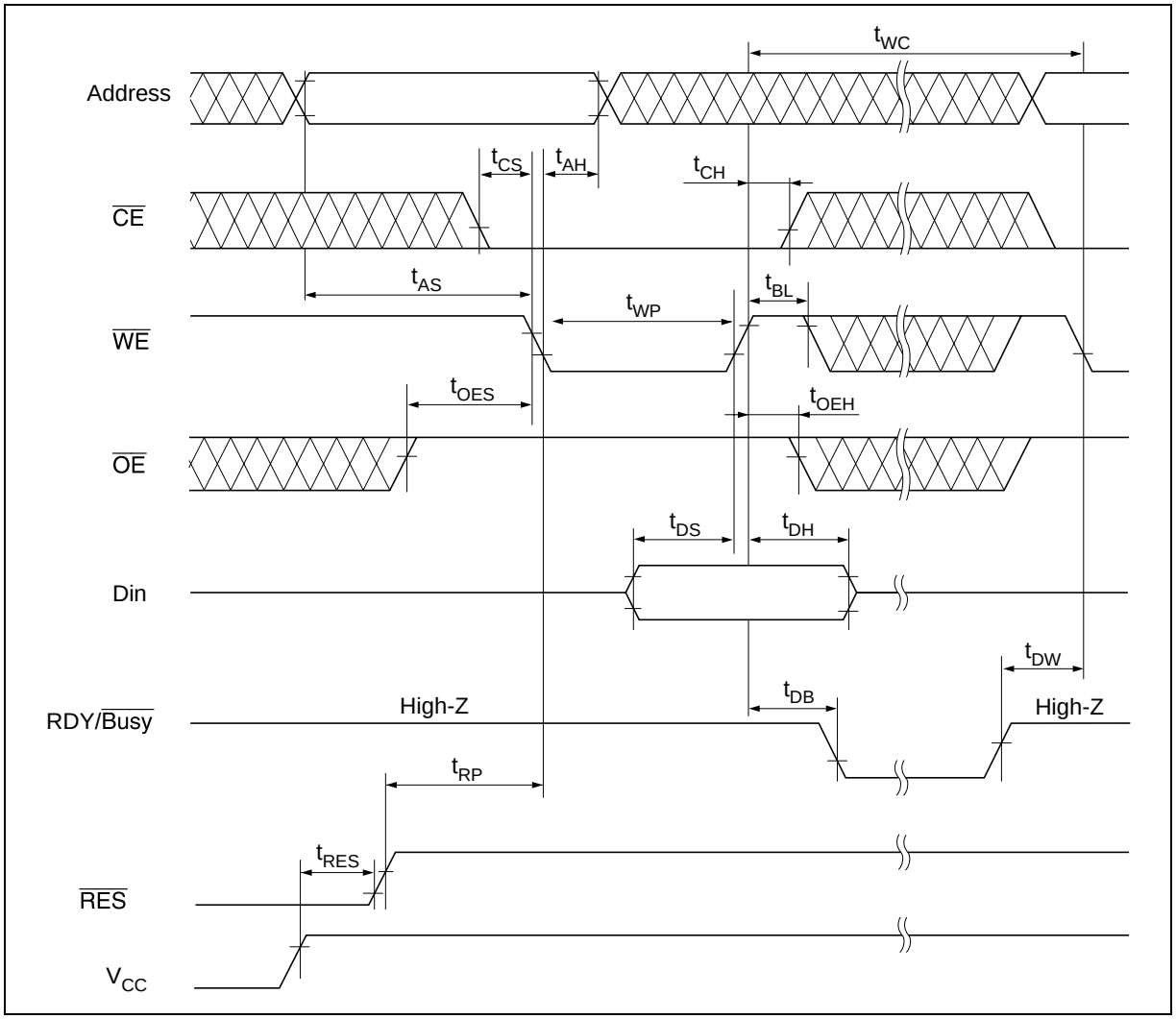
Notes: 1. t_{DF} and t_{DFR} are defined as the time at which the outputs achieve the open circuit conditions and are no longer driven.
2. Use this device in longer cycle than this value.
3. t_{WC} must be longer than this value unless polling techniques or RDY/$\overline{Busy}$ are used. This device automatically completes the internal write operation within this value.
4. Next read or write operation can be initiated after t_{DW} if polling techniques or RDY/$\overline{Busy}$ are used.
5. This parameter is sampled and not 100% tested.
6. A7 to A16 are page addresses and must be same within the page write operation.
7. See AC read characteristics.

Timing Waveforms

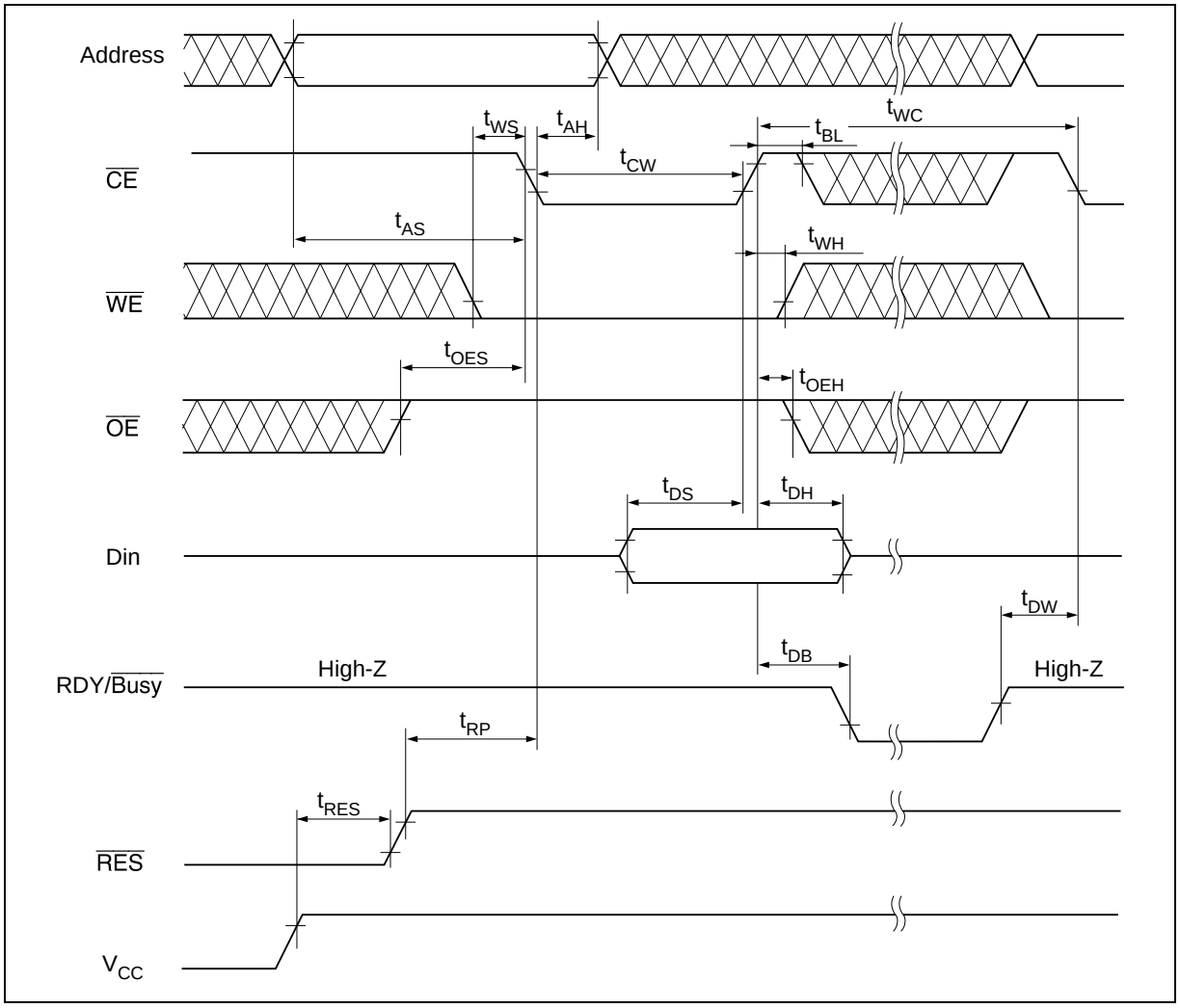
Read Timing Waveform



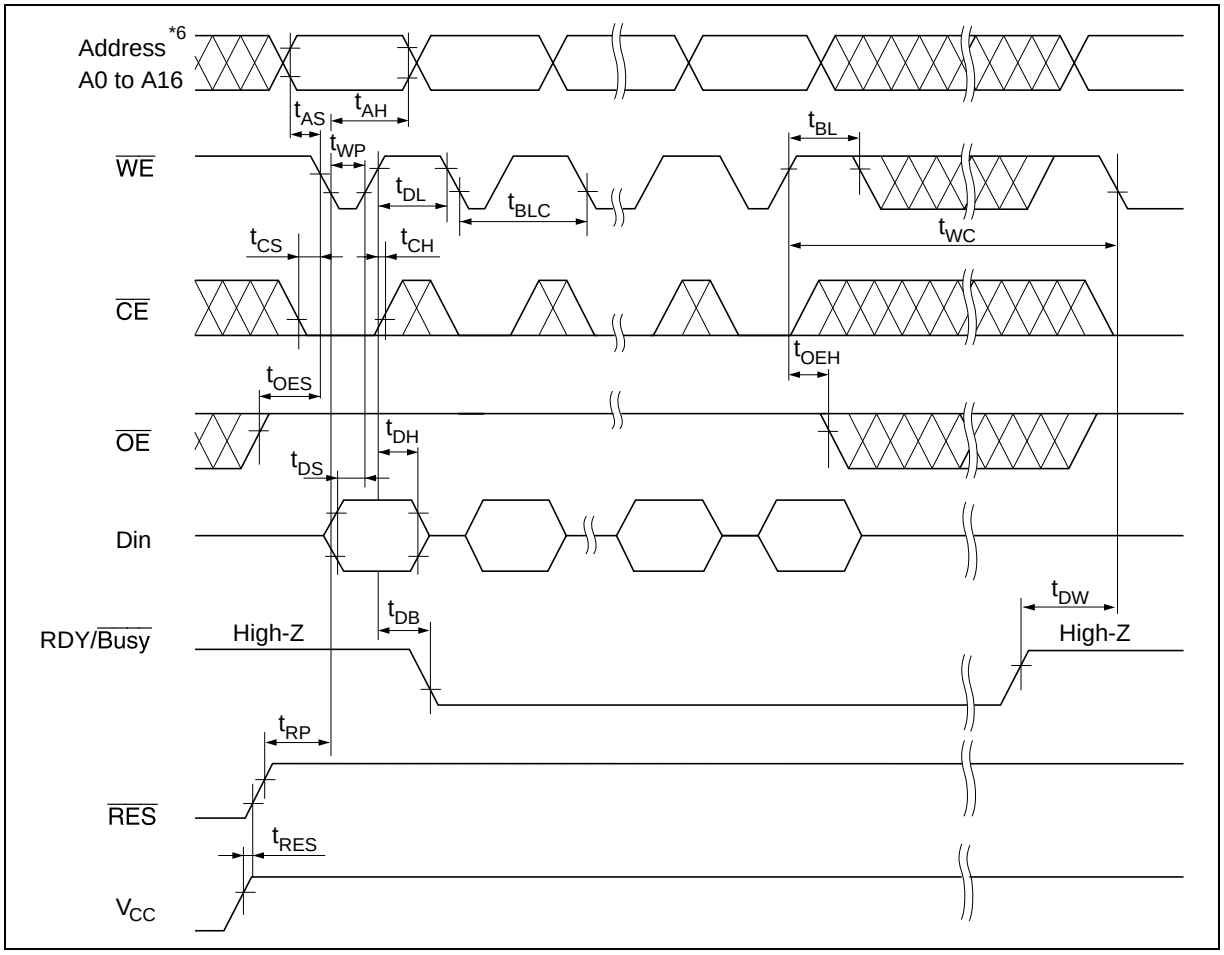
Byte Write Timing Waveform (1) ($\overline{WE}$ Controlled)



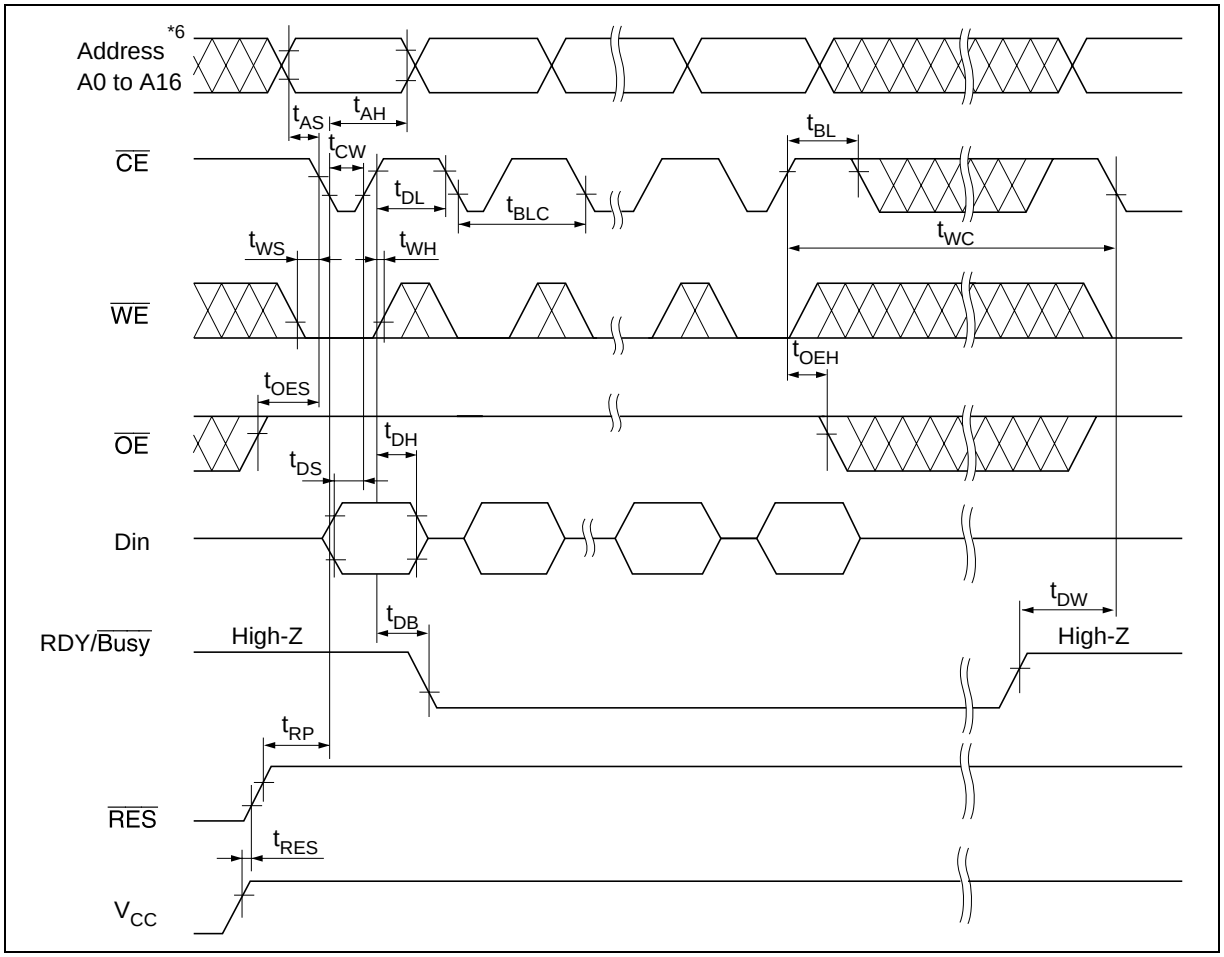
Byte Write Timing Waveform (2) ($\overline{CE}$ Controlled)



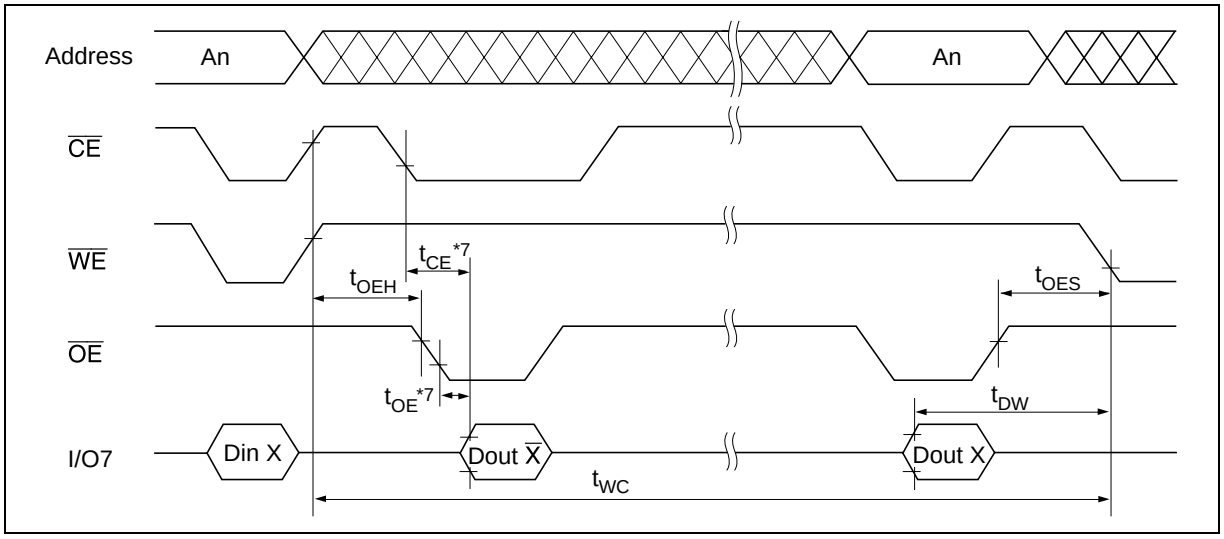
Page Write Timing Waveform (1) ($\overline{WE}$ Controlled)



Page Write Timing Waveform (2) ($\overline{CE}$ Controlled)



Data Polling Timing Waveform

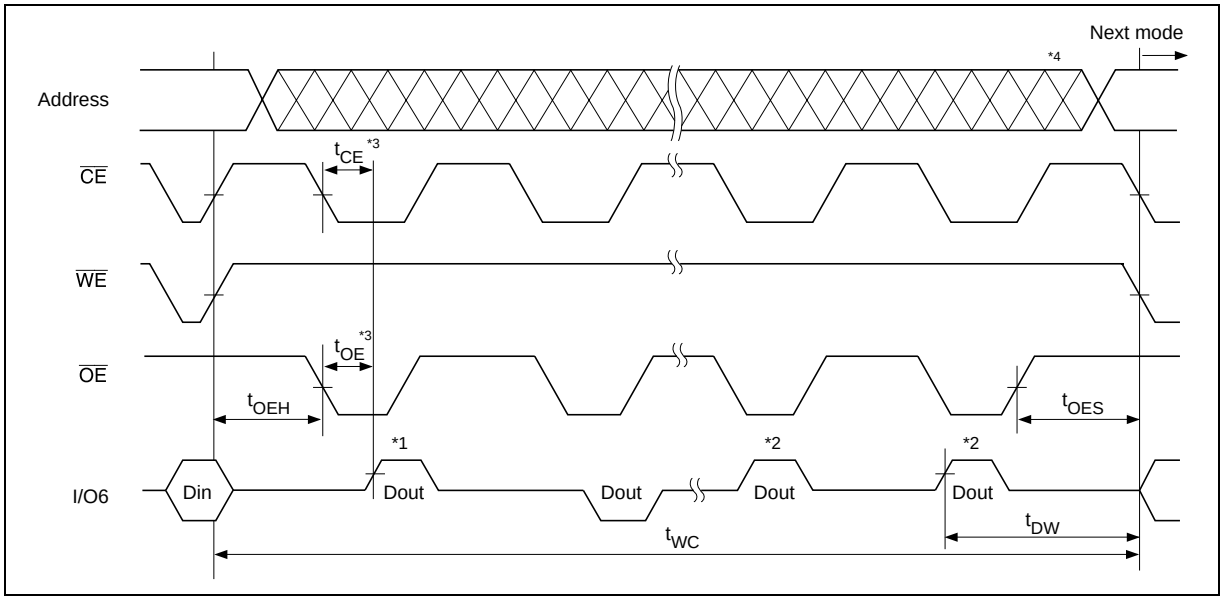


Toggle bit

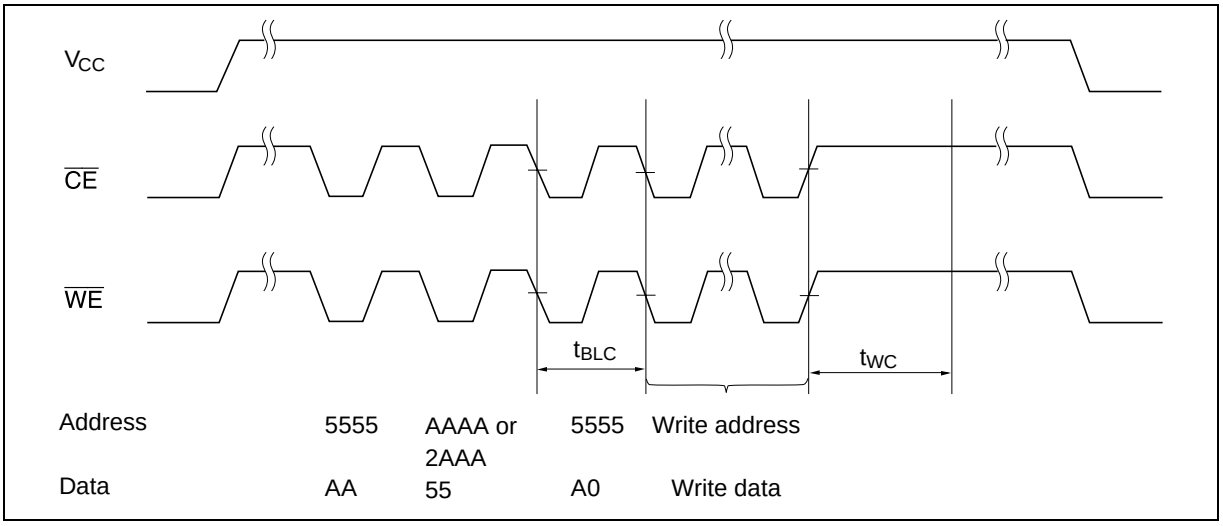
This device provide another function to determine the internal programming cycle. If the EEPROM is set to read mode during the internal programming cycle, I/O6 will charge from "1" to "0" (toggling) for each read. When the internal programming cycle is finished, toggling of I/O6 will stop and the device can be accessible for next read or program.

Notes: 1. I/O6 beginning state is "1".
2. I/O6 ending state will vary.
3. See AC read characteristics.
4. Any location can be used, but the address must be fixed.

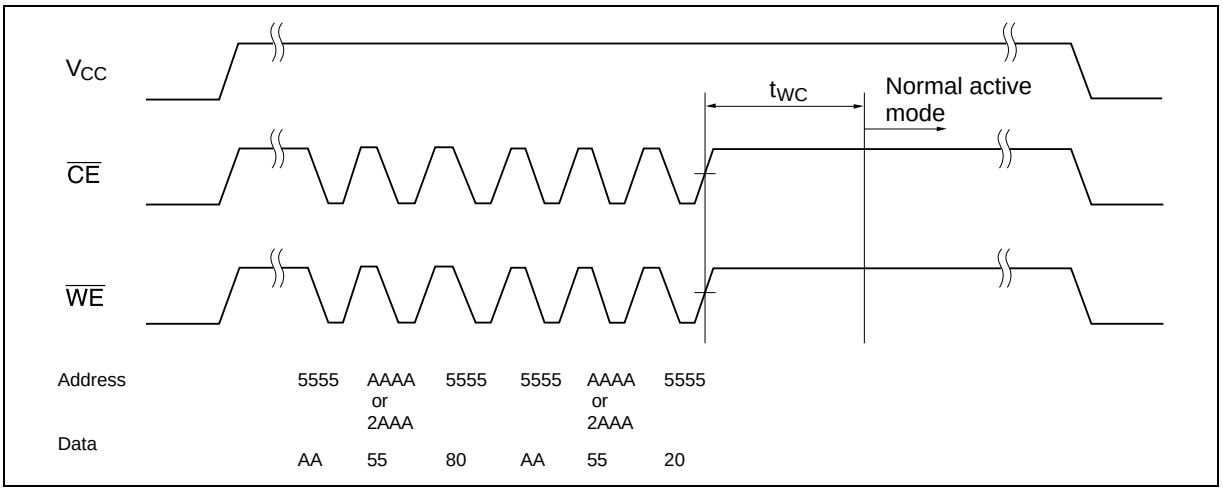
Toggle bit Waveform



Software Data Protection Timing Waveform (1) (in protection mode)



Software Data Protection Timing Waveform (2) (in non-protection mode)



Functional Description

Automatic Page Write

Page-mode write feature allows 1 to 128 bytes of data to be written into the EEPROM in a single write cycle. Following the initial byte cycle, an additional 1 to 127 bytes can be written in the same manner. Each additional byte load cycle must be started within 30 µs from the preceding falling edge of $\overline{WE}$ or $\overline{CE}$. When $\overline{CE}$ or $\overline{WE}$ is kept high for 100 µs after data input, the EEPROM enters write mode automatically and the input data are written into the EEPROM.

$\overline{Data}$ Polling

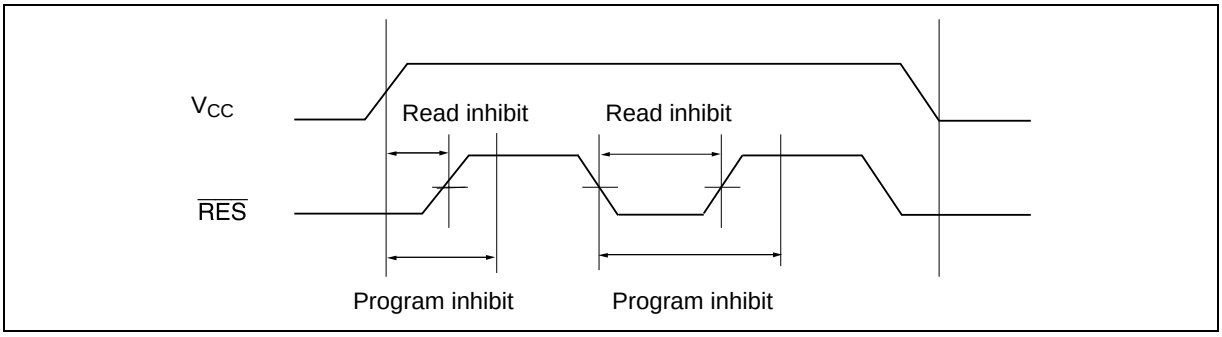
$\overline{Data}$ polling allows the status of the EEPROM to be determined. If EEPROM is set to read mode during a write cycle, an inversion of the last byte of data to be loaded outputs from I/O7 to indicate that the EEPROM is performing a write operation.

RDY/$\overline{Busy}$ Signal

RDY/$\overline{Busy}$ signal also allows status of the EEPROM to be determined. The RDY/$\overline{Busy}$ signal has high impedance except in write cycle and is lowered to V_{OL} after the first write signal. At the end of write cycle, the RDY/$\overline{Busy}$ signal changes state to high impedance.

$\overline{RES}$ Signal

When $\overline{RES}$ is low, the EEPROM cannot be read or programmed. Therefore, data can be protected by keeping $\overline{RES}$ low when V_{CC} is switched. $\overline{RES}$ should be high during read and programming because it doesn't provide a latch function.



$\overline{WE}$, $\overline{CE}$ Pin Operation

During a write cycle, addresses are latched by the falling edge of $\overline{WE}$ or $\overline{CE}$, and data is latched by the rising edge of $\overline{WE}$ or $\overline{CE}$.

Write/Erase Endurance and Data Retention Time

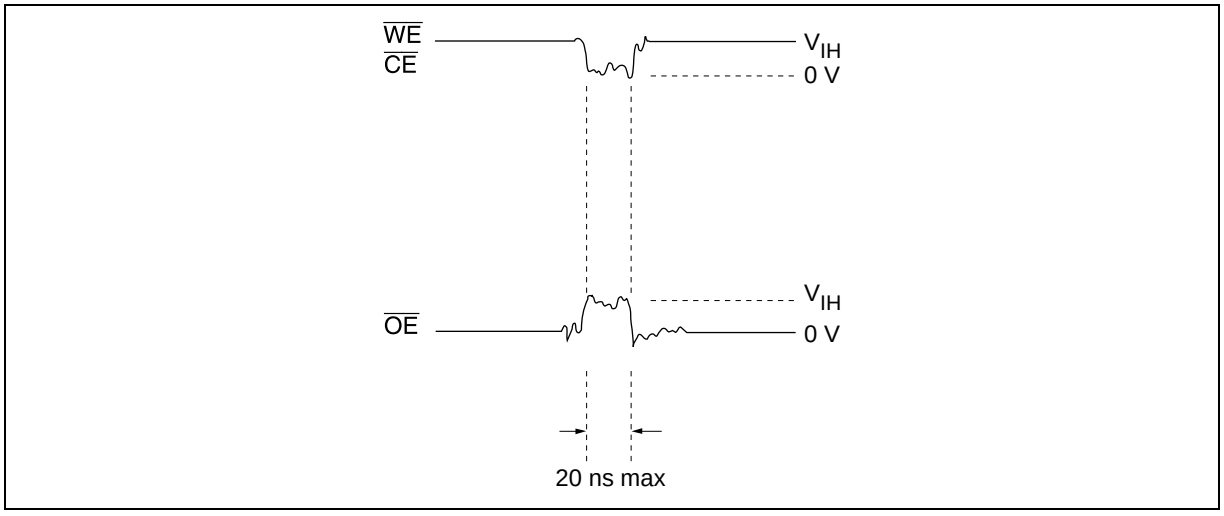
The endurance is 10^4 cycles in case of the page programming and 10^3 cycles in case of the byte programming (1% cumulative failure rate). The data retention time is more than 10 years when a device is page-programmed less than 10^4 cycles.

Data Protection

To prevent this phenomenon, this device has a noise cancellation function that cuts noise if its width is 20 ns or less in program mode.

1. Data Protection against Noise on Control Pins ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$) during Operation

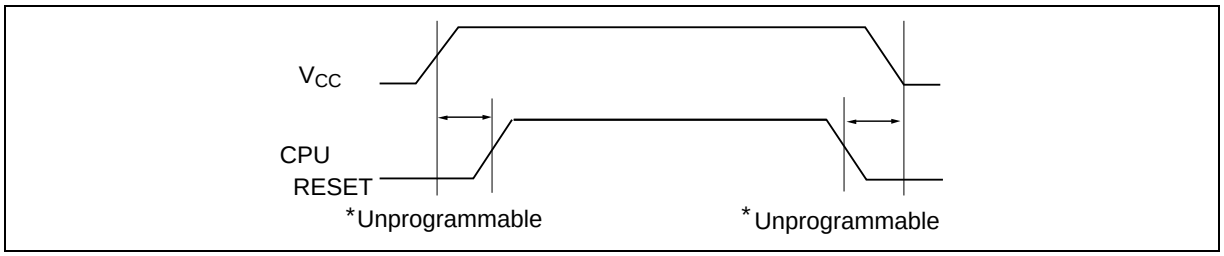
   During readout or standby, noise on the control pins may act as a trigger and turn the EEPROM to programming mode by mistake. Be careful not to allow noise of a width of more than 20 ns on the control pins.



2. Data Protection at V_{CC} On/Off

When V_{CC} is turned on or off, noise on the control pins generated by external circuits (CPU, etc) may act as a trigger and turn the EEPROM to program mode by mistake. To prevent this unintentional programming, the EEPROM must be kept in an unprogrammable state while the CPU is in an unstable state.

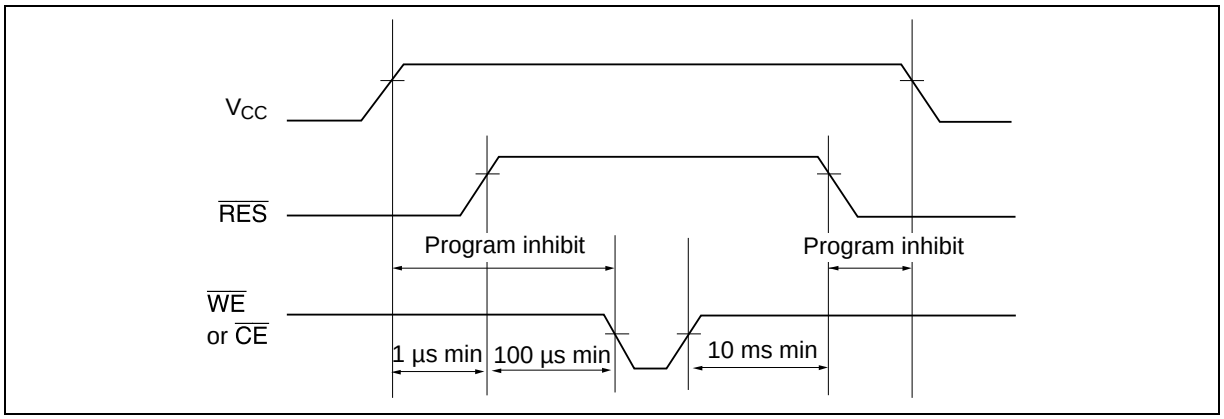
Note: The EEPROM should be kept in unprogrammable state during V_{CC} on/off by using CPU RESET signal.



2.1 Protection by $\overline{RES}$

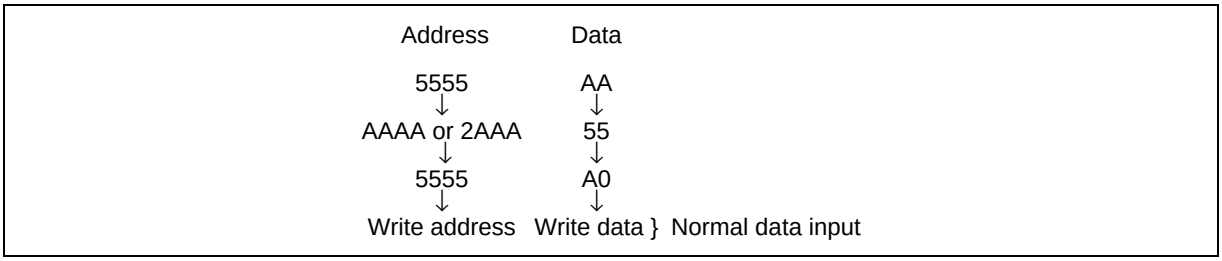
The unprogrammable state can be realized by that the CPU's reset signal inputs directly to the EEPROM's $\overline{RES}$ pin. $\overline{RES}$ should be kept V_{SS} level during V_{CC} on/off.

The EEPROM brakes off programming operation when $\overline{RES}$ becomes low, programming operation doesn't finish correctly in case that $\overline{RES}$ falls low during programming operation. $\overline{RES}$ should be kept high for 10 ms after the last data input.

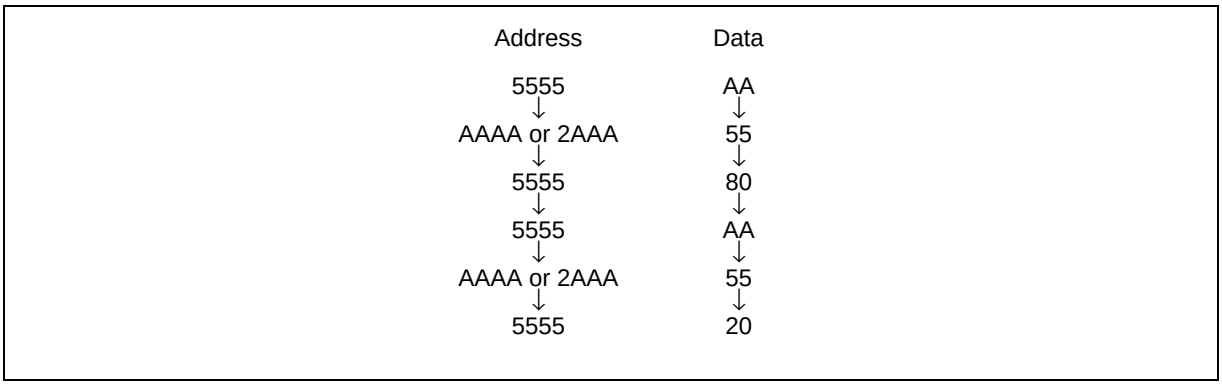


3. Software data protection

To prevent unintentional programming, this device has the software data protection (SDP) mode. The SDP is enabled by inputting the following 3 bytes code and write data. SDP is not enabled if only the 3 bytes code is input. To program data in the SDP enable mode, 3 bytes code must be input before write data.



The SDP mode is disabled by inputting the following 6 bytes code. Note that, if data is input in the SDP disable cycle, data can note be written.



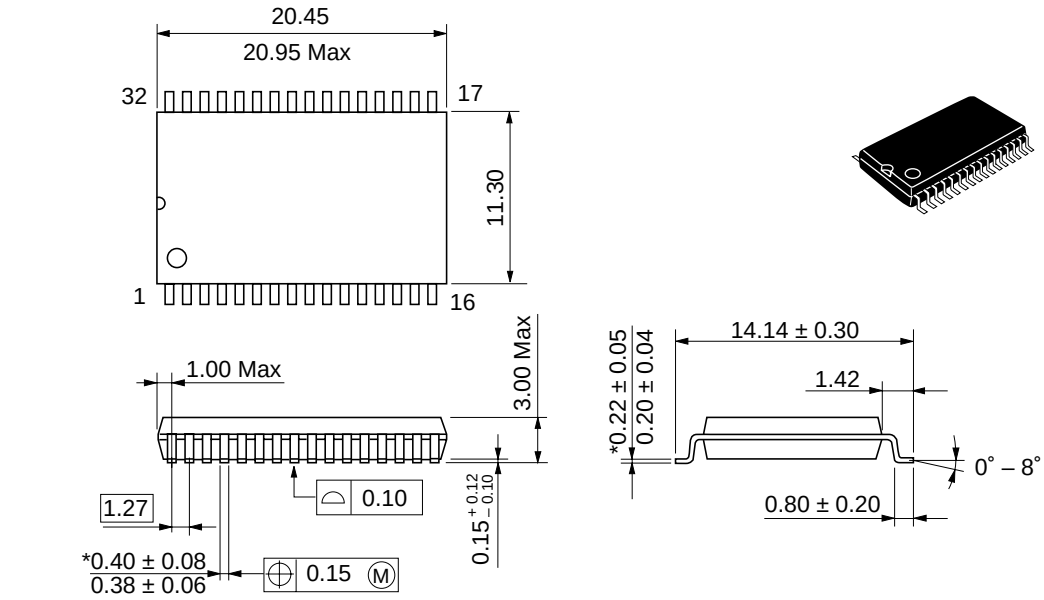
The software data protection is not enabled at the shipment.

Note: There are some differences between Renesas Technology's and other company's for enable/disable sequence of software data protection. If there are any questions , please contact with Renesas Technology's sales offices.

Package Dimensions

HN58C1001FP Series (FP-32D, FP-32DV)

Unit: mm



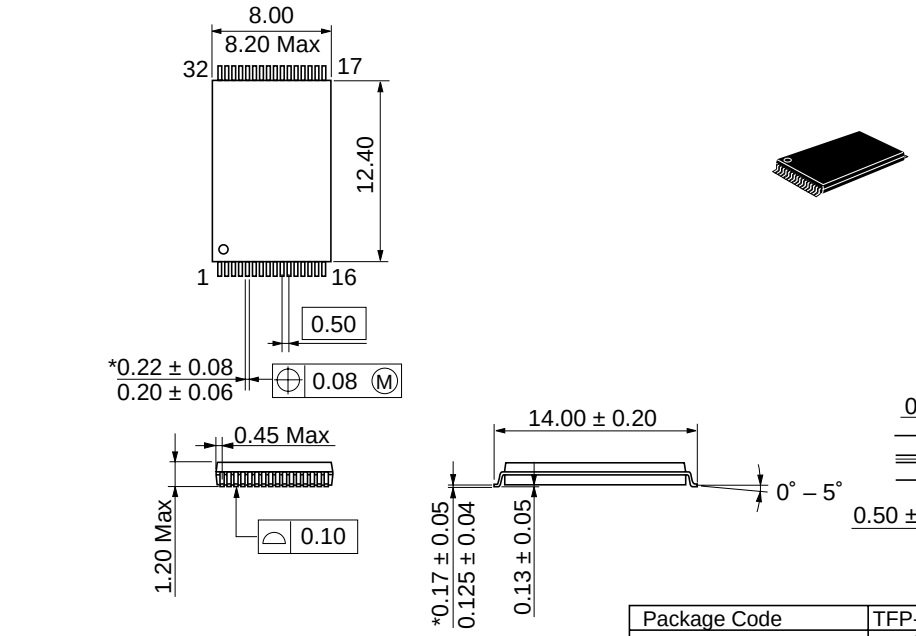
*Dimension including the plating thickness
Base material dimension

Package Code	FP-32D, FP-32DV
JEDEC	Conforms
JEITA	—
Mass (reference value)	1.3 g

Package Dimensions (cont.)

HN58C1001T Series (TFP-32DA, TFP-32DAV)

Unit: mm



*Dimension including the plating thickness
Base material dimension

Package Code	TFP-32DA, TFP-32DAV
JEDEC	Conforms
JEITA	Conforms
Mass (reference value)	0.26 g

Rev.	Date	Contents of Modification	
		Page	**Description**
0.0	Jul. 11. 1991	—	Initial issue
1.0	Jan. 10. 1992	—	Recommended DC Operating Conditions Addition of V_H
		5	DC Characteristics I_{CC3} max: 40 mA to 50 mA I_{CC3} test: Cycle = 200 ns to Cycle = 150 ns V_{IH} max: V_{CC} + 1 V to V_{CC} + 0.3 V V_H min: V_{CC} – 1.0 V to V_{CC} – 0.5 V
		6	AC Characteristics Change of Test Conditions Reference level: 1.8 V to 2.0 V t_{DL} min: 200 ns to 300 ns t_{BLC} min: 0.35 µs to 0.55 µs t_{WP}/t_{CW} min: 150 ns to 250 ns t_{CS}/t_{CH} to t_{WS}/t_{WH} ($\overline{CE}$ Controlled)
		16	Functional Description Deletion of Write Protection (2) Data Protection 2: during programming because to during programming and read because unprogrammable, standby or readout state to unprogrammable state Deletion of protection of mistake by $\overline{CE}$ = V_{CC} or $\overline{OE}$ = Low or $\overline{WE}$ = V_{CC} level at V_{CC} on/off Software data protection Address: AAAA to AAAA or 2AAA
		8	Change of Timing Waveforms
2.0	Jan. 21. 1993	—	Deletion of HN58C1001-12
		6	AC Characteristics t_{DH} min: 0 ns to 10 ns
		—	Deletion of Mode Description
		—	Addition of Reset function
		—	Change of erase/write cycles in page mode: 10^5 to 10^4
		—	Change of erase/write cycles in byte mode: 104 to 10^3
3.0	Apr. 23. 1993	14	Addition of Toggle Bit
4.0	Nov. 25. 1994	6	Capacitance Addition of note 1
		6	AC Characteristics Write cycle: Addition of note 2,3 Addition of t_{DW} min: 150 ns
		11	Page write timing waveform Addition of note 1
5.0	May. 23. 1995	—	Deletion of HN58C1001R series (TFP-32DAR)

Revision Record (cont.)

6.0	Apr. 8. 1997	—	Change of format
		6	AC Characteristics
			Addition of note.6
		8	Timing Waveforms
			Toggle bit
			Addition of note.3, 4
		16	Functional Description
			Addition of CPU Reset timing waveform
			Data protection 3: Addition of note
7.0	Oct. 31. 1997	8	Timing Waveforms
			Read Timing Waveforms: Correct error
8.00	Nov. 27. 2003	—	Change format issued by Renesas Technology Corp.
		2	Ordering Information
			Deletion of HN58C1001P-15
			Addition of HN58C1001FP-15E, HN58C1001T-15E
		20-21	Package Dimensions
			Deletion of DP-32
			FP-32D to FP-32D, FP-32DV
			TFP-32DA to TFP-32DA, TFP-32DAV

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Colophon 1.0