FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-13106-2E

Linear IC Converter

CMOS

A/D Converter

(With 24-Channel Input at 10-bit Resolution)

MB88111

■ DESCRIPTION

The MB88111 is an analog-to-digital converter that converts its analog input to a 10-bit digital value and outputs it as serial data.

The MB88111 employs a successive approximation method for A/D conversion. It has 24 input channels to be A/D converted selectively by setting in an internal register.

Since the MB88111 can input and output 16-bit serial data in synchronization with the clock, it can be easily connected to the serial I/O port in a 16-bit microcontroller.

■ FEATURES

- 24-channel analog input
- RC-type successive approximation system with a sample-and-hole circuit
- 10-bit resolution
- Conversion speed within 50 μs (at a system clock rate of 1 MHz)
- Digitally converted data output from the MSB
- Digitally converted data output as 16-bit serial data
- Clock-synchronous serial transfer system
- Internal extended serial interface
- Capable of triggering A/D conversion through an external pin
- Capable of input through an 8-channel port
- Serial data output format selectable using an external pin
- 10-bit monotonicity
- No missing code
- Power supply voltage ranging from 3.5 to 5.5 V

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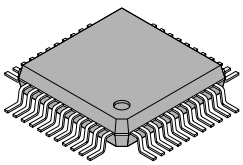
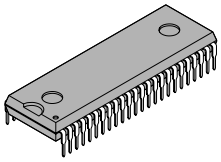
■ PACKAGES

44-pin, Plastic QFP



(FPT-44P-M11)

48 pin, Plastic SH-DIP



(DIP-48P-M01)

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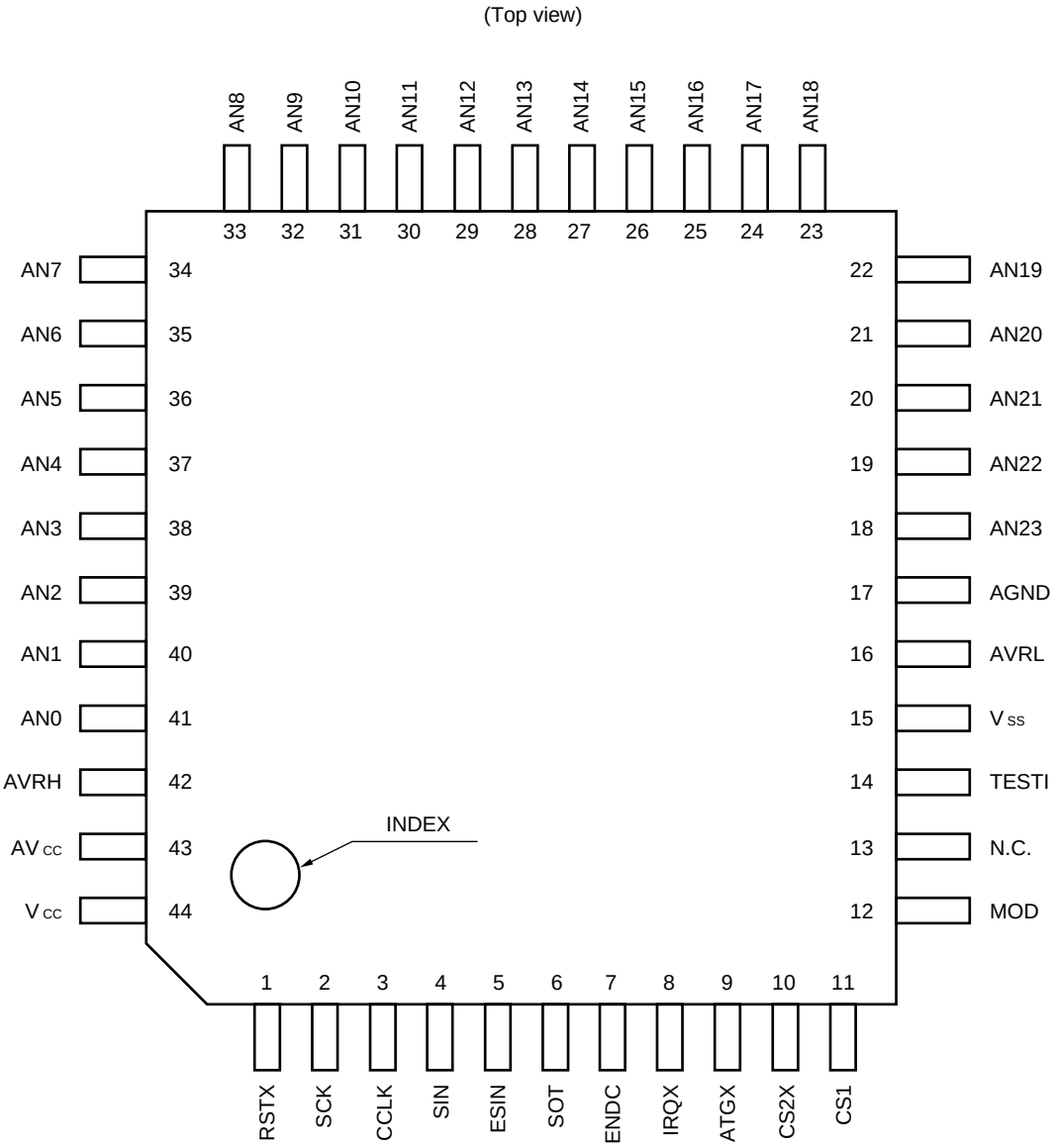
- Operating temperature ranging from –40 to +50°C
- CMOS process
- Package options of 44-pin QFP and 48-pin SH-DIP

■ PIN ASSIGNMENT



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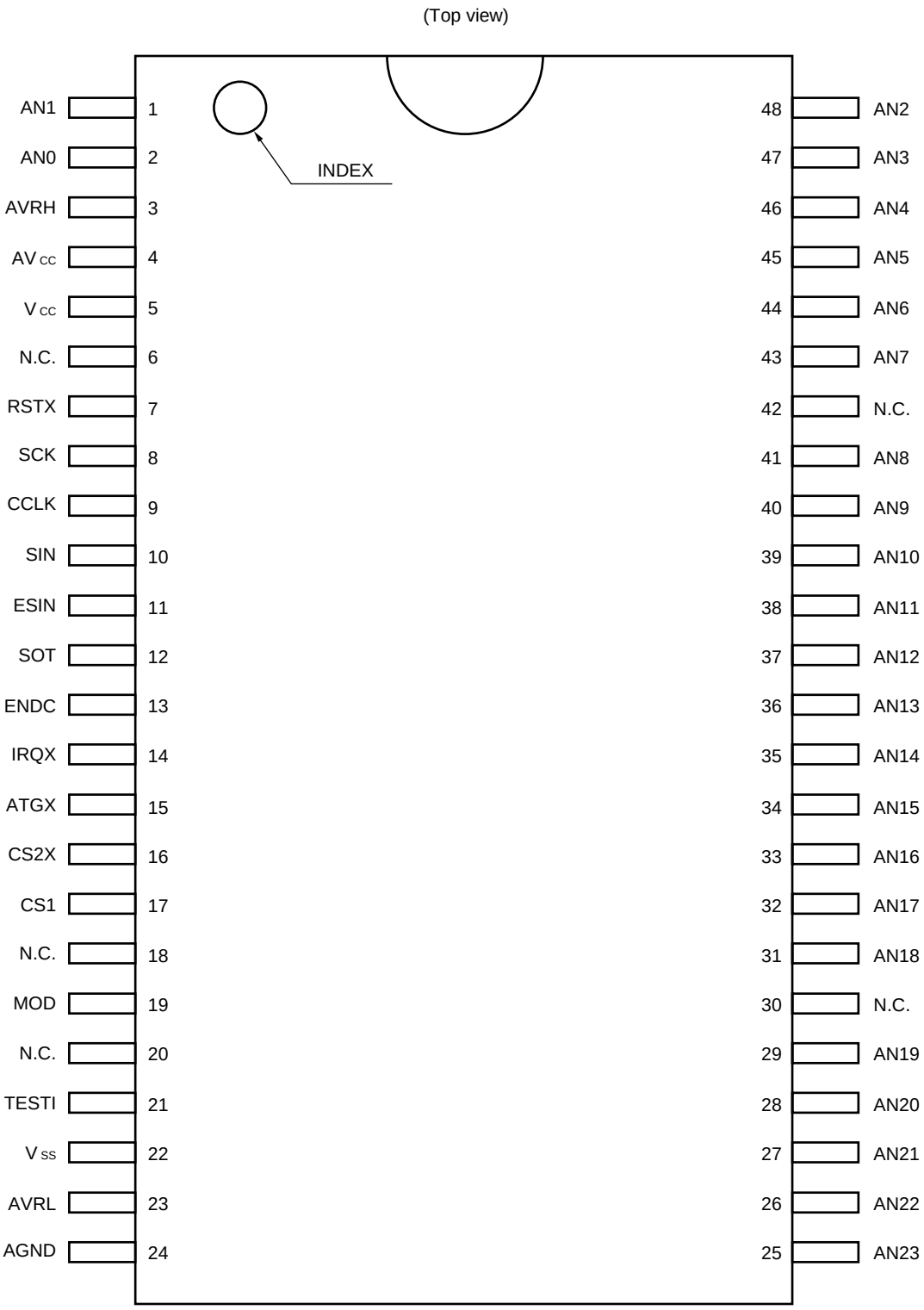

(DIP-48P-M01)

■ PIN DESCRIPTION

Pin no.		Symbol	I/O	Circuit type	Descriptions
QFP	DIP				
41 to 26	2 to 1, 48 to 43, 41 to 34	AN0 to AN15	I	F	Analog input pins. The pin to be subject to conversion is selected by the command input through the SIN pin. Also, a series of pins from AN16 to AN23 can be used as a port input.
25 to 18	33 to 31, 29 to 25	AN16 to AN23		G	
12	19	MOD	I	A	Pin for selecting a serial data output mode: "L": Mode A for output from the SOT pin in synchronization with the fall of the SCK signal. "H": Mode B for output from the SOT pin in synchronization with the rise of the SCK signal.
11 10	17 16	CS1 CS2X	I	A	Input pins for selecting an extended serial interface mode. Setting the CS1 level to "H" and the CS2X level to "L" enables A/D converted data transfer. Setting the CS1 level to "L" or the CS2X level to "H" clears the register command without affecting A/D conversion. Serial data input to the external extended serial input pin ESIN is output to the SOT pin as it is. (See Section 7 "Extended Serial Interface" in "■ OPERATION.")
4	10	SIN	I	B	Serial data input pin This pin is a hysteresis input with a filter.
6	12	SOT	O	H	Serial data output pin
3	9	CCLK	I	B	System clock input pin This pin is a hysteresis input.
2	8	SCK	I	B	Serial data transfer clock input pin This pin is a hysteresis input with a filter.
9	15	ATGX	I	C	External trigger input pin. This pin incorporates a pull-up resistor. The ATC command initiates A/D conversion at the rise of the signal at this pin. The pin is a hysteresis input.
8	14	IRQX	O	H	A/D conversion interrupt signal input pin. The signal level becomes "L" upon completion of A/D conversion; it becomes "H" upon reception of data to be converted.
7	13	ENDC	O	H	A/D conversion completion signal output pin. The signal level becomes "H" upon completion of A/D conversion; it becomes "L" upon reception of data to be converted.
5	11	ESIN	I	A	Serial input extension input pin. When the CS1 level is "L" or the CS2X level is "H," data input to the ESIN pin is output to the SOT pin as it is.
1	7	RSTX	I	D	Reset signal input pin. This pin incorporates a pull-up resistor. Setting the signal level to "L" initializes the internal circuit of the device. This pin is a hysteresis input with a filter.

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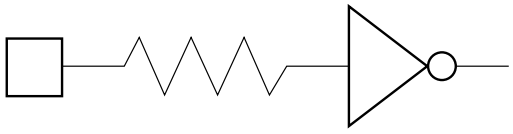
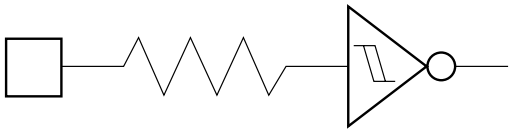
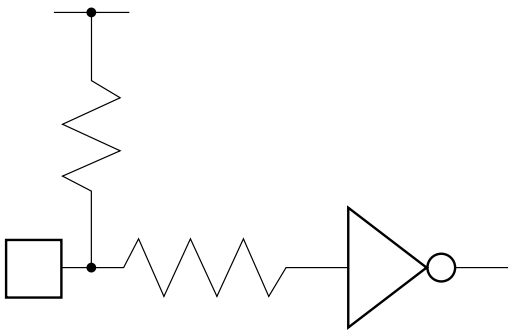
Pin no.		Symbol	I/O	Circuit type	Descriptions
QFP	DIP				
14	21	TESTI	I	E	Test input pin. This pin incorporates a pull-down resistor. Maintain the pin at “L” level during normal use.
44	5	V_{CC}	—	—	Digital circuit power supply pin
15	22	V_{SS}	—	—	Digital circuit ground pin
43	4	AV_{CC}	—	—	Analog circuit power supply pin
17	24	AGND	—	—	Analog circuit ground pin
42	3	AVRH	—	—	Reference (high) voltage input pin
16	23	AVRL	—	—	Reference (low) voltage input pin
13	6, 18, 20, 30, 42	N.C.	—	—	Non-connection pin

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• CMOS input
B		• Hysteresis input • CMOS input
C		• Input with pull-up resistor • CMOS input

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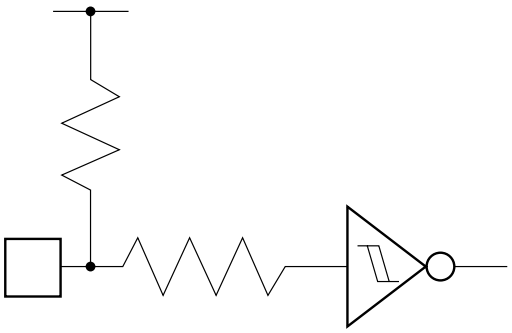
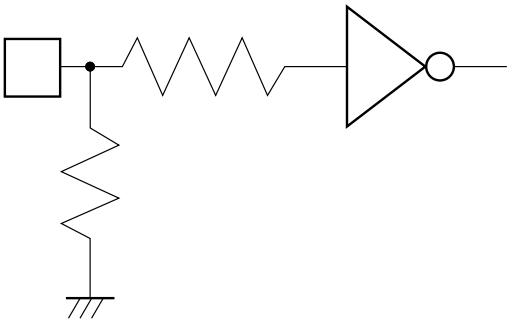
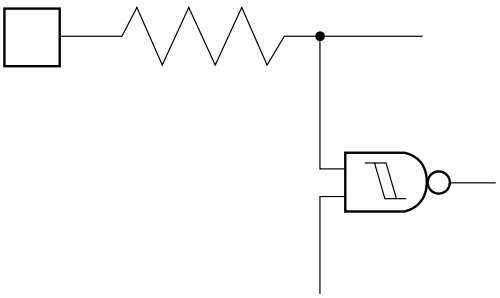
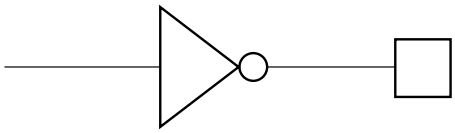
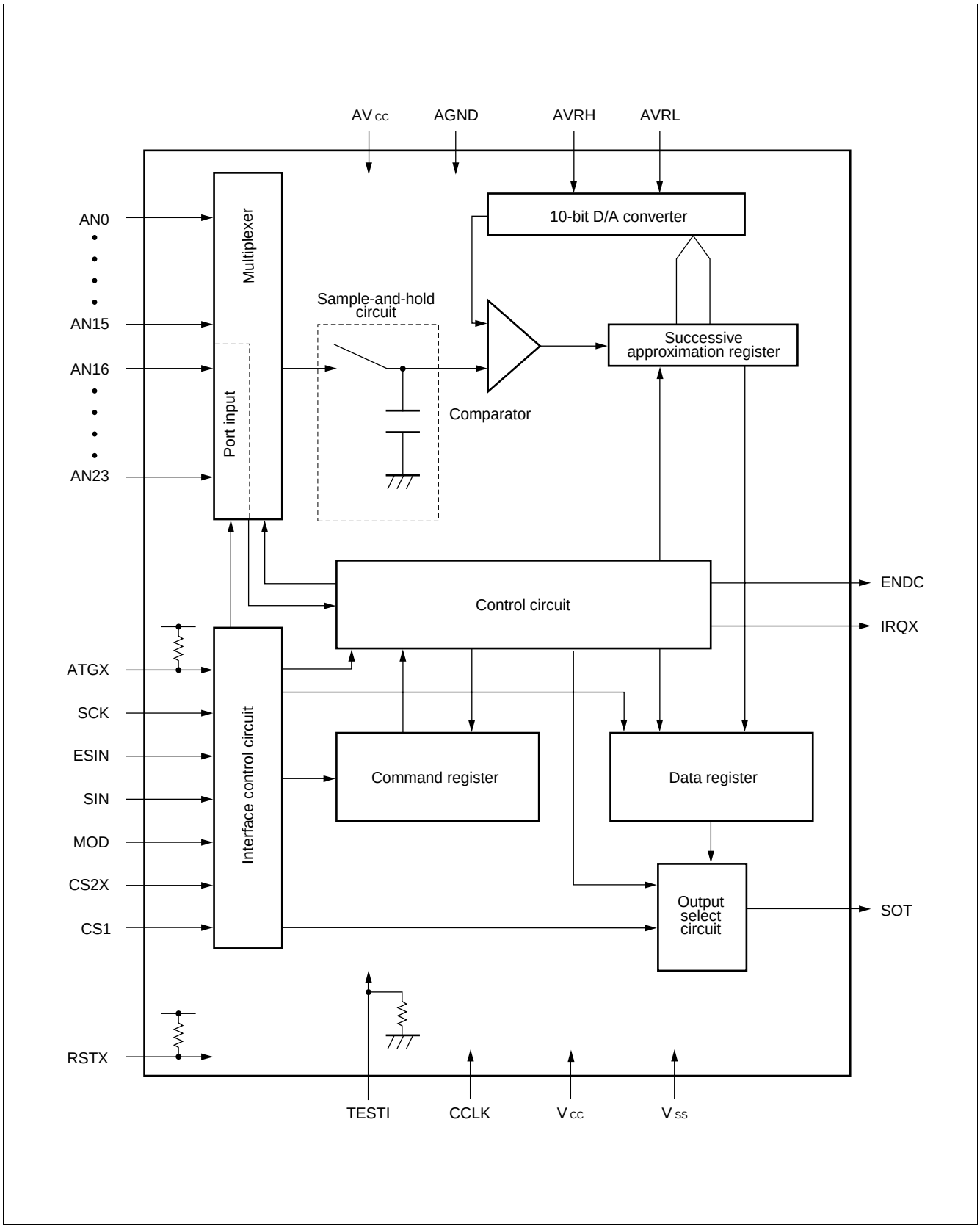
Type	Circuit	Remarks
D		• Input with pull-up resistor • Hysteresis input • CMOS input
E		• Input with pull-down resistor • CMOS input
F		• Analog input
G		• Analog input • Hysteresis input • CMOS input
H		• CMOS output

■ BLOCK DIAGRAM



■ FUNCTIONAL DESCRIPTION

1. SC (Serial Command) Register (Reset status: 0000H)

The SC register contains an A/D converter command and an input channel identification. Accessing this register after releasing it from the reset status activates the A/D converter.

Note that this register accepts setting even during A/D conversion.

Note also that input of a command to the register must take an interval of at least 4 CCLKs after input of the previous command.

MSB															LSB
bf	be	bd	bc	bb	ba	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Command			Channel					Don't care							

(1) Command bits

A string of command bits selects an A/D converter command such as STOP. Setting a command during execution of another command cancels the command currently being executed.

bf	be	bd	Command name	Function
0	0	0	STOP	Stops A/D conversion (if it is being executed) and initializes the A/D converter. This command has the same effect as RSTX.
0	0	1	STC	Executes A/D conversion of the specified channel once. (See Section 3 “STC (Standard Conversion) Command.”)
0	1	0	—	Unused (*)
0	1	1	—	Unused (*)
1	0	0	NOP	No-op command. Input of this command during A/D conversion does not affect operation. If followed by this command, the ATC command can transfer converted data while holding the NOP command.
1	0	1	ATC	The basic operation of this command is the same as that of the STC command. The ATC command can leave the A/D conversion start timing to the external trigger pin ATGX. (See Section 4 “ATC (Auto Trigger Conversion) Command.”)
1	1	0	—	Unused (*)
1	1	1	—	Unused (*)

* : These command settings cause the STOP command to be executed.

(2) Channel select bits

A string of channel select bits selects the pin to be subject to A/D conversion. This bit string is enabled only for the STC or ATC command.

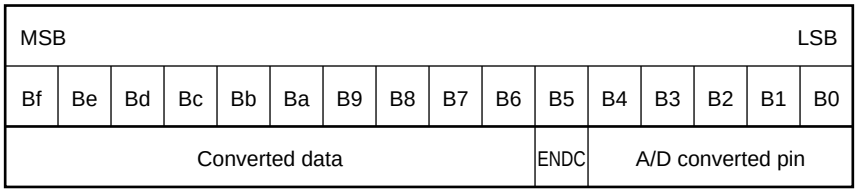
bc	bb	ba	b9	b8	Pin to be selected	bc	bb	ba	b9	b8	Pin to be selected
0	0	0	0	0	AN0	1	0	0	0	0	AN16
0	0	0	0	1	AN1	⋮	⋮	⋮	⋮	⋮	⋮
0	0	0	1	0	AN2	1	0	1	1	1	AN23
0	0	0	1	1	AN3	1	1	0	0	0	Undefined (*1)
0	0	1	0	0	AN4	1	1	0	0	1	
⋮	⋮	⋮	⋮	⋮	⋮	1	1	0	1	0	
0	1	0	1	1	AN11	1	1	0	1	1	
0	1	1	0	0	AN12	1	1	1	0	0	
0	1	1	0	1	AN13	1	1	1	0	1	
0	1	1	1	0	AN14	1	1	1	1	0	
0	1	1	1	1	AN15	1	1	1	1	1	Port input AN16 to AN23 (*2)

*1: These settings of the bit string cause the STOP command to be executed.

*2: This setting is enabled only for the STC command. (See Section 5 “Port Input Command.”)
If this setting is made for the ATC command, the STOP command is executed.

2. Data Output Format

Upon completion of A/D conversion, the ENDC pin level becomes “H” and the IRQX pin level becomes “L.” Execution of serial transfer at this time outputs data in the format illustrated below. The data output timing can be selected by the MOD pin between the falling edge (mode A) or rising edge (mode B) of the SCK signal. When the ENDC pin level is “L,” 0000H is output.



ENDC (A/D conversion completion flag): This bit is set to “1” upon completion of A/D conversion. It is set to “0” upon completion of serial transfer.

Note: SCK input upon low-to-high transition of the ENDC pin level should be avoided. Otherwise, data may not be output correctly.

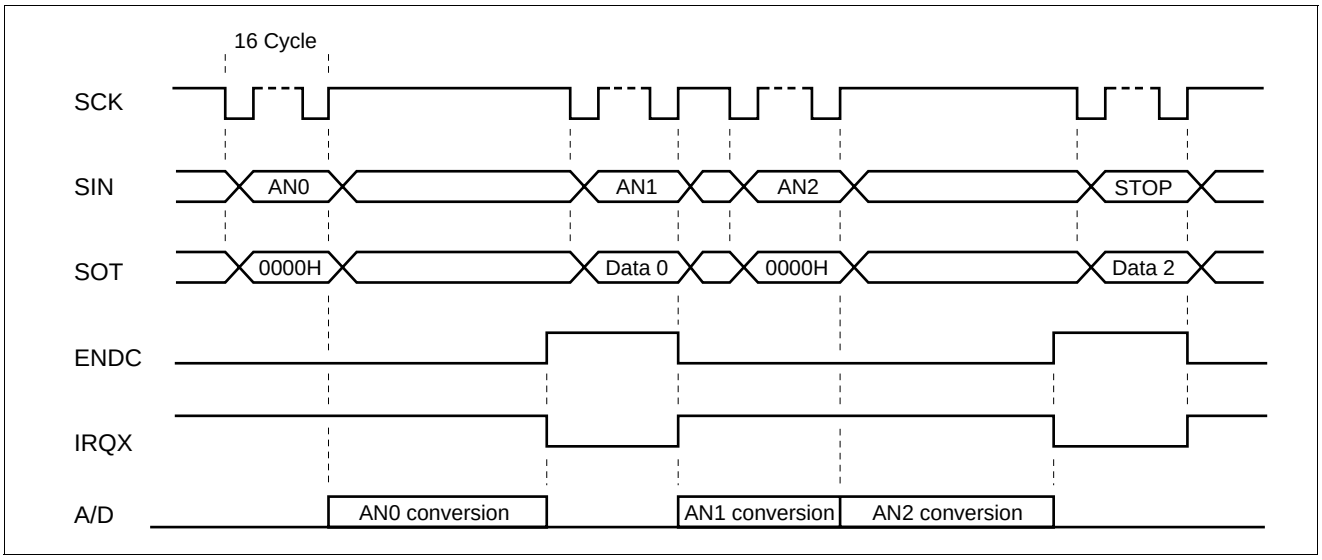
3. STC (Standard Conversion) Command

Input of the STC command executes A/D conversion of the specified channel once.

Impletion of A/D conversion, the ENDC signal rises while the IRQX signal falls. Clock input to the SCK pin after A/D conversion outputs data to the SOT pin. Upon completion of data output, the ENDC signal falls while the IRQX signal rises. If the next command is STOP or NOP, the A/D conversion is terminated. If the STC command is input during A/D conversion, the command currently being executed is cancelled and the STC command is executed.

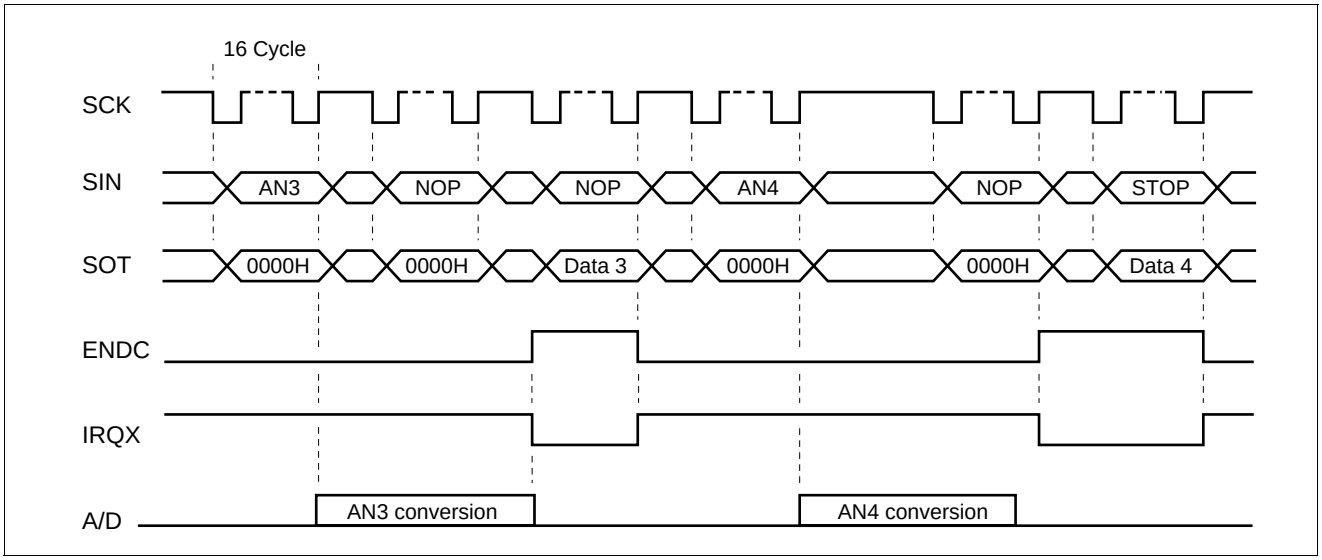
- **Example of STC command execution (1)**

STC command input during A/D conversion cancels the current command and executes A/D conversion of the new specified channel. Output data at this time is 0000H.



- **Example of STC command execution (2)**

NOP command input during A/D conversion does not affect operation. Output data at this time is 0000H. If A/D conversion is completed during NOP command input, the ENDC and IRQX pin levels become “H” and “L” respectively upon completion of the NOP command input.

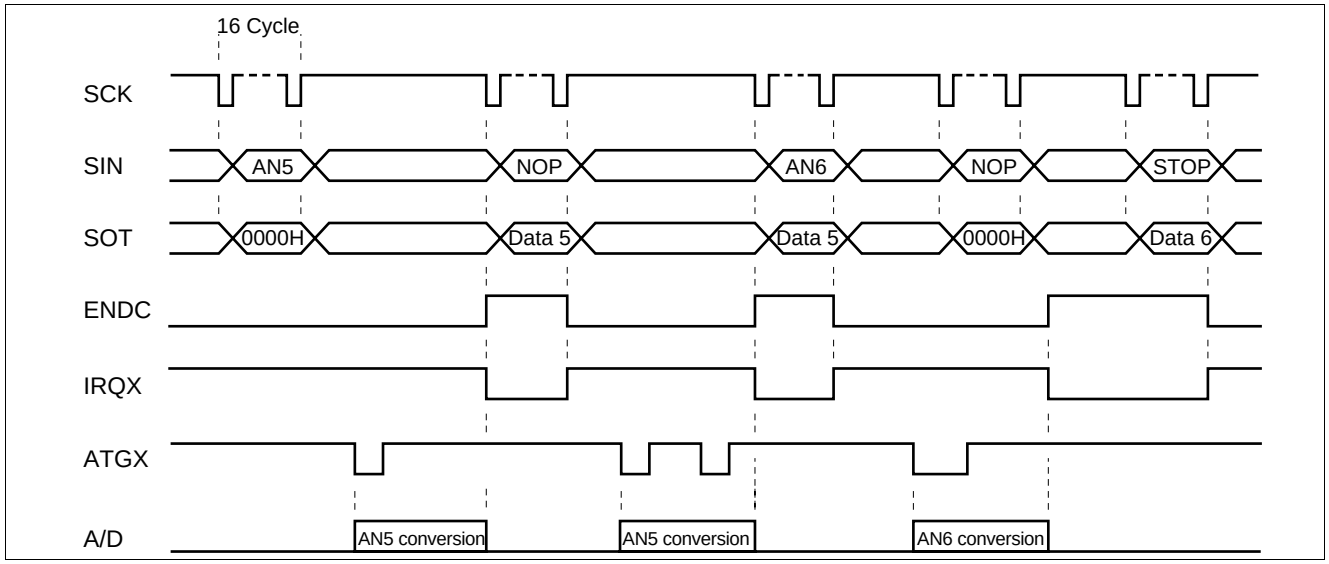


4. ATC (Auto Trigger Conversion) Command

The ATC command is the same as the STC command in basic operation. This command can initiates A/D conversion using the external trigger pin ATGX. The external trigger signal is sampled by 1 µs clock and filtered by 1 clock. The external trigger signal input during A/D conversion is ignored. If the next command is the STOP command, A/D conversion is terminated. If it is the NOP command, the ATC command is executed continuously. The channel cannot be changed at this time. To change the channel, input the ATC command to that effect.

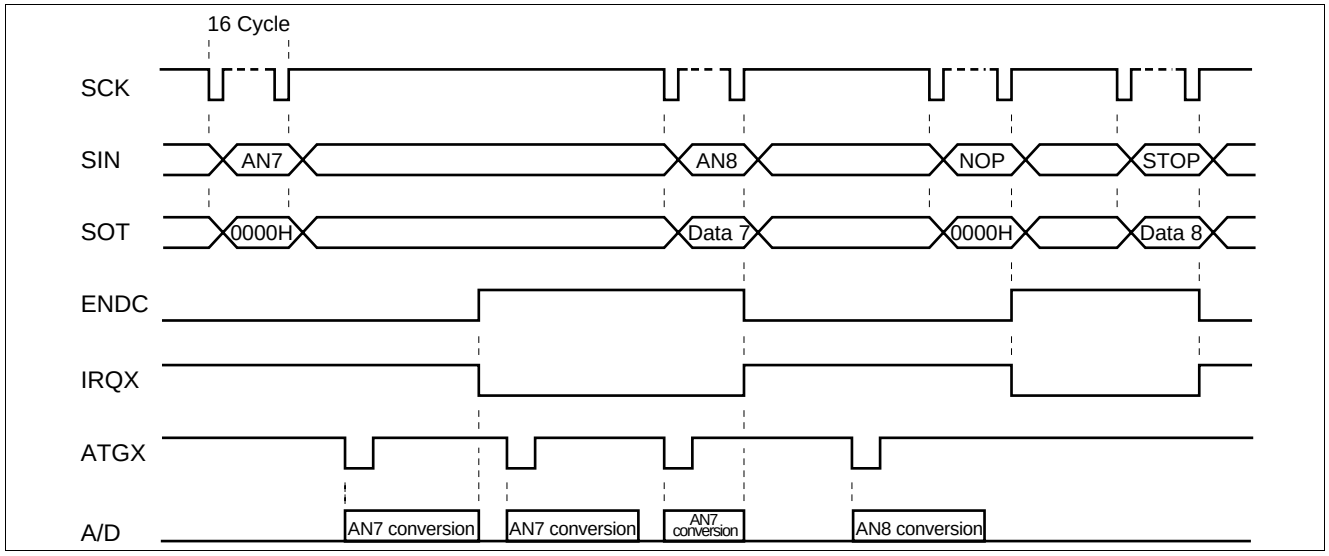
- **Example of ATC command execution (1)**

  NOP command input during A/D conversion enables the same channel to be A/D converted.
  An attempt to set the ATGX signal low during A/D conversion is ignored.
  NOP command input during A/D conversion does not affect operation. Output data at this time is 0000H.



- **Example of ATC command execution (2)**

Setting the ATGX signal low again after A/D conversion restarts A/D conversion.
In data output mode B, however, do not use the ATC command in this way, or data will not be output correctly.
If A/D conversion is completed during NOP command input, the ENDC and IRQX pin levels become “H” and “L” respectively upon completion of the NOP command input.



5. Port Input Command

The port input command executes I/O evaluation of 8-channel inputs from the AN16 to AN23 pins at a prescribed threshold in 10 clock cycles and outputs the results as port input data. The processing sequence is activated each time port input is selected by the STC command. Port input data is output in the following format:

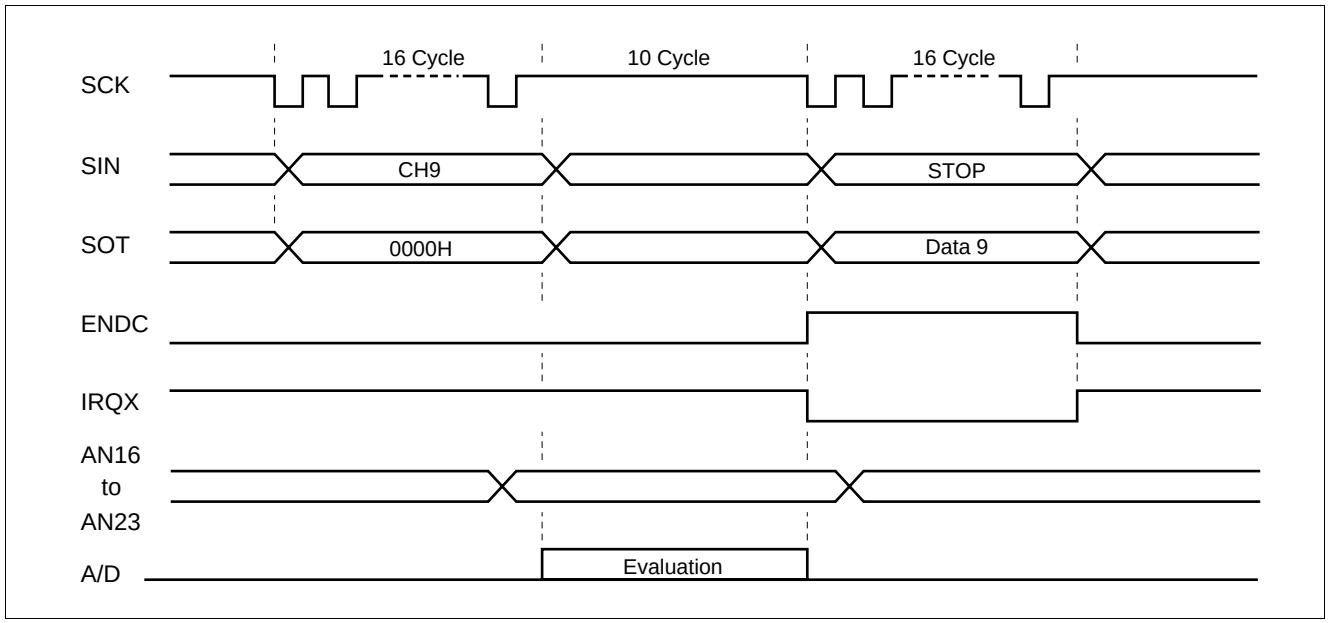
MSB															LSB
Bf	Be	Bd	Bc	Bb	Ba	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Evaluation data								"0"		ENDC	"1"				

Evaluation data:
The evaluation values of AN23 to AN16 are output to bits Bf to B8.

Evaluation value
"H": Vin ≥ 0.8 x Vcc
"L": Vin ≤ 0.2 x Vcc

ENDC (A/D completion flag):
This bit is set to "1" upon completion of A/D conversion. It is set to "0" upon completion of serial transfer.

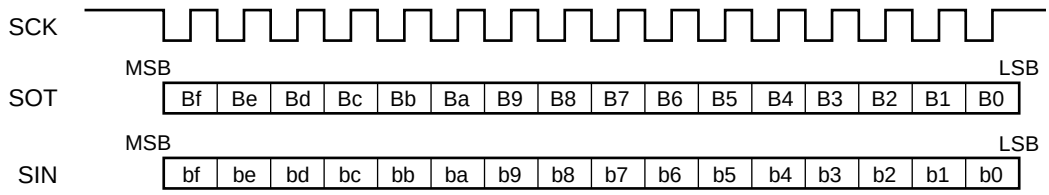
- **Example of STC command execution (3) (Port input command)**



6. Serial Output Select Function

The MB88111 can select the serial data output timing between the rising edge or falling edge of the clock signal according to the setting of the MOD pin.

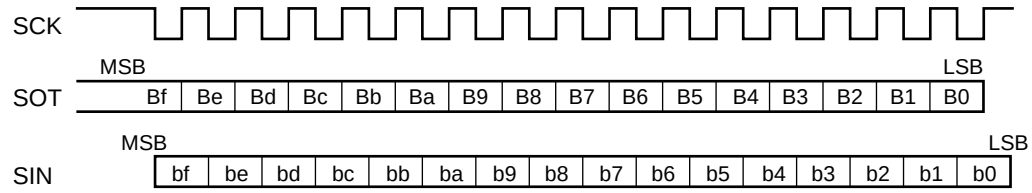
Mode A (MOD = "L")



Serial data is output at the falling edge of the SCK signal.

Note: A/D converted data is not guaranteed if the MOD pin is switched when the ENDC signal is active. Before changing the output mode, make the ENDC inactive or set the RSTX pin level to "L" after switching the MOD pin.

Mode B (MOD = "H")



Serial data is output at the rising edge of the SCK signal.

Note: A/D converted data is not guaranteed if the MOD pin is switched when the ENDC signal is active. Before changing the output mode, make the ENDC inactive or set the RSTX pin level to "L" after switching the MOD pin. The first bit is output when the ENDC signal becomes "H."

7. Extended Serial Interface

The MB88111 can select whether to output A/D converted data or to output data input to the ESIN pin by controlling the CS1 and CS2X pins.

CS1	CS2X	SOT pin
H	L	A/D converted data
L	L	Connection to the ESIN pin
L	H	
H	H	

Note: A/D converted data is not guaranteed if the CS1 or CS2X setting is changed during SCK input.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

(V_{SS} = AGND = 0 V)

Parameter	Symbol	Conditions	Ratings		Unit
			Min.	Max.	
Power supply voltage	V_{CC}	Based on V_{SS} (Ta = +25°C)	–0.3	+7.0	V
	AV_{CC}		–0.3	+7.0*	V
	AVRH		–0.3	+7.0*	V
Input voltage	V_{IN}		–0.3	V_{CC} + 0.3	V
Output voltage	V_{OUT}		–0.3	V_{CC} + 0.3	V
Power consumption	P_D	—	—	150	mW
Storage temperature	T_{stg}	—	–55	+150	°C

* : $V_{CC} \geq AV_{CC} \geq$ AVRH

2. Recommended Operating Conditions

Parameter	Symbol	Values		Unit
		Min.	Max.	
Power supply voltage	V_{CC} AV_{CC}	3.5*	5.5*	V
	V_{CC} AGND	0	0	V
	AVRH	$AV_{CC} \times 0.8$	AV_{CC}	V
	AVRL	0	$AV_{CC} \times 0.2$	V
Operation temperature	Ta	–40	+105	°C

* : $V_{CC} \geq AV_{CC} \geq$ AVRH

3. DC Characteristics

(1) Digital section

(V_{CC} = +3.5 V to +5.5 V, V_{SS} = AGND = 0 V, Ta = –40°C to +105°C)

Parameter	Pin name	Symbol	Conditions	Value			Unit
				Min.	Typ.	Max.	
Power supply voltage	V_{CC}	V_{CC}	—	3.5	5.0	5.5	V
Power supply current		I_{CC}	Operation at CLK = 1 MHz (with no load)	—	0.5	1.5	mA
Low-level input leakage current	MOD, CCLK CS1, CS2X SCK, ESIN SIN	I_{IZL1}	$V_{IN} = V_{SS}$	–2	—	2	µA
	ATGX RSTX	I_{IZL2}	$V_{IN} = V_{SS}$ V_{CC} = 5.0 V	–200	–100	–50	µA
High-level input leakage current	MOD, CCLK CS1, CS2X SCK, ESIN SIN, ATGX RSTX	I_{IZL1}	$V_{IN} = V_{CC}$	–2	—	2	µA
Low-level input voltage	MOD, ESIN CS1, CS2X	V_{IL}	—	V_{SS} – 0.3	—	0.3 V_{CC}	V
	SCK, CCLK SIN, ATGX RSTX, *	V_{ILS}	—	V_{SS} – 0.3	—	0.2 V_{CC}	V
High-level input voltage	MOD, ESIN CS1, CS2X	V_{IH}	—	0.7 V_{CC}	—	V_{CC} + 0.3	V
	SCK, CCLK SIN, ATGX RSTX, *	V_{IHS}	—	0.8 V_{CC}	—	V_{CC} + 0.3	V
Hysteresis width	SCK, CCLK SIN, ATGX RSTX, *	V_{HYS}	—	0.02 V_{CC}	—	0.3 V_{CC}	V
Low-level output voltage	SOT IRQX ENDC	V_{OL}	I_{OL} = 2.5 mA	—	—	0.4	V
High-level output voltage		V_{OH}	I_{OH} = –400 µA	V_{CC} – 0.4	—	—	V

* : AN16 to AN23 (port input mode)

(2) Analog section

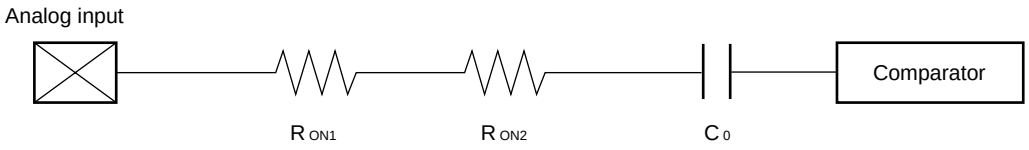
(AV_{CC}, V_{CC} = +3.5 V to +5.5 V ($V_{CC} \geq AV_{CC}$), V_{SS} = AGND = 0 V, Ta = –40°C to +105°C)

Parameter	Pin name	Symbol	Conditions	Value			Unit
				Min.	Typ.	Max.	
Resolution	AN0 to AN23	—	—	—	10	—	bits
Monotonic increase		—	—	—	10	—	bits
Linearity error		—	—	—	—	±1	LSB
Differential linearity error		—	—	—	—	±1	LSB
Full-scale transition error		—	—	—	—	±1/2	LSB
Zero-transition error		—	—	—	—	±1/2	LSB
Total error		—	—	—	—	±2	LSB
Conversion time	—	—	CCLK = 1 MHz	—	—	50	µs
Input clock frequency	CCLK	—	—	800	1000	1200	KHz
Supply current	AV_{CC}	IA	—	—	3.0	6.0	mA
Reference voltage supply current	AVRH	IR	—	—	150	300	µA
Analog reference voltage	AVRH	—	—	0.8 AV_{CC}	—	AV_{CC}	V
	AVRL	—	—	0	—	0.2 AV_{CC}	V
Analog input voltage	AN0 to AN23	—	—	AVRL	—	AVRH	V
Multiplexer OFF-leakage current		—	—	–200	—	200	nA

- No missing code is guaranteed.

Notes:
- If the output impedance of the external input is too high, the analog voltage sampling time may be insufficient.
- In the power-on sequence, turn the power supply for the digital system first before turning that for the analog system on.

Analog input equivalent circuit



- R_{ON1} = About 1.5 kΩ
- R_{ON2} =About 1.5 kΩ
- C_0 =About 15 pF

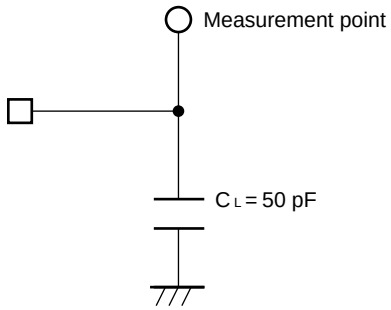
Note: The above values are reference values.

4. AC Characteristics

(AV_{CC}, V_{CC} = +3.5 V to +5.5 V ($V_{CC} \geq AV_{CC}$), V_{SS} = AGND = 0 V, Ta = –40°C to +105°C)

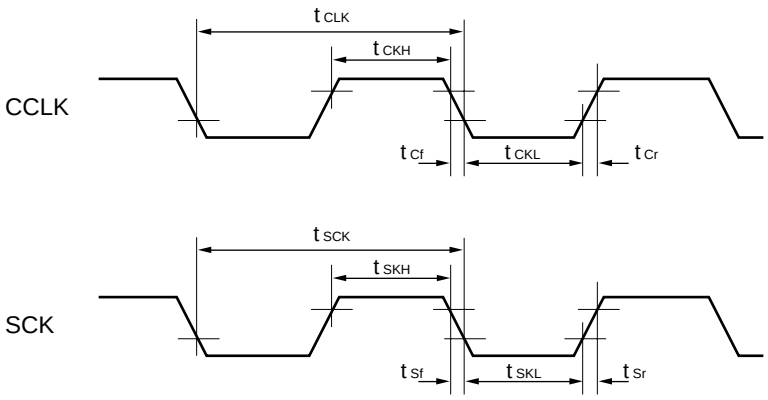
Parameter	Symbol	Conditions	Values		Unit
			Min.	Max.	
CCLK clock cycle time	f_{CLK}	$f_{CLK} = 1/f_{CLK}$	800	1200	KHz
Low-level CCLK clock pulse width	t_{CKL}	—	400	—	ns
High-level CCLK clock pulse width	t_{CKH}	—	400	—	ns
CCLK clock rise time	t_{Cr}	—	–	10	ns
CCLK clock fall time	t_{Cf}				
SCK clock cycle time	f_{SCK}	$t_{SCK} = 1/f_{SCK}$	400	1200	KHz
Low-level SCK clock pulse width	t_{SKL}	—	400	—	ns
High-level SCK clock pulse width	t_{SKH}	—	400	—	ns
SCK clock rise time	t_{Sr}	—	–	10	ns
SCK clock fall time	t_{Sf}				
SIN setup time	t_{SIS}	—	50	—	ns
SIN hold time	t_{SIH}	—	250	—	ns
Command interval	t_{COM}	CCLK = 1 MHz	4	—	µs
ENDC reset time	t_{ENR}	See “Load conditions.”	–	1	µs
RSTX pulse width	t_{RSH}	—	100	—	ns
RSTX ↑ → SCK ↓ time	t_{RSS}	—	1	—	µs
SCK ↑ → CS1 ↓ time SCK ↑ → CS2X ↑ time	t_{CSS}	—	500	—	ns
CS1 ↑ → SCK ↓ time CS2X ↓ → SCK ↓ time	t_{CSH}	—	500	—	ns
SOT output delay time (mode A)	t_{SODA}	See “Load conditions.”	—	300	ns
SOT output delay time (mode B)	t_{SODB}	See “Load conditions.”	—	300	ns
ENDC ↑ → SOT output (mode B)	t_{SOHB}	See “Load conditions.”	—	200	ns
STC command A/D conversion time	t_{STC}	CCLK = 1 MHz	—	50	µs
ATC command A/D conversion time	t_{SATC}	CCLK = 1 MHz	—	50	µs
ATGX setup time	t_{SATS}	CCLK = 1 MHz	4	—	µs
ATGX hold time	t_{SATH}	CCLK = 1 MHz	2	—	µs
Port input evaluation time	t_{POT}	CCLK = 1 MHz	—	10	µs
Port input setup time	t_{PTS}	—	0	—	ns
Port input hold time	t_{PTH}	—	0	—	ns
Extended serial HL propagation delay	t_{SHL}	See “Load conditions.”	—	100	ns
Extended serial LH propagation delay	t_{SLH}	See “Load conditions.”	—	100	ns
Noise filter width	t_{INF}	—	15	—	ns

AC Test Condition



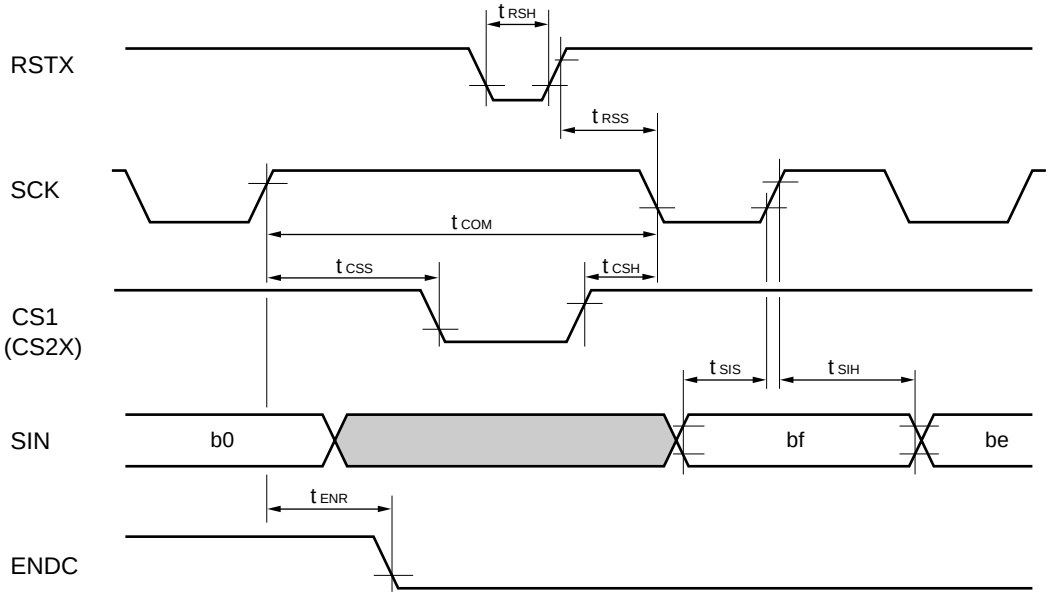
■ TIMING DIAGRAM

1. Input Clock Timing



Evaluation levels are 80% and 20% of the V_{CC}.

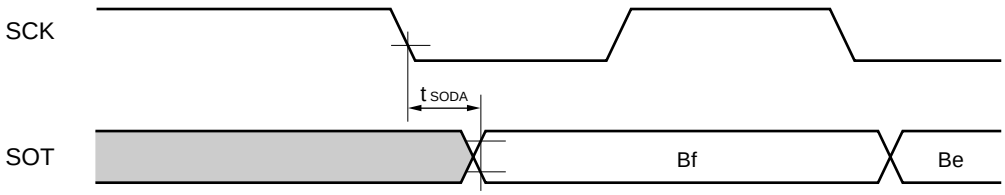
2. Serial Data Input Timing



Evaluation levels are 80% and 20% of the V_{CC}.

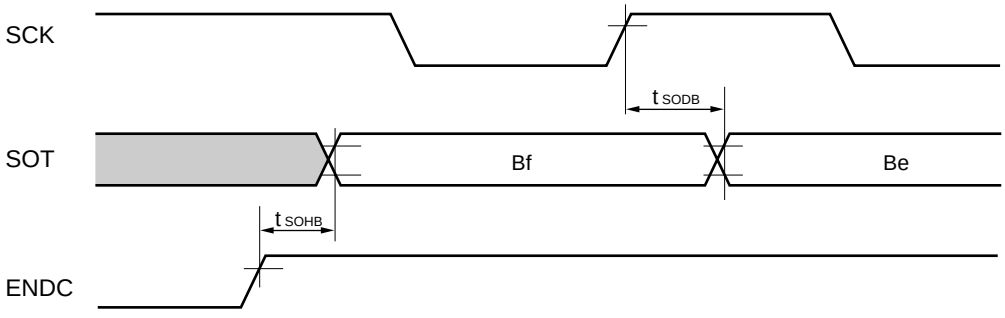
3. Serial Data Output Timing

Mode A



Evaluation levels are 80% and 20% of the V_{CC}.

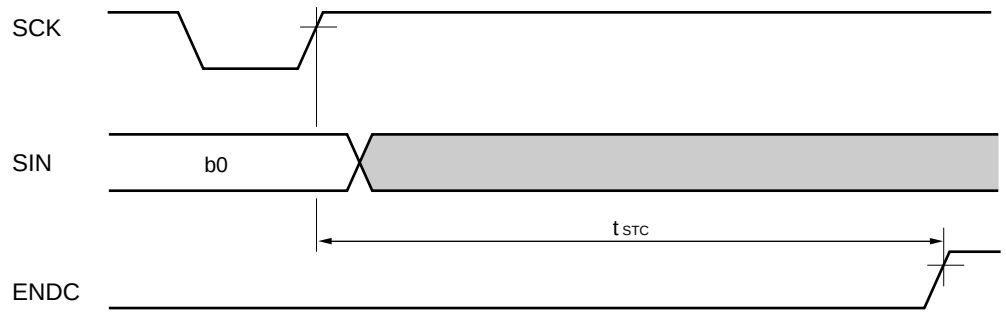
Mode B



Evaluation levels are 80% and 20% of the V_{CC}.

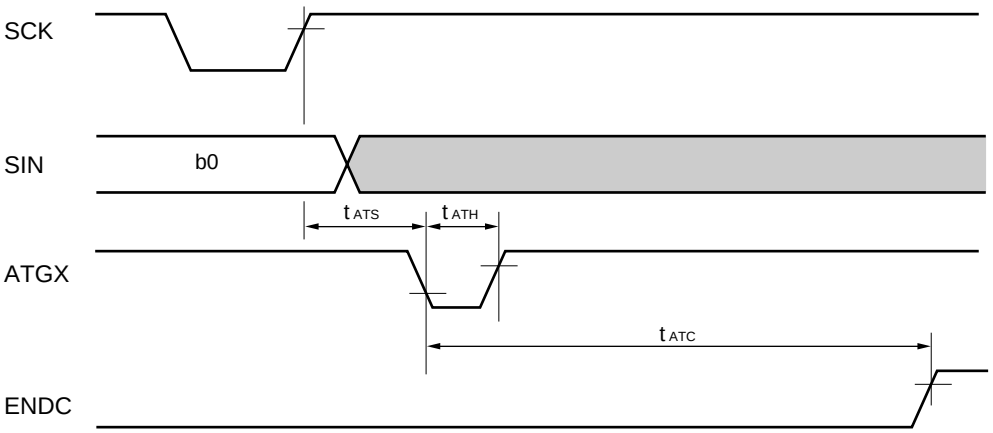
4. A/D Conversion and Port Input Evaluation

STC command (normal mode)



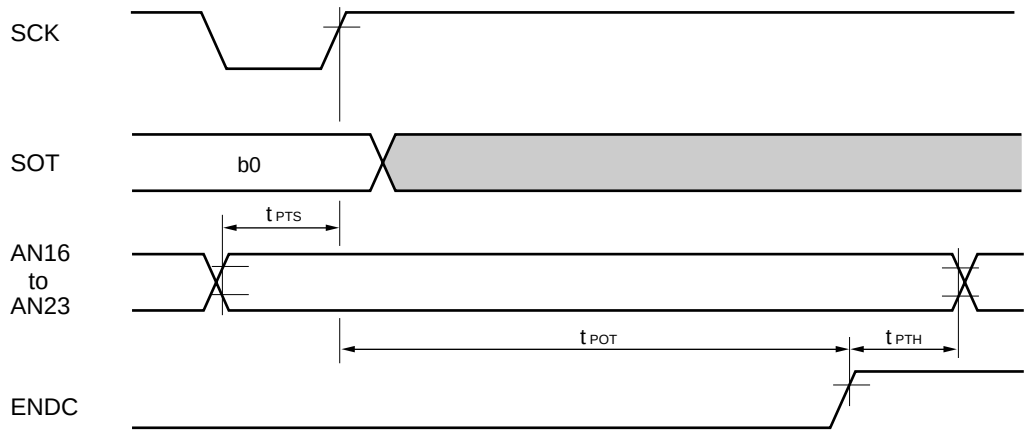
Evaluation levels are 80% and 20% of the V_{CC}.

ATC command



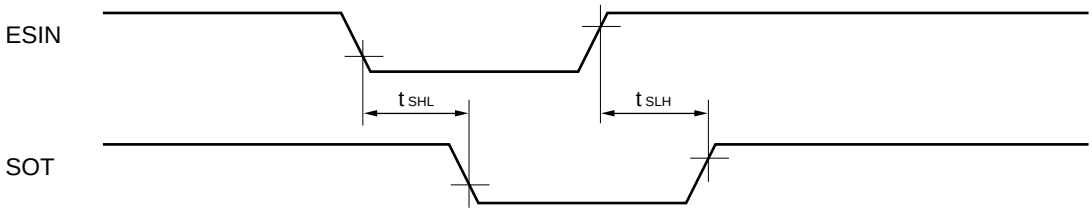
Evaluation levels are 80% and 20% of the V_{CC}.

STC command (port input mode)



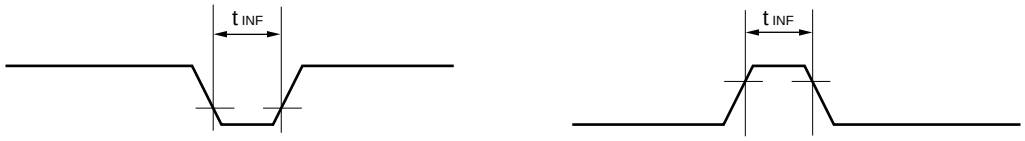
Evaluation levels are 80% and 20% of the V_{CC}.

5. Extended Serial Interface



Evaluation levels are 80% and 20% of the V_{CC}.

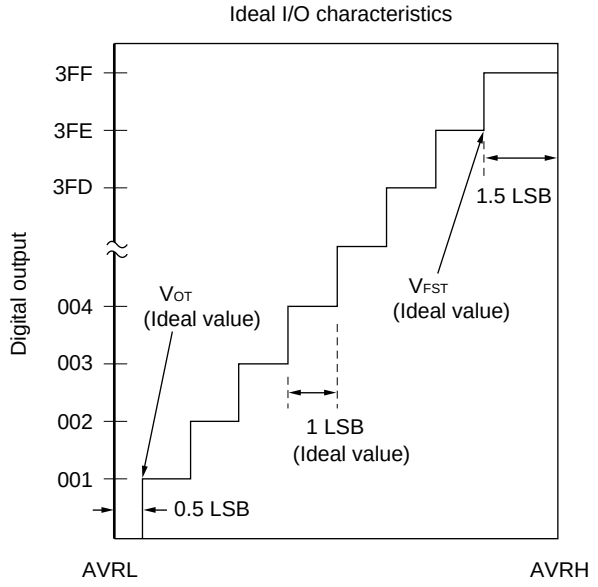
6. Noise Filter

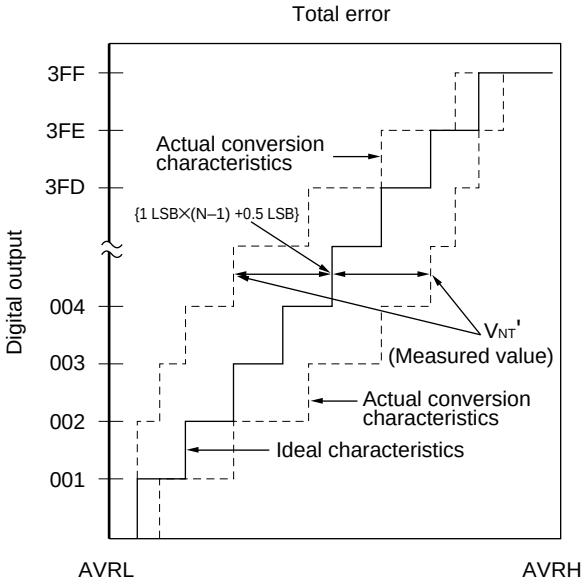


Evaluation levels are 80% and 20% of the V_{CC}.

■ DEFINITIONS OF A/D CONVERTER TERMS

- Resolution
  Analog transition identifiable by the A/D converter
- Linearity error
  Deviation of the straight line drawn between the zero transition point (00 0000 0000 ↔ 00 0000 0001) and the full-scale transition point (11 1111 1110 ↔ 11 1111 1111) of the device from actual conversion characteristics
- Differential linearity error
  Deviation from the ideal input voltage required to shift output code by one LSB
- Total error
  Difference between actual and logical values. This error is caused by a zero transition error, full-scale transition error, linearity error, quantum error, and by noise.





$$1\ \text{LSB (Ideal value)} = \frac{\text{AVRH}-\text{AVRL}}{1024}\ [\text{V}]$$

$$V_{OT}\ \text{(Ideal value)} = 0.5\ \text{LSB}\ [\text{V}]$$

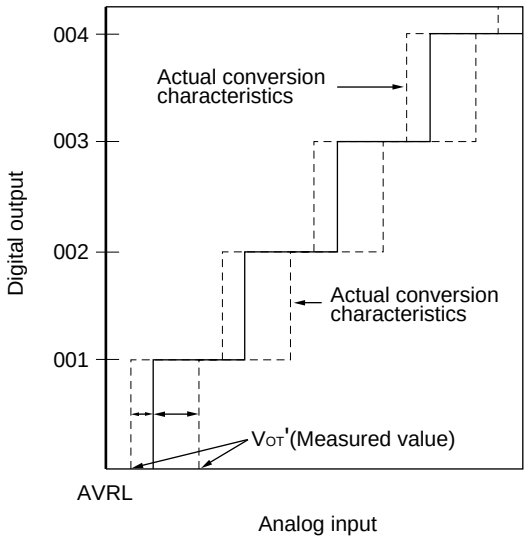
$$V_{FST}\ \text{(Ideal value)} = \text{AVRH} - 1.5\ \text{LSB}\ [\text{V}]$$

$$\text{Total error of digital output N} = \frac{V_{NT}' - \{1\ \text{LSB} \times (\text{N}-1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}$$

(Continued)

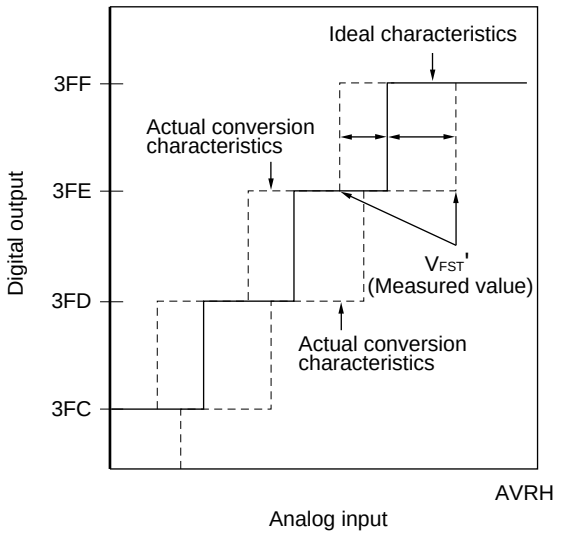
(Continued)

Zero transition error



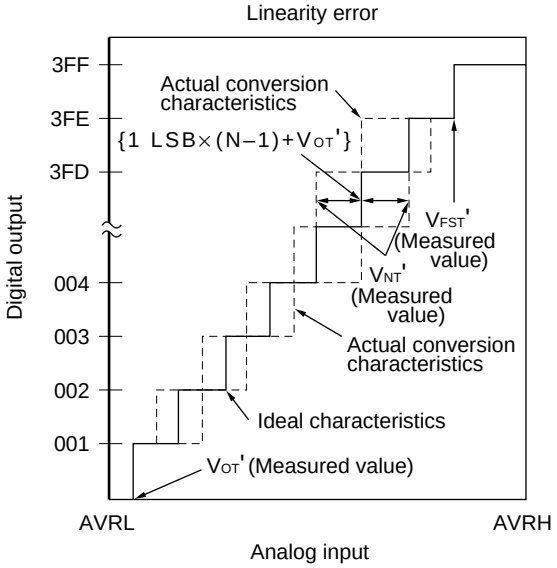
$$\text{Zero transition error} = \frac{V_{OT}' - 0.5\ \text{LSB}}{1\ \text{LSB}}$$

Full-scale transition error



$$\text{Full scale transition error} = \frac{V_{FST}' - (\text{AVRH} - 1.5\ \text{LSB})}{1\ \text{LSB}}$$

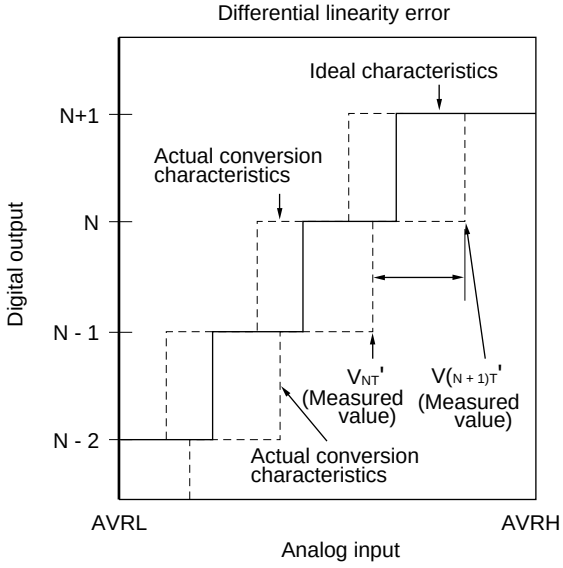
Linearity error



$$\text{Linearity error of digital output N} = \frac{V_{NT}' - \{1\ \text{LSB}' \times (N-1) + V_{OT}'\}}{1\ \text{LSB}'}$$

$$1\ \text{LSB}' = \frac{V_{FST}' - V_{OT}'}{1022}\ [V]$$

Differential linearity error



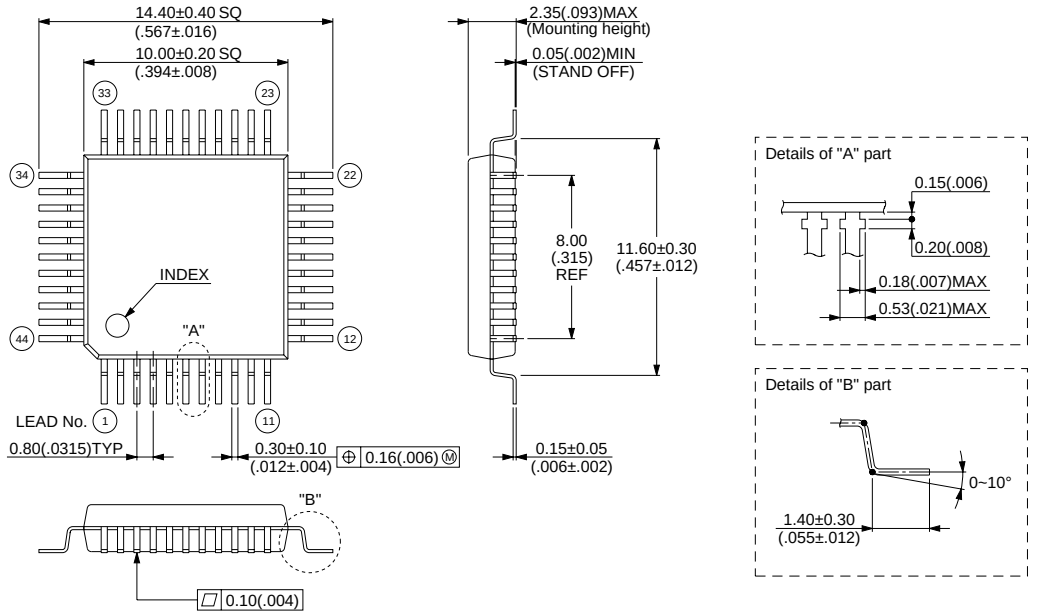
$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T}' - V_{NT}'}{1\ \text{LSB}'} - 1$$

■ ORDERING INFORMATION

Part number	Package	Remarks
MB88111PFQ	44-pin, Plastic QFP (FPT-44P-M11)	
MB88111P-SH	48-pin, Plastic SH-DIP (DIP-48P-M01)	

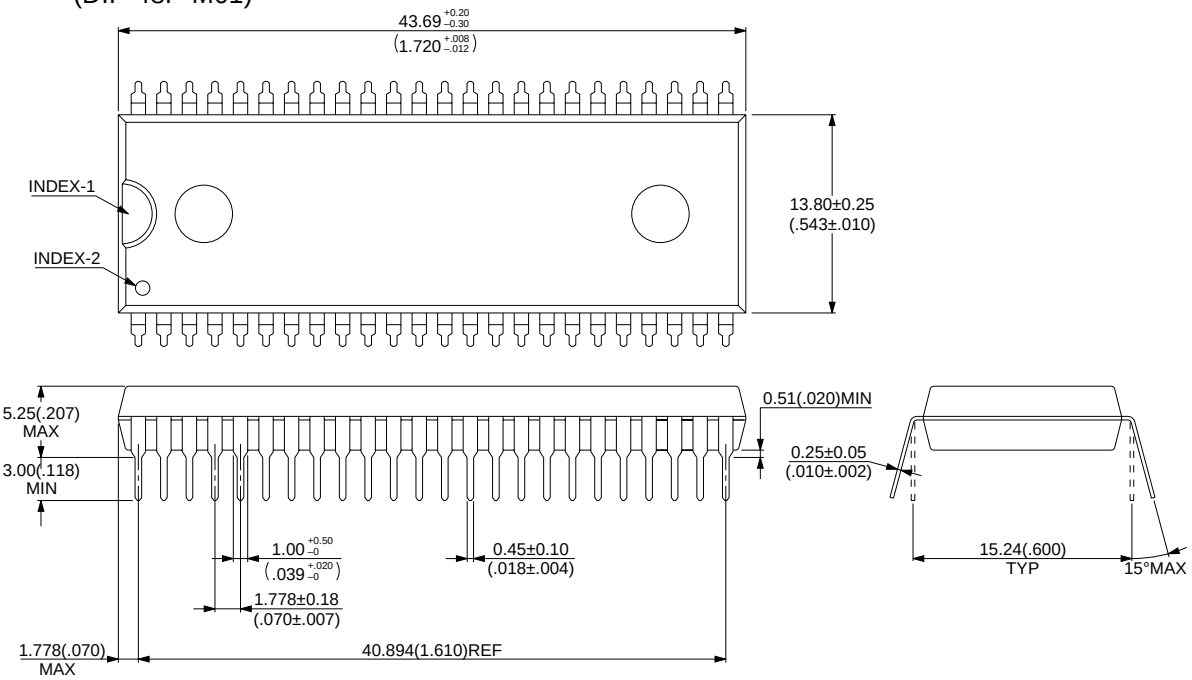
■ PACKAGE DIMENSIONS

44-pin, Plastic QFP
(FPT-44P-M11)



Dimensions in mm (inches).

48-pin, Plastic SH-DIP
(DIP-48P-M01)



Dimensions in mm (inches).

FUJITSU LIMITED

For further information please contact:

Japan
FUJITSU LIMITED
Corporate Global Business Support Division
Electronic Devices
KAWASAKI PLANT, 4-1-1, Kamikodanaka
Nakahara-ku, Kawasaki-shi
Kanagawa 211-88, Japan
Tel: (044) 754-3763
Fax: (044) 754-3329

North and South America
FUJITSU MICROELECTRONICS, INC.
Semiconductor Division
3545 North First Street
San Jose, CA 95134-1804, U.S.A.
Tel: (408) 922-9000
Fax: (408) 432-9044/9045

Europe
FUJITSU MIKROELEKTRONIK GmbH
Am Siebenstein 6-10
63303 Dreieich-Buchschlag
Germany
Tel: (06103) 690-0
Fax: (06103) 690-122

Asia Pacific
FUJITSU MICROELECTRONICS ASIA PTE. LIMITED
#05-08, 151 Lorong Chuan
New Tech Park
Singapore 556741
Tel: (65) 281-0770
Fax: (65) 281-0220

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