INTERNATIONAL CMOS
TECHNOLOGY, INC.

PEEL™153
CMOS Programmable Electrically Erasable Logic Device

Features

- **ADVANCED CMOS EEPROM TECHNOLOGY**
- **LOW POWER CONSUMPTION**
  - 35mA + 1mA/MHz max
- **COMPATIBLE PERFORMANCE**
  - t_{PD} = 30ns max, t_{OE} = 30ns max
- **EE REPROGRAMMABILITY**
  - Superior programming and functional yield
  - Low cost windowless package
  - Erases and programs in seconds
- **DEVELOPMENT SUPPORT**
  - Third-party software and programmers
  - ICT PEEL Development System and software.
- **FPLA ARCHITECTURE**
  - Programmable AND/OR arrays
  - 8 inputs and 10 I/Os
  - 42 product terms: 32 logic terms, 10 control terms
  - 10 sum terms
- **DROP-IN REPLACEMENT FOR PLS153**
  - Pin compatible
  - JEDEC file compatible
- **APPLICATION VERSATILITY**
  - Replace random SSI/MSI logic
  - Create customized comparators, multiplexers,encoders, converters, etc.

General Description

The ICT PEEL153 is a CMOS Programmable Electrically Erasable Logic device that provides a high-performance, low-power, reprogrammable, and architecturally enhanced alternative to conventional FPLAs. Designed in advanced CMOS EEPROM technology, the PEEL153 rivals speed parameters of comparable bipolar PLDs while providing a dramatic improvement in active power consumption. The EE-reprogammability of the PEEL153 reduces development and field retrofit costs and enhances testability to ensure 100% field programmability and function. PEEL technology allows for low cost "windowless" packaging in a ceramic or plastic 20-pin, 300-mil DIP.

The PEEL153 provides both a programmable AND array and a programmable OR array to offer drop-in compatibility with the bipolar PLS153. Applications for the PEEL153 cover a wide range of combinatorial functions, such as: replacement of random SSI/MSI logic circuitry, priority encoders, comparators, parity generators, code converters, address decoders, and multiplexers. The PEEL153 is supported by popular development tools and programmers from third-party manufacturers and by ICT's PEEL Development System and APEEL Logic Assembler.

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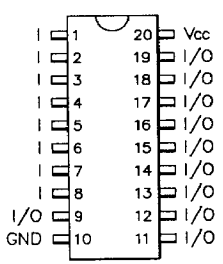
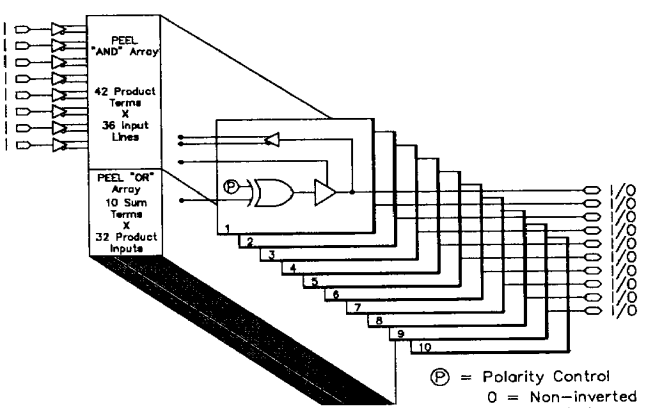
Pin Configuration



Pin Names
I = Dedicated Input
I/O = Bidirectional I/O
GND = Ground
Vcc = Power Supply (5V)

Block Diagram



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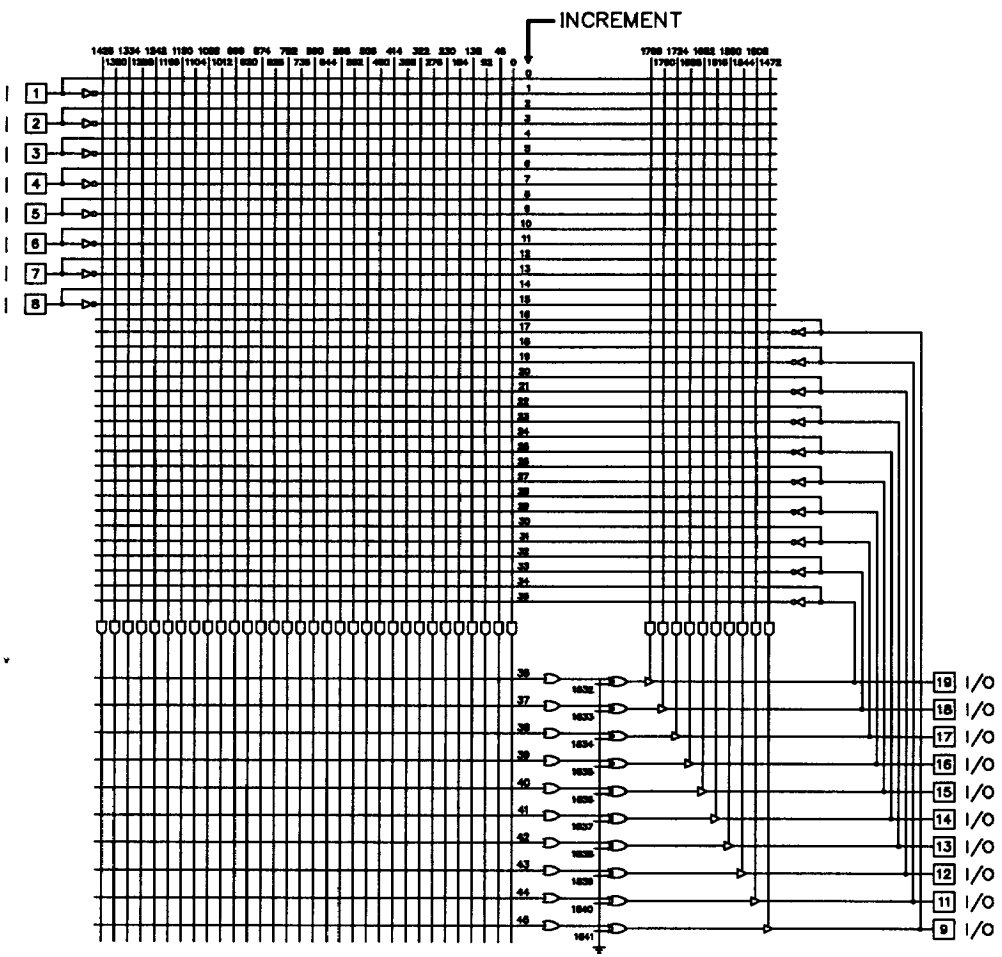
JEDEC Programming Cell Number = Product Term Number + Increment



PEEL153 Logic Array Diagram

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Absolute Maximum Ratings

Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Supply Voltage	Relative to GND	− 0.6 to +7.0	V
V_{IO}	Voltage Applied to Any Pin [8]	Relative to GND [1]	− 0.6 to V_{CC} + 0.6	V
T_A	Ambient Temp, Power Applied		− 10 to + 85	°C
T_{ST}	Storage Temperature		− 65 to + 150	°C
T_{LT}	Lead Temperature	Soldering 10 seconds	+ 300	°C

Operating Ranges

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage	Commercial	4.75	5.25	V
T_A	Ambient Temperature	Commercial	0	70	°C

D.C. Electrical Characteristics

Over the operating range

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input HIGH Level		2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Level		− 0.3	0.8	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = − 3.2mA	2.4		V
V_{OHC}	Output HIGH Voltage CMOS	V_{CC} = Min, I_{OH} = − 10µA	V_{CC} − 0.1		V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 8mA [4]		0.5	V
V_{OLC}	Output LOW Voltage CMOS	V_{CC} = Min, I_{OL} = 10µA		0.1	V
I_L	Input Leakage Current	V_{CC} = Max, GND ≤ V_I ≤ V_{CC}		10	µA
I_{OS}	Output Short Circuit Current [2]	V_{CC} = Max, V_O=GND	− 30	− 90	mA
I_{OZ}	Output Leakage Current	I/O = High Impedence V_{CC} = Max, GND ≤ V_O ≤ V_{CC}		± 10	µA
I_{CCSC}	Power Supply Current, Standby, CMOS Interface	All inputs = GND or V_{CC} [3]		35	mA
I_{CCAC}	Power Supply Current, Active, CMOS Interface	V_{IN} = V_{IL} or V_{IH}. All inputs, feedback, and I/Os switching [3]		I_{CCSC} + 1mA/MHz	mA
I_{CCST}	Power Supply Current Standby, TTL Interface	V_{IN} = V_{IL} or V_{IH} [3]		45	mA
I_{CCAT}	Power Supply Current, Active, TTL Interface	V_{IN} = V_{IL} or V_{IH}. All inputs, feedback, and I/Os switching [3]		I_{CCST} + 1mA/MHz	mA

Capacitance

These measurements are periodically sample tested..

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C V_{CC} = 5.0V, f = 1kHz		6	pF
C_{OUT}	Output Capacitance			12	pF

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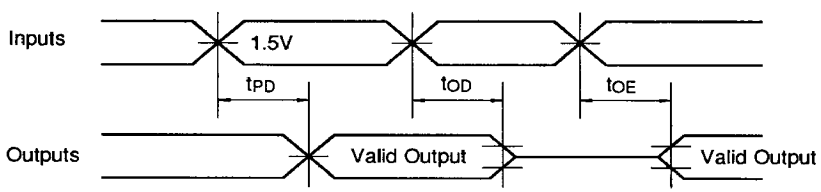
A.C. Electrical Characteristics

Over the Operating Range [5,9]

Symbol	Parameter	PEEL153-30		PEEL153-35		PEEL153-40		Unit
		Min	Max	Min	Max	Min	Max	
t_{PD}	Propagation Delay, Input to Output		30		35		40	ns
t_{OE}	Input toOutput Enable [6]		30		35		40	ns
t_{OD}	Input to Output Disable [6,7]		30		35		40	ns

Switching Waveforms



Notes:

1. Minimum DC input is – 0.5V, however, inputs may undershoot to – 2.0V for periods less than 30ns.
2. Test one ouput at a time. Duration of short circuit should not exceed 1 second.
3. All I/O pins open (no load).
4. Assumes worst-case conditions - all outputs loaded. V_{OL} = 0.5V @ I_{OL} = 15mA with one output loaded.
5. Test conditions assume: signal transitions of 5ns or less fron the 10% and 90% points; timing reference levels of 1.5V (unless otherwise specified);and test loads shown.
6. t_{OE} is measured from input transition to $V_{REF} \pm 0.1V$. t_{OD} is measured from input transition to $V_{OH} - 0.1V$ or $V_{OL} + 0.1V$.
7. C_L includes scope and jig capacitance. t_{OD} is measured with C_L = 5pF
8. V_{IO} specified is not for program/verify operation. Contact ICT for information regarding PEEL153 program/verify specifications
9. PEEL Deivce test leads are specified at the end of this section.

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