

BIDIRECTIONAL LOW CAPACITANCE TVS ARRAYS
APPLICATIONS

- ✓ Ethernet - 10/100 Base T
- ✓ FireWire
- ✓ SCSI
- ✓ Bluetooth & RF

IEC COMPATIBILITY (EN61000-4)

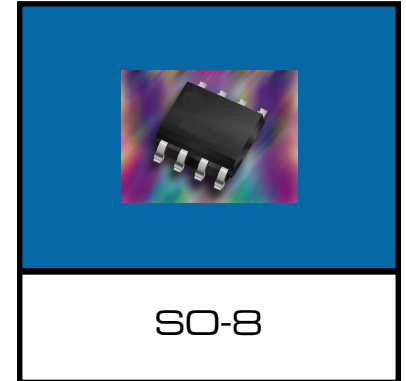
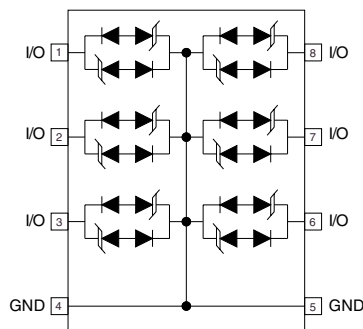
- ✓ 61000-4-2 (ESD): Air - 15kv, Contact - 8kv
- ✓ 61000-4-4 (EFT): 40A - 5/50ns
- ✓ 61000-4-5 (Surge): 24A, 8/20 μ s - Level 2(Line-Gnd) & Level 3(Line-Line)

FEATURES

- ✓ 500 Watts Peak Pulse Power Dissipation($t_p = 8/20\mu$ s)
- ✓ Bidirectional Configuration
- ✓ Available in 4 Voltage Types: 3.3V to 15V
- ✓ Protects Up to Six (6) Lines
- ✓ ESD Protection > 40 kilovolts
- ✓ **LOW CAPACITANCE -8pF**

MECHANICAL CHARACTERISTICS

- ✓ Molded JEDEC SO-8
- ✓ Weight 15 milligrams (Approximate)
- ✓ Flammability Rating UL 94V-0
- ✓ 12mm Tape and Reel Per EIA Standard 481-1-A
- ✓ Device Marking Code & Logo
- ✓ Pin 1 Indicated By Dot on Package


CIRCUIT DIAGRAM


PLCDA03C-6 thru PLCDA15C-6

DEVICE CHARACTERISTICS

MAXIMUM RATINGS @ 25°C Unless Otherwise Specified

PARAMETER	SYMBOL	VALUE	UNITS
Operating Temperature	T_J	-55°C to 150°C	°C
Storage Temperature	T_{STG}	-55°C to 150°C	°C

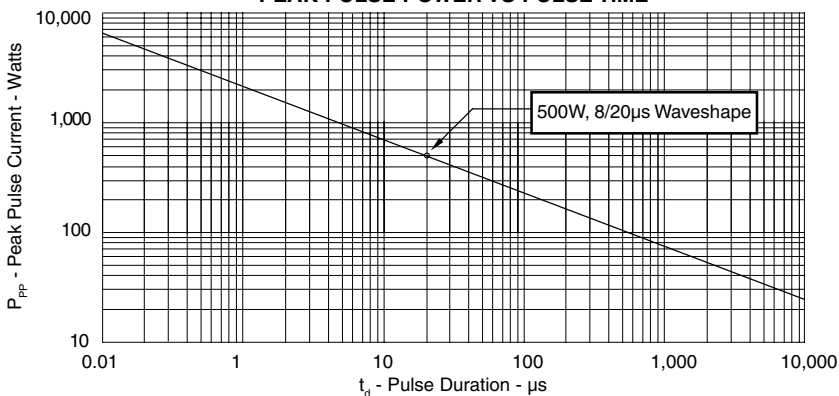
ELECTRICAL CHARACTERISTICS PER LINE @ 25°C Unless Otherwise Specified

PART NUMBER (See Note 1)	DEVICE MARKING	RATED STAND-OFF VOLTAGE V_{WM} VOLTS	MINIMUM BREAKDOWN VOLTAGE @ 1mA $V_{(BR)}$ VOLTS	MAXIMUM CLAMPING VOLTAGE (See Fig. 2) @ $I_P = 1A$ V_C VOLTS	MAXIMUM CLAMPING VOLTAGE (See Fig. 2) @ 8/20 μ s $V_C @ I_{PP}$	MAXIMUM LEAKAGE CURRENT @ V_{WM} I_D μA	TYPICAL CAPACITANCE (See Note 2) 0V @ 1 MHz C pF
PLCDA03C-6	PRS	3.3	4.5	7.0	10.9V @ 43.0A	125	8
PLCDA05C-6	PRT	5.0	6.0	9.8	13.5V @ 42.0A	20	8
PLCDA08C-6	PRW	8.0	8.5	13.4	16.9V @ 34.0A	10	8
PLCDA15C-6	PRU	15.0	16.7	22.0	30.0V @ 17.0A	2	8

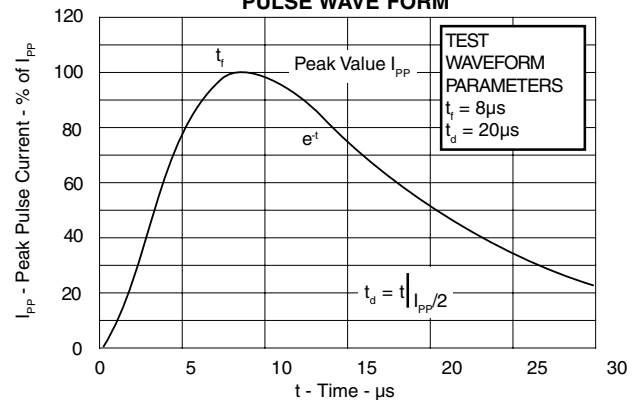
Note 1: Spice model and parameters for this series are available on the ProTek Devices web site: www.protekdevices.com.

Note 2: Capacitance between I/O pins and ground (pins 4 & 5) is typically 8pF. Capacitance between I/O pins is typically 4 pF.

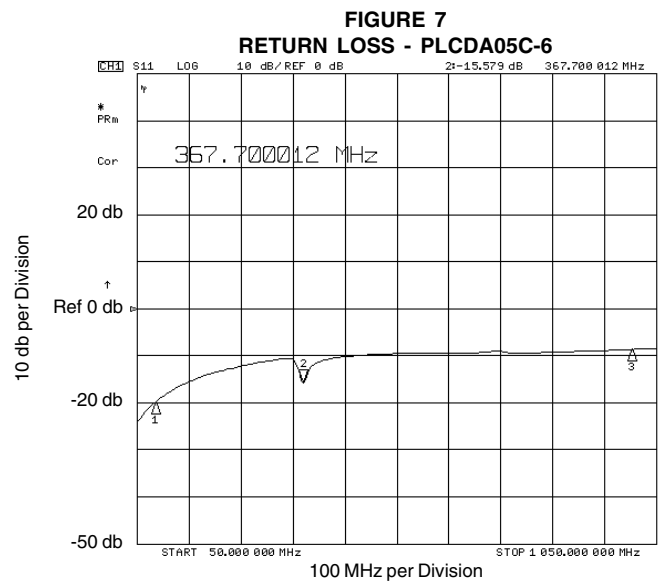
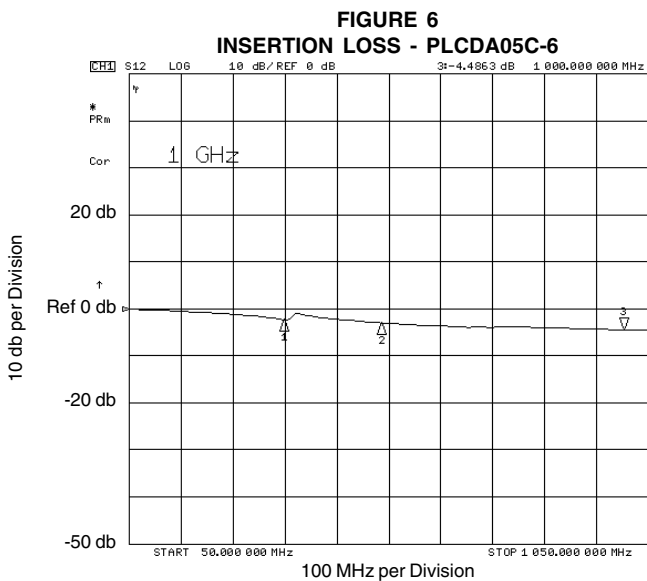
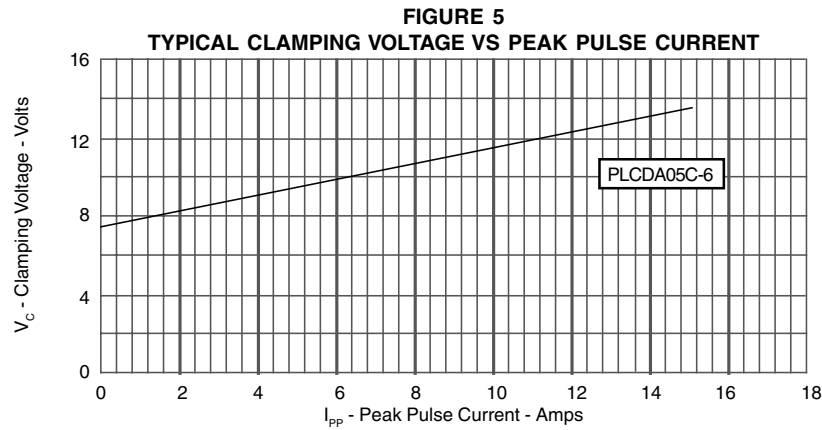
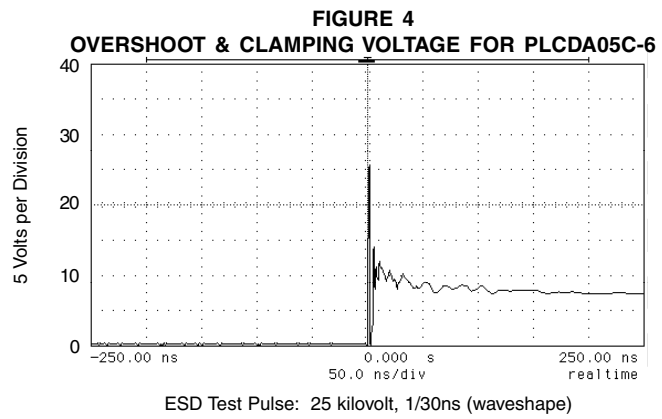
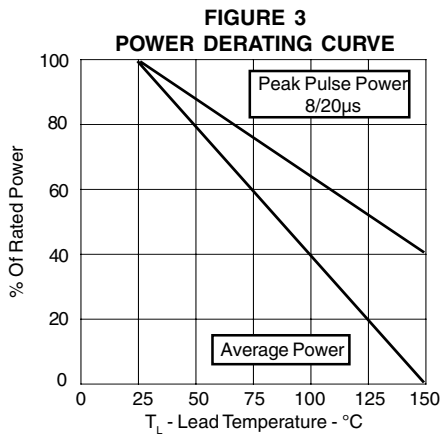
**FIGURE 1
PEAK PULSE POWER VS PULSE TIME**



**FIGURE 2
PULSE WAVE FORM**



GRAPHS



APPLICATION NOTE

The PLCDAxxC-6 Series are low capacitance, bidirectional TVS arrays that are designed to protect I/O or high speed data lines from the damaging effects of ESD or EFT. This product series has a surge capability of 500 Watts P_{pp} per line for an 8/20 μ s waveshape and offers ESD protection > 40kv.

BIDIRECTIONAL COMMON MODE CONFIGURATION (Figure 1)

Ideal for use multimode transceiver I/O lines, the PLCDAxxC-6 Series provides up to six (6) lines of protection in a common mode configuration as depicted in Figure 1.

Circuit connectivity is as follows:

- ✓ Line 1 is connected to Pin 1.
- ✓ Line 2 is connected to Pin 2.
- ✓ Line 3 is connected to Pin 3.
- ✓ Line 4 is connected to Pin 8.
- ✓ Line 5 is connected to Pin 7.
- ✓ Line 6 is connected to Pin 6.
- ✓ Pins 4 and 5 are connected to Ground.

BIDIRECTIONAL COMMON MODE CONFIGURATION (Figure 2)

The PLCDAxxC-6 Series also provides video line applications six (6) lines of protection in a common mode configuration as depicted in Figure 2.

Circuit connectivity is as follows:

- ✓ Line 1 (Red) is connected to Pin 1.
- ✓ Line 2 (Green) is connected to Pin 2.
- ✓ Line 3 (Blue) is connected to Pin 3.
- ✓ Line 4 (VSYNC) is connected to Pin 6.
- ✓ Line 5 (HSYNC) is connected to Pin 7.
- ✓ Pins 4 and 5 are connected to Ground.

CIRCUIT BOARD LAYOUT RECOMMENDATIONS

Circuit board layout is critical for Electromagnetic Compatibility (EMC) protection. The following guidelines are recommended:

- ✓ The protection device should be placed near the input terminals or connectors, the device will divert the transient current immediately before it can be coupled into the nearby traces.
- ✓ The path length between the TVS device and the protected line should be minimized.
- ✓ All conductive loops including power and ground loops should be minimized.
- ✓ The transient current return path to ground should be kept as short as possible to reduce parasitic inductance.
- ✓ Ground planes should be used whenever possible. For multilayer PCBs, use ground vias.

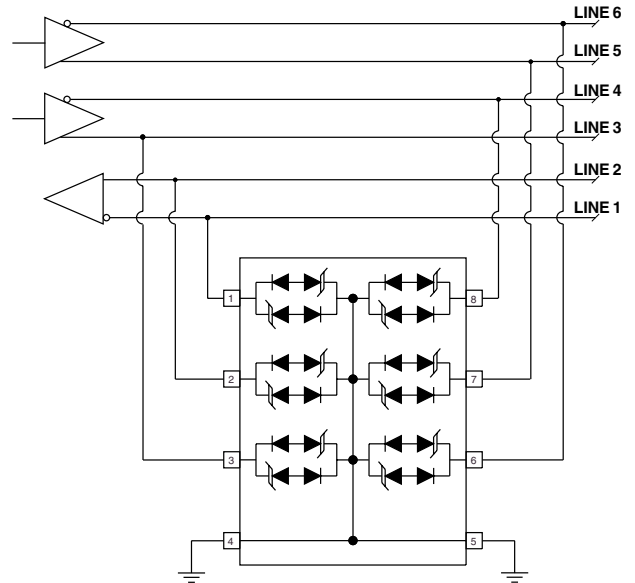


Figure 1: Typical Transceiver Protection Circuit

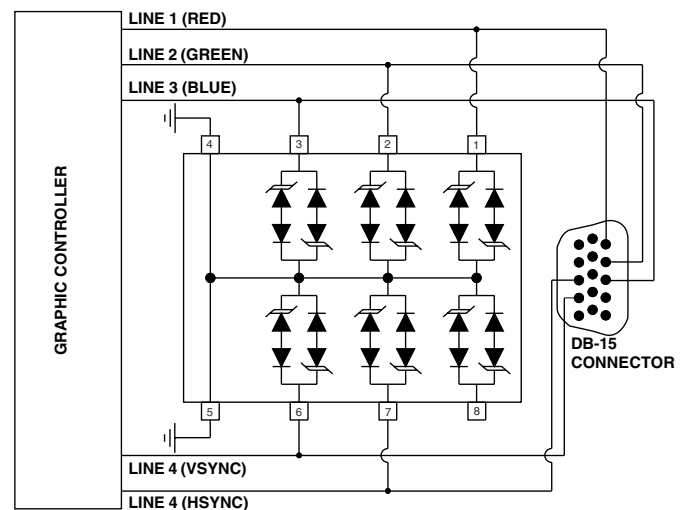


Figure 2: Typical Video Line Protection Circuit

PLCDA03C-6 thru PLCDA15C-6

PACKAGE OUTLINE & DIMENSIONS

PACKAGE OUTLINE

SO-8

PACKAGED DIMENSIONS

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.196
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.250	0.016	0.049
G	1.27 BSC	1.27 BSC	0.05 BSC	0.05 BSC
J	0.18	0.25	0.007	0.009
K	0.10	0.25	0.004	0.008
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

NOTES:

- T - = Seating Plane and Datum Surface.
- Dimensions "A" and "B" are Datum.
- Dimensions "A" and "B" do not include mold protrusion.
- Maximum mold protrusion is 0.015" (0.380 mm) per side.
- Dimensioning and tolerances per ANSI Y14.5M, 1982.
- Dimensions are exclusive of mold flash and metal burrs.

06009 Rev 1 -11/01

MOUNTING PAD

TAPE & REEL PACKAGING:

Surface mount product is taped and reeled in accordance with EIA-481, reel quantities and sizes are as follows:

7 Inch Reel - 1,000 pieces per reel; 13 Inch Reel - 2,500 pieces per reel

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