3.3V 8BIT 3MSPS DAC BW1245X

GENERAL DESCRIPTION

The BW1245X is a CMOS 8-bit D/A converter for general applications. It consists of a 1-of-256 decoder, a resistor string with 256 resistors and an OP amp block.
The maximum conversion rate of BW1245X is 3MSPS and supply voltage is 3.3V single.

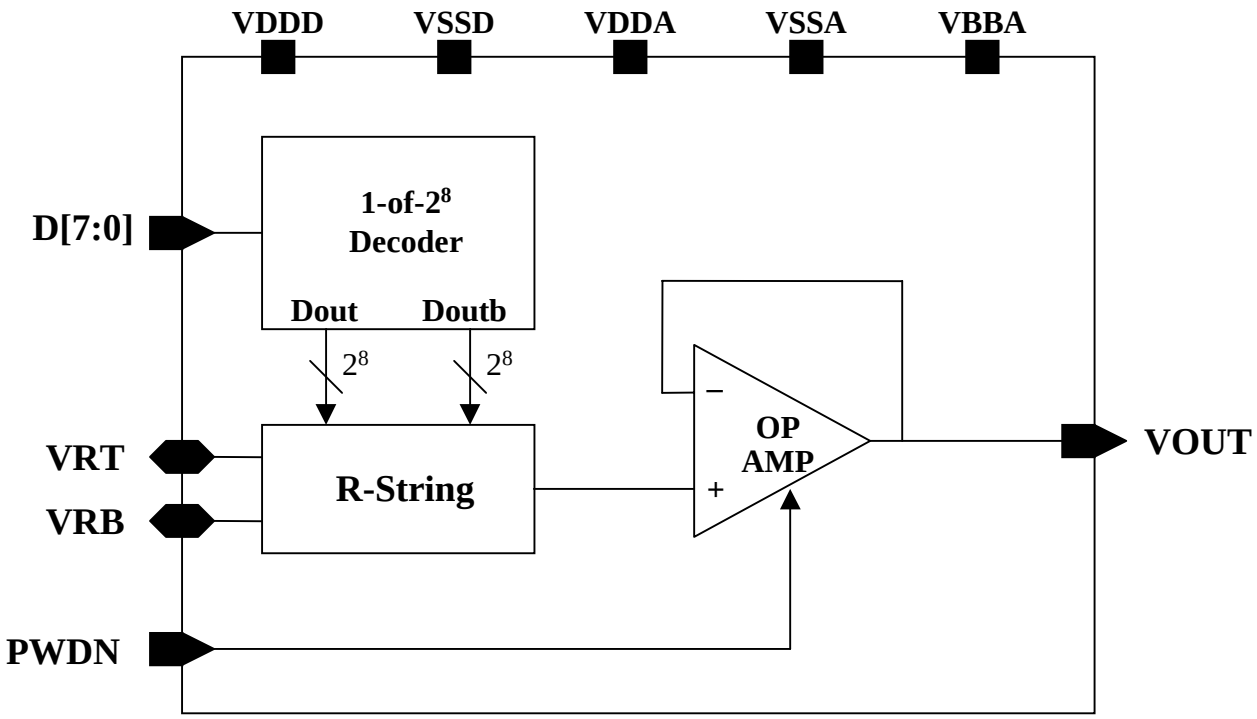
TYPICAL APPLICATIONS

- Hard Disk Drive (HDD)
- Battery Operated Instruments
- Motor Control Systems
- General Applications

FEATURES

- **Resolution : 8Bit**
- **Differential Linearity Error : ± 0.5 LSB**
- **Integral Linearity Error : ± 1.0 LSB**
- **Maximum Conversion Rate : 3MSPS**
- **Low Power Consumption : 9.9mW**
- **Power Down Mode**
- **Operation Temperature Range : 0° C ~ 70° C**
- **Power Supply : 3.3V Single**

FUNCTIONAL BLOCK DIAGRAM



Ver 1.8 (April 2002)
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CORE PIN DESCRIPTION

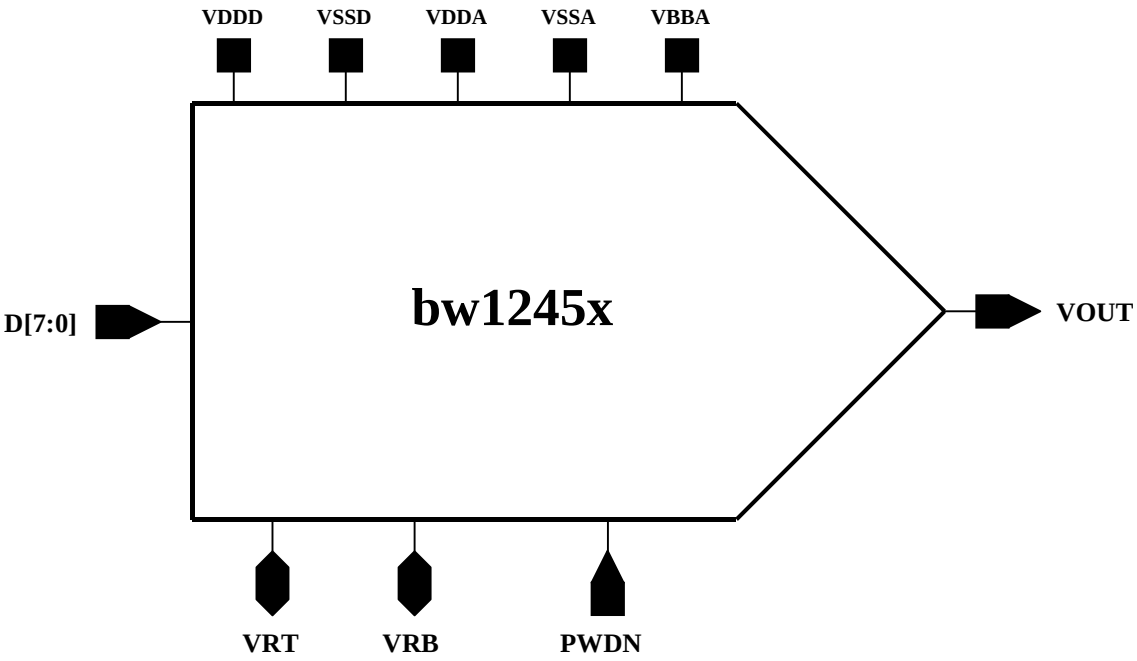
NAME	I/O TYPE	I/O PAD	PIN DESCRIPTION
D[7:0]	DI	picc_bb	Digital Input Data (8BIT) D[7] : MSB , D[0] : LSB
PWDN	DI	picc_bb	Power Down (Active Low)
VRT	AB	pia_bb	Voltage Reference Top
VRB	AB	pia_bb	Voltage Reference Bottom
VOUT	AO	poa_bb	Analog Voltage Output
VDDD	DP	vddd	Digital Power (+3.3V)
VSSA	DG	vssd	Digital Ground (0.0V)
VDDA	AP	vdda	Analog Power (+3.3V)
VSSA	AG	vssa	Analog Ground (0.0V)
VBBA	AG	vbba	Analog Sub Bias (0.0V)

I/O TYPE ABBR.

- AI : Analog Input
- DI : Digital Input
- AO : Analog Output
- DO : Digital Output
- AB : Analog Bidirectional
- DB : Digital Bidirectional

- AP : Analog Power
- DP : Digital Power
- AG : Analog Ground
- DG : Digital Ground

CORE CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Supply Voltage	VDD (VDDA,VDDD)	4.5	V
Analog Output Voltage	VOUT	VSS to VDD	V
Digital Input Voltage	D[7:0]	VSS to VDD	V
Reference Voltage	VRT VRB	VDD VSS	V
Operating Temperature Range	Topr	0 to 70	°C

NOTES :

1. ABSOLUTE MAXIMUM RATING specifies the values beyond which the device may be damaged permanently. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect reliability. Each condition value is applied with the other values kept within the following operating conditions and function operation under any of these conditions is not implied.
2. All voltages are measured with respect to VSS(VSSA or VSSD or VBBA) unless otherwise specified.
3. 100pF capacitor is discharged through a 1.5kΩ resistor (Human body model)

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Supply Voltage	VDDA - VSSA VDDD - VSSD	3.15	3.3	3.45	V
Supply Voltage Difference	VDDA - VDDD	-0.1	0.0	0.1	V
Reference Voltage	VRT VRB	- 0.0	- -	3.3 -	V
Digital Input 'Low' Voltage Digital Input 'High' Voltage	VIL VIH	- 0.7×VDD	- -	0.3×VDD -	V
Operating Temperature	Topr	0	-	70	°C

NOTE :

It is strongly recommended that to avoid power latch-up all the supply pins(VDDA,VDDD) be driven from the same source.

DC ELECTRICAL CHARACTERISTICS

(Converter Specifications : VDDA=VDDD=3.3V, VSSA=VSSD=VBBA=0V,
PWDN=High, Top=25°C, VRT=3.3V, VRB=0.0V unless otherwise specified.)

Characteristics	Symbol	Min	Typ	Max	Unit	Conditions
Resolution	Bit	-	-	8	Bits	-
Differential Linearity Error	DLE	-	0.3	0.5	LSB	-
Integral Linearity Error	ILE	-	0.5	1.0	LSB	-
Zero Scale Error[1]	V_{ZSE}	-	10	18	mV	VRT=3.3V , VRB=0.0V
Full Scale Voltage Error[2]	V_{FSE}	-	4	23	mV	
Maximum Output Voltage	Vo_{MAX}	3.245	3.281	3.287	V	Vo_{MAX} = VOUT(D[7:0]=High)
LSB Size	V_{LSB}	12.73	12.86	12.89	mV	V_{LSB} = Vo_{MAX} / 255

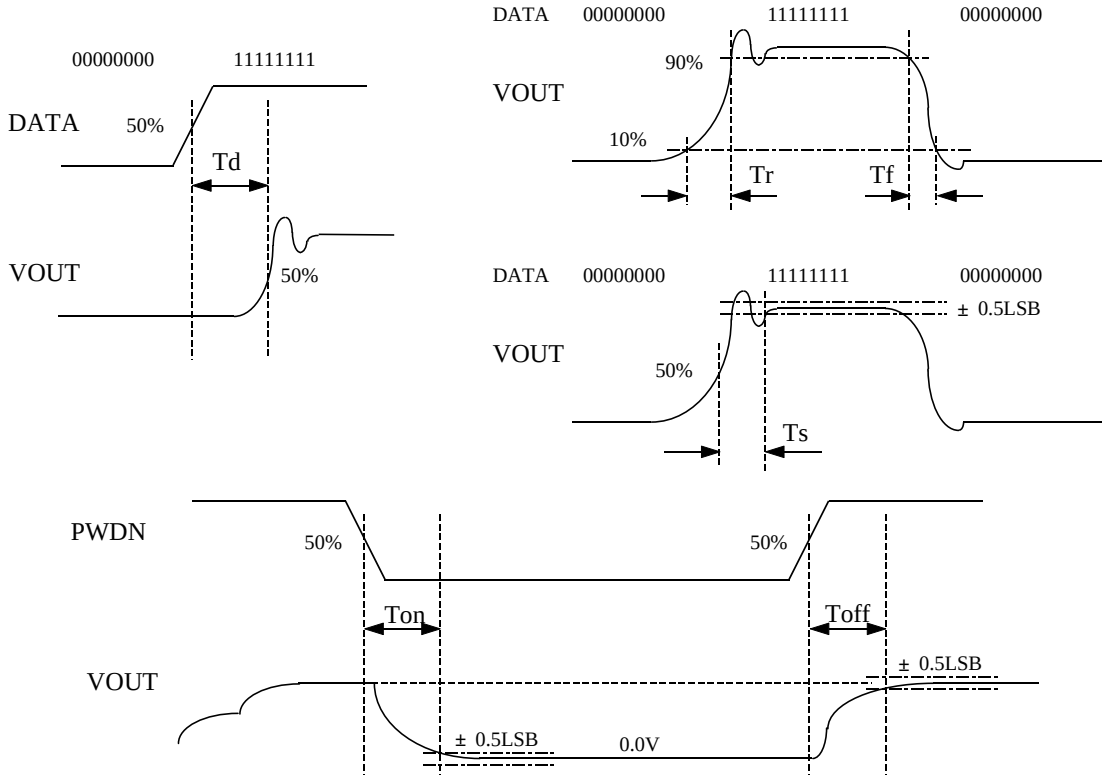
NOTE 1 : V_{ZSE}=VOUT(D[7:0]=Low) - VRB
2 : V_{FSE}=VOUT(D[7:0]=High) - {(VRT-VRB) × 255/256 + VRB}

AC ELECTRICAL CHARACTERISTICS

(Converter Specifications : VDDA=VDDD=3.3V, VSSA=VSSD=VBBA=0V, load cap=25pF
Top=25°C, VRT=3.3V, VRB=0.0V unless otherwise specified.)

Characteristics	Symbol	Min	Typ	Max	Unit	Conditions
Maximum Conversion Rate	f_C	-	-	3	MSPS	Data Rate = 3MHz
Dynamic Supply Current	Ivdd1	-	3	-	mA	Ivdd1 = I_{VDDA} + I_{VRT} + I_{VDDD} Data Rate = 3MHz
Dynamic Supply Current (Power Down Mode)	Ivdd2	-	-	10	uA	Ivdd2 = I_{VDDA} + I_{VDDD} Data Rate = 3MHz PWDN=LOW
Analog Output Delay	Td	75	82	87	ns	Data Rate = 3MHz Data : All LOW → All HIGH
Analog Output Rise Time	Tr	95	102	110	ns	Data Rate = 3MHz Data : All LOW → All HIGH
Analog Output Fall Time	Tf	88	94	100	ns	Data Rate = 3MHz Data : All HIGH → All LOW
Analog Output Settling Time	Ts	160	232	330	ns	Data Rate = 3MHz Data : All LOW → All HIGH VRT = VDD/2
Power Down On Time	Ton	50	52	60	ns	PWDN : HIGH → LOW
Power Down Off Time	Toff	150	160	170	ns	PWDN : LOW → HIGH

TIMING DIAGRAM



1. Output delay measured from the 50% point of the rising edge of input data to the full scale transition.
2. Settling time measured from the 50% point of full scale transition to the output remaining within ±1/2 LSB.
3. Output rise/fall time measured between the 10% and 90% points of full scale transition.

FUNCTIONAL DESCRIPTION

1. The bw1245x has a 1-of-256 decoder, a R-String Block for 8bit and an OP amp block for driving output.

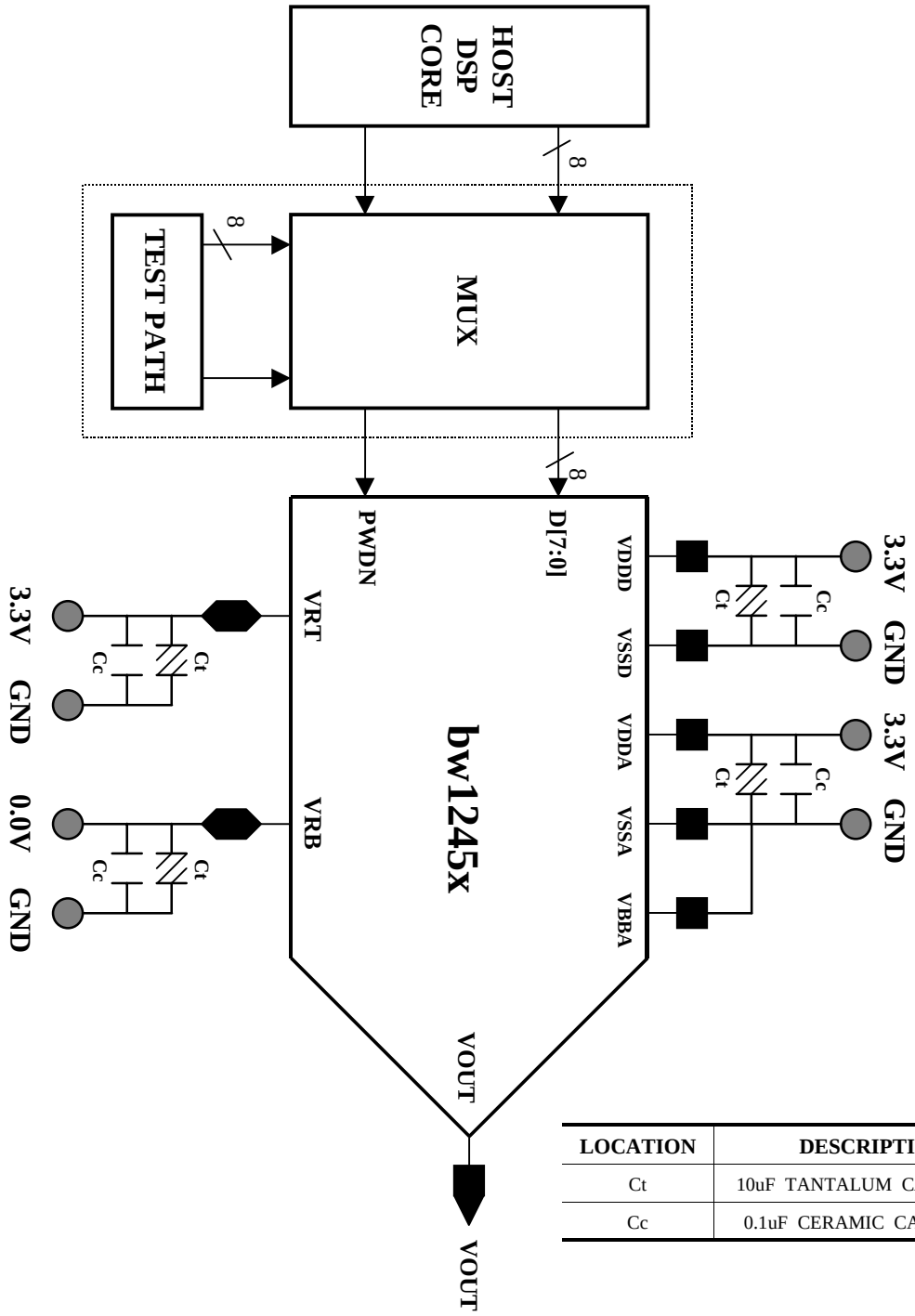
2. The decoder has 256 digital outputs and only one of them is valid.
   The R-string block consists of R-array with 256 resistors and 256 CMOS switches and decides to output voltage according to 256 digital inputs generated by 1-of-256 decoder.

3. $$V_{Rstring} = \frac{VRT - VRB}{2^8} \sum_{n=0}^{7} (2^n * Dn) + VRB$$

4. The output of the R-string block is driven by OP amp.

5. In power down mode, only analog current (I_{VDDA}) is reduced.

CORE EVALUATION GUIDE

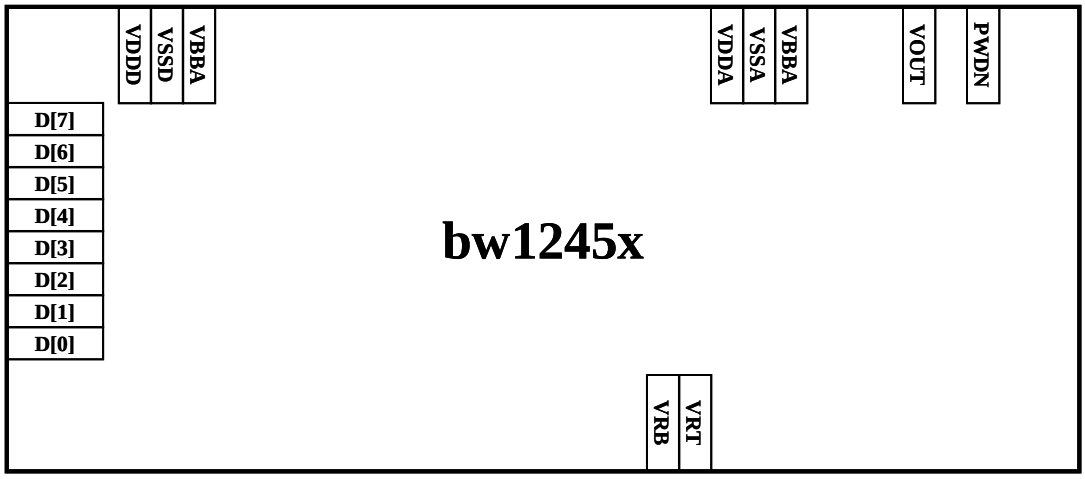


LOCATION	DESCRIPTION
Ct	10uF TANTALUM CAPACITOR
Cc	0.1uF CERAMIC CAPACITOR

TESTABILITY

Whether you use MUX or the internal logic for testability, it is required to be able to select the values of digital inputs (D[7:0]).
See above figure. Only if it is, you can check the main function. (Linearity)
Normal Test Condition : VRT=3.3V , VRB=0.0V , PWDN=High

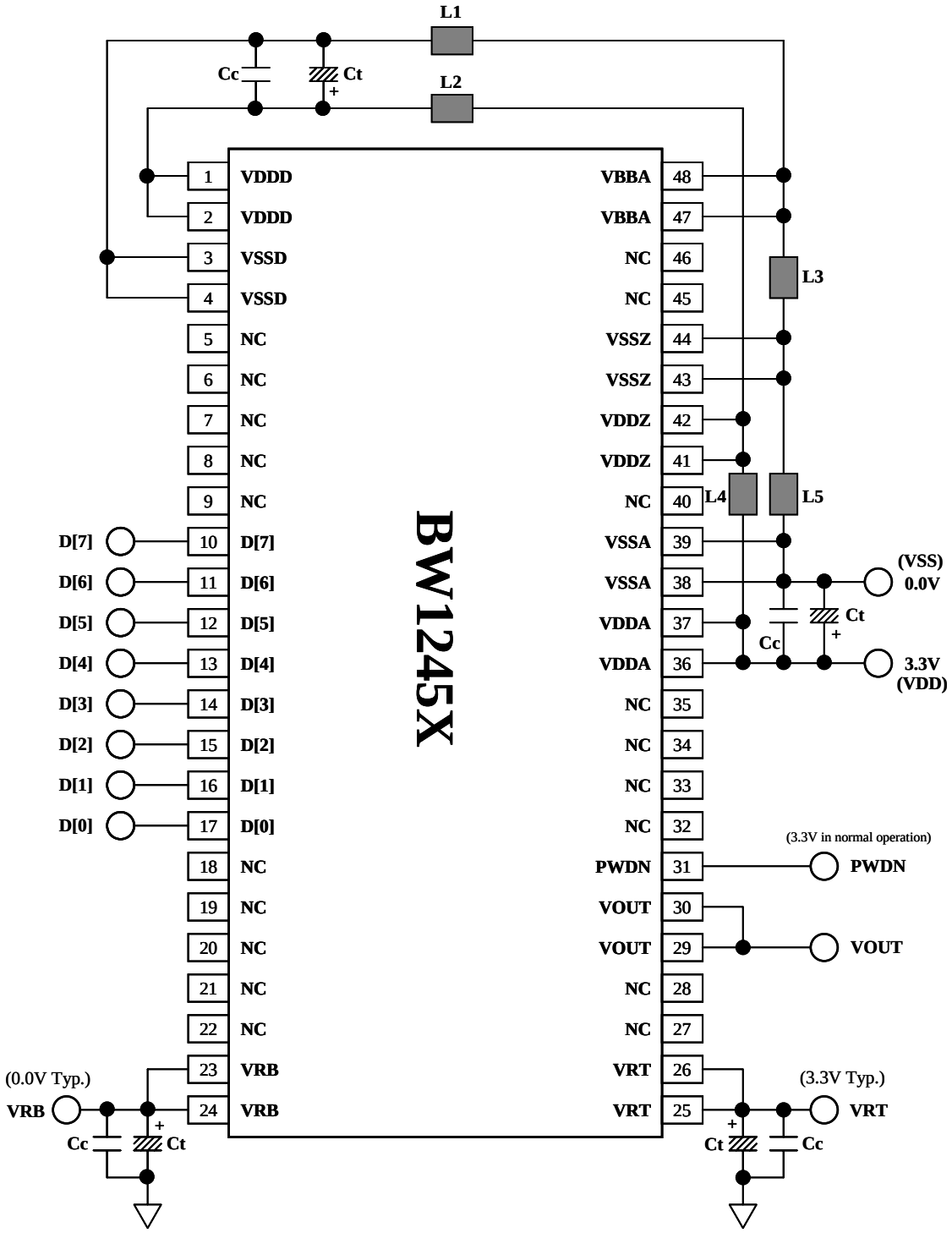
PHANTOM CELL INFORMATION



Pin Name	Property	Pin Usage	Pin Layout Guide
D[7:0]	DI	Internal / External	1. Digital Input Signal lines must have same length to reduce propagation delay.
PWDN	DI	Internal / External	
VRT	AB	External	1. Voltage reference lines (VRT and VRB) must be wide metal to reduce voltage drop of metal lines. 2. VOUT signal should not be crossed by any signals and should not run next to digital signals to minimize capacitive coupling between the two signals.
VRB	AB	External	
VOUT	AO	Internal / External	
VDDA	AP	External	1. It is recommended that you use thick analog power metal. When connected to PAD, the path should be kept as short as possible. 2. Digital power and analog power are separately used. 3. VBBA has two ports and they are connected internally, so you may connect just one of them with VBBA pad.
VSSA	AG	External	
VDDD	DP	External	
VSSD	DG	External	
VBBA	AG	External	

1. When the core block is connected to other blocks, it must be double guard-ring using N-well and P+ active to remove the substrate and coupling noise.
   In that case, the power metal should be connected to PAD directly.
2. The Bulk power is used to reduce the influence of substrate noise.

PACKAGE CONFIGURATION



LOCATION	DESCRIPTION
Ct	10uF TANTALUM CAPACITOR
Cc	0.1uF CERAMIC CAPACITOR
L1~L5	FERRITE BEAD (0.1mh)

PACKAGE PIN DESCRIPTION

NAME	PIN NO	I/O TYPE	PIN DESCRIPTION
VDDD	1,2	DP	Digital Power (3.3V)
VSSD	3,4	DG	Digital Ground (0.0V)
D[7:0]	10~17	DI	Digital Input Data
VRB	23,24	AB	Voltage Reference Bottom (0.0V)
VRT	25,26	AB	Voltage Reference Top (3.3V)
VOUT	29,30	AO	Analog Voltage Output
PWDN	31	DI	Power Down Mode (Low Active)
VDDA	36,37	AP	Analog Power (3.3V)
VSSA	38,39	AG	Analog Ground (0.0V)
VDDZ	41,42	AP	Pad Power (3.3V)
VSSZ	43,44	AG	Pad Ground (0.0V)
VBBA	47,48	AG	Analog Sub Bias (0.0V)
NC	5,6,7,8,9,18,19 20,21,22,27 28,32,33,34 35,40,45,46	DO	No Connection

I/O TYPE ABBR.

- AI : Analog Input
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- DO : Digital Output
- AB : Analog Bidirectional
- DB : Digital Bidirectional

- AP : Analog Power
- DP : Digital Power
- AG : Analog Ground
- DG : Digital Ground

PC BOARD LAYOUT CONSIDERATION

1. PC Board Considerations

To minimize noise on the power lines and the ground lines, the digital inputs need to be shielded and decoupled. This trace length between groups of VDD (VDDA,VDDD) and VSS (VSSA,VSSD) pins should be as short as possible so as to minimize inductive ringing.

2. Supply Decoupling and Planes

For the decoupling capacitor between the power line and the ground line, 0.1uF ceramic capacitor is used in parallel with a 10uF tantalum capacitor.
The digital power plane(VDDD) and analog power plane(VDDA) are connected through a ferrite bead, and also the digital ground plane(VSSD) and the analog ground plane(VSSA). This ferrite bead should be located within 3inches of the BW1245X. The analog power plane supplies power to the BW1245X of the analog output pin and related devices.

FEEDBACK REQUEST

We appreciate your interest in out products.
If you have further questions, please specify in the attached form.
Thank you very much.

DC / AC ELECTRICAL CHARACTERISTIC

Characteristics	Min	Typ	Max	Unit	Remarks
Supply Voltage				V	
Power dissipation				mW	
Resolution				Bits	
Analog Output Voltage				V	
Operating Temperature				°C	
Output Load Capacitor				pF	
Output Load Resistor				kΩ	
Integral Non-Linearity Error				LSB	
Differential Non-Linearity Error				LSB	
Maximum Conversion Rate				MHz	

VOLTAGE OUTPUT DAC

Reference Voltage TOP BOTTOM				V	
Analog Output Voltage Range				V	
Digital Input Format	Binary Code or 2's Complement Code				

CURRENT OUTPUT DAC

Analog Output Maximum Current				mA	
Analog Output Maximum Signal Frequency				kHz	
Reference Voltage				V	
External Resistor for Current Setting(RSET)				Ω	
Pipeline Delay				sec	

- Do you want to Power down mode?
- Do you want to Internal Reference Voltage(BGR)?
- Which do you want to serial input data type or parallel input data type?
- Do you need 5V power supply in your system?

HISTORY CARD

Version	Date	Modified Items	Comments
Ver 1.5	00.02.22	Version updated All pictures and texts are modified with dac1236x's datasheet. The format ant fonts of datasheet are same with dac1236x's datasheet.	Reference datasheet DAC1236X BW1244X BW1244D
Ver 1.6	01.03.28	Version Updated page 4 : power down mode current ($\rightarrow$10uA) page 11 : °C $\rightarrow$ kΩ (Output Load Resistor)	
Ver 1.7	01.04.23	Version Updated page 11 : Interal $\rightarrow$ Internal	
Ver 1.8	02.04.23	Version Updated page 5 : functional description is modified. page 6 : functon $\rightarrow$ function page 7 : phantom cell is modified and table is added. page 8 : VRT pin number is modified (18 $\rightarrow$ 25) page 11 : W $\rightarrow$ Ω	