Ordering number : ENN*6710

CMOS IC

LC868901/51

Row Driver IC for Dot Matrix Graphic LCD

Preliminary

Overview

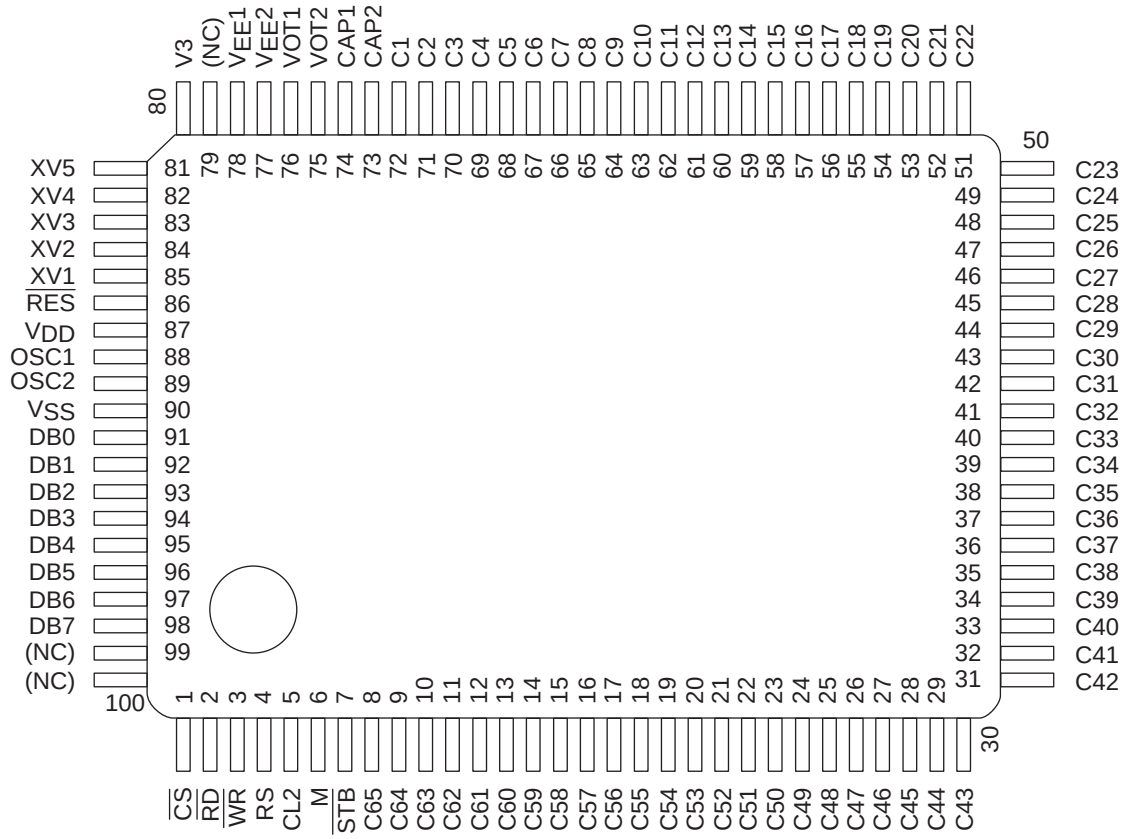
The LC868901 sereis is a common driver for the liquid crystal dot-matrix graphic display. It generates 65 commons maximum. The LC868901series has the RC-oscillator circuit attached resistor and the capacitor outside, and generates the timing signals and LCD powers for the LC868900 segmentdrivers.
As the LC868901 series is fabricated using CMOS process technology, combining it with a CMOS microcontroller produces an LCD device of low power demand.

Features

- Classification
  - Interfacing allowed for 80-family and our LC868000 microcontroller :LC868901
  - Interfacing allowed for Motorola family :LC868951
- 65 common outputs
- Automatic LCD display controller
  - Duty 1 / 1 to 1 / 65 (programmable)
  - Bias 1 / 5, 1 / 7 and 1 / 9 (programmable)
  - Contrasts 32-step programmable
  - Instructions
    - Display on / off
    - Horizontal display bit control
      - [Horizontal display number] × [Display pitch (bit length)]
    - Busy flag readable
- Built-in power booster
- Stand-by function
  - Two kinds of stand-by setting
    1. Applying low level to $\overline{STB}$
    2. Programming
  - Stand-by releasing
    - Read after applying low level to $\overline{CS}$ and $\overline{RD}$
- Oscillator
  - RC oscillator must be attached resistor and the capacitor outside.
- Power supply
  - Logic circuit 3V to 5V (V_{DD})
- CMOS process
- Factory shipment
  - Chip delivery form
  - QFP100E package

SANYO Electric Co.,Ltd. Semiconductor Company
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Pin Assignment



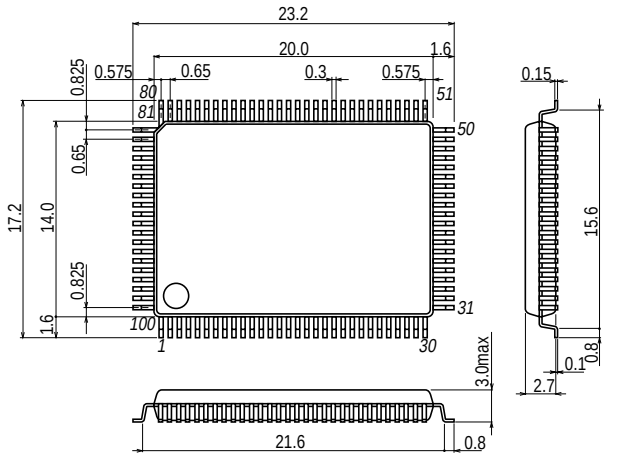
SANYO : QIP-100E

ILC00202

Package Dimension

(unit : mm)

3151



SANYO : QIP-100E
(FLP100)

Pads

Pin No.	Pad No.	name	Pad axis	
			X μm	Yμm
1	1	$\overline{CS}$	−2113	−1645
2	2	$\overline{RD}$	−1950	−1645
3	3	$\overline{WR}$	−1788	−1645
4	4	RS	−1625	−1645
5	5	CL2	−1463	−1645
6	6	M	−1300	−1645
7	7	$\overline{STB}$	−1138	−1645
8	8	C65	−914	−1794
9	9	C64	−752	−1794
10	10	C63	−589	−1794
11	11	C62	−427	-1794
12	12	C61	−264	−1794
13	13	C60	−102	−1794
14	14	C59	61	−1794
15	15	C58	223	−1794
16	16	C57	386	−1794
17	17	C56	548	−1794
18	18	C55	711	−1794
19	19	C54	873	-1794
20	20	C53	1036	−1794
21	21	C52	1198	−1794
22	22	C51	1361	−1794
23	23	C50	1523	−1794
24	24	C49	1686	−1794
25	25	C48	1848	−1794
26	26	C47	2011	−1794
27	27	C46	2173	−1794
28	28	C45	2336	−1794
29	29	C44	2498	−1794
30	30	C43	2661	−1794
31	31	C42	2690	−1482
32	32	C41	2690	−1320
33	33	C40	2690	−1157
34	34	C39	2690	−995
35	35	C38	2690	−832
36	36	C37	2690	−670
37	37	C36	2690	−507
38	38	C35	2690	−345
39	39	C34	2690	−182
40	40	C33	2690	−20
41	41	C32	2690	143
42	42	C31	2690	305
43	43	C30	2690	468
44	44	C29	2690	630
45	45	C28	2690	793
46	46	C27	2690	955
47	47	C26	2690	1118
48	48	C25	2690	1280
49	49	C24	2690	1443
50	50	C23	2690	1605

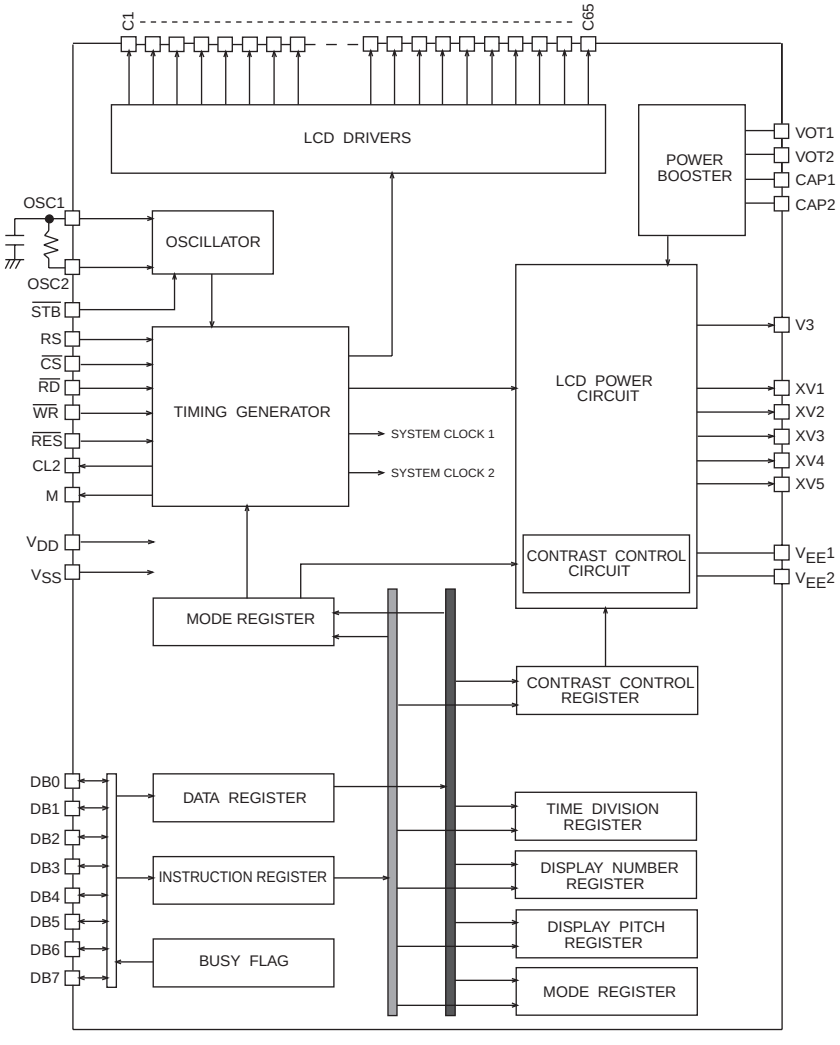
Pin No.	Pad No.	name	Pad axis	
			X μm	Yμm
51	51	C22	2478	1764
52	52	C21	2315	1764
53	53	C20	2153	1764
54	54	C19	1990	1764
55	55	C18	1828	1764
56	56	C17	1665	1764
57	57	C16	1503	1764
58	58	C15	1340	1764
59	59	C14	1178	1764
60	60	C13	1015	1764
61	61	C12	853	1764
62	62	C11	690	1764
63	63	C10	528	1764
64	64	C9	365	1764
65	65	C8	203	1764
66	66	C7	40	1764
67	67	C6	−122	1764
68	68	C5	−285	1764
69	69	C4	−447	1764
70	70	C3	−610	1764
71	71	C2	−772	1764
72	72	C1	−935	1764
73	73	CAP2	−1569	1617
74	74	CAP1	−1732	1617
75	75	VOT2	−1894	1617
76	76	VOT1	−2057	1617
77	77	$V_{EE}2$	−2278	1617
78	78	$V_{EE}1$	−2441	1617
79	−	NC		
80	79	V3	−2603	1617
81	80	XV5	−2526	1156
82	81	XV4	−2526	993
83	82	XV3	−2526	831
84	83	XV2	−2526	668
85	84	XV1	−2526	506
86	85	$\overline{RES}$	−2556	316
87	86	V_{DD}	−2556	153
88	87	OSC1	−2556	−9
89	88	OSC2	−2556	−172
90	89	V_{SS}	−2556	−334
91	90	DB0	−2556	−497
92	91	DB1	−2556	−659
93	92	DB2	−2556	−822
94	93	DB3	−2556	−984
95	94	DB4	−2556	−1147
96	95	DB5	−2556	−1309
97	96	DB6	−2556	−1472
98	97	DB7	−2556	−1634
99	−	NC		
100	−	NC		

Notes 1. Using for chip, the substrate must be shortened to V_{DD}, or left open.
2. Ask the solder-soaking condition for QFP100E package.

Pin function

Pin name	Pin No.	I / O	Description	Pin form type
V_{SS}	90	–	Negative power pin (–)	
V_{DD}	87	–	Positive power pin (+)	
V_{EE}1, 2	78, 77	–	LCD power pins	
VOT1, 2	76, 75	–	Power booster pins	
CAP1, 2	74, 73	–	Capacitor connecting pins for power booster	
DB0 to DB7	91 to 98	I / O	Data bus	DB0-4, 7 : C DB5, 6 : D
$\overline{RES}$	86	Input	Reset (active low)	B
$\overline{CS}$	1	Input	Chip select (active low)	A
$\overline{RD}$	2	Input	Read (active low)	A
$\overline{WR}$	3	Input	Write (active low)	A
RS	4	Input	Register select RS=1 : instruction register RS=0 : data register	A
CL2	5	Output	LCD clock for data shifting	E
M	6	Output	LCD clock for synchronizing	E
$\overline{STB}$	7	Input	Stand-by (active low)	B
V3	80	Output	Monitor pin for LCD power	
XV1 to XV5	85 to 81	Output	LCD power suppliers	
C1 to C65	72 to 8	Output	Common outputs for LCD display	F

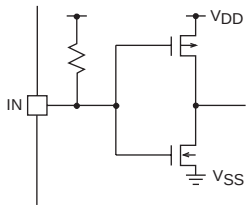
Block Diagram



ILC00203

Pin forms

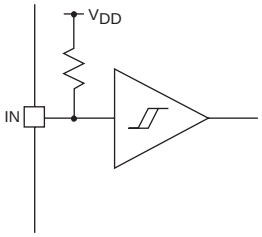
A type



ILC00204

$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, RS pins

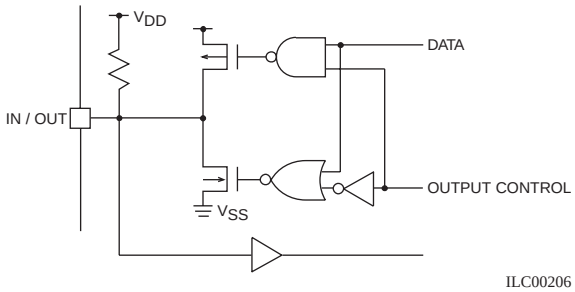
B type



ILC00205

$\overline{RES}$, $\overline{STB}$ pins

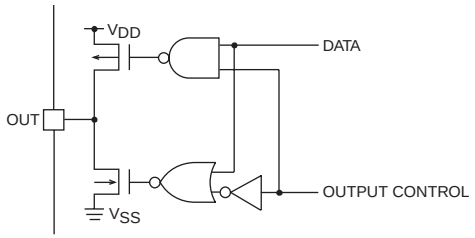
C type



ILC00206

DB0 to DB4, DB7

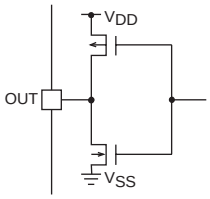
D type



ILC00207

DB5, DB6

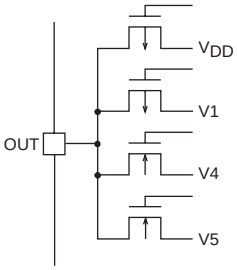
E type



ILC00208

CL2, M

F type



ILC00209

C1 to C65

1. Absolute Maximum Ratings at Ta=25°C, V_{SS}=0V

Parameter	Symbol	Pins	Conditions		Ratings			unit
				V_{DD}[v]	min.	typ.	max.	
Supply voltage	V_{DD} MAX	V_{DD}			−0.3		+7.0	V
Input voltage	VI(1)	$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, RS, $\overline{RES}$			−0.3		VDD+0.3	
	V_I(2)	DB0 to DB7	At input mode		−0.3		V_{DD}+0.3	
	V_I(3)	V_{EE}1, V_{EE}2			V_{DD}−21		V_{DD}+0.3	
Output voltage	V_O(1)	C1 to C65			V_{EE}2−0.3		V_{DD}+0.3	
	V_O(2)	DB0 to DB7	At output mode		−0.3		V_{DD}+0.3	
	V_O(3)	M, CL2			−0.3		V_{DD}+0.3	
	V_O(4)	VOT1, VOT2, CAP1, CAP2			V_{DD}−21		V_{DD}+0.3	
High-level output current	∑IOAH	C1 to C65	The total all pins		−25			mA
Low-level output current	∑IOAL	C1 to C65	The total all pins				30	mA
Maximum power dissipation	Pdmax	QFP100E	Ta= −30 to + 70°C				200	mW
Operating temperature limits	Topg				−30		70	°C
Storage temperature limits	Tstg				−55		150	

2. Recommended Operating Limits at Ta= −30°C to +70°C, V_{SS}=0V

Parameter	Symbol	Pins	Conditions		Ratings			unit
				V_{DD} [V]	min.	typ.	max.	
Operating supply voltage limits	V_{DD}	V_{DD}			2.5		6.0	V
LCD power supply voltage limits	V_{EE}	V_{EE}1, V_{EE}2		4.5 to 6.0	−2V_{DD}		V_{DD}	
				2.5 to 4.5	−V_{DD}		V_{DD}	
Input high voltage	V_{IH}(1)	DB0 to DB7	At input mode	4.5 to 6.0	2.2		V_{DD}	
				2.5 to 4.5	0.75V_{DD}		V_{DD}	
	VIH(2)	$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, RS		4.5 to 6.0	2.2		VDD	
				2.5 to 4.5	0.75V_{DD}		V_{DD}	
	VIH(3)	$\overline{RES}$ (schmitt), $\overline{STB}$ (schmitt)		4.5 to 6.0	0.75VDD		VDD	
				2.5 to 4.5	0.75V_{DD}		V_{DD}	
Input low voltage	V_{IL}(1)	DB0 to DB7	At input mode	4.5 to 6.0	0		0.8	
				2.5 to 4.5	0		0.25V_{DD}	
	V_{IL}(2)	$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, RS		4.5 to 6.0	0		0.8	
				2.5 to 4.5	0		0.25V_{DD}	
	VIL(3)	$\overline{RES}$ (schmitt), $\overline{STB}$ (schmitt)		4.5 to 6.0	0		0.25VDD	
				2.5 to 4.5	0		0.25V_{DD}	
Oscillation frequency limits	FRC	OSC1, OSC2	•RC oscillation •Fig. 1	2.5 to 6.0	20		500	kHz

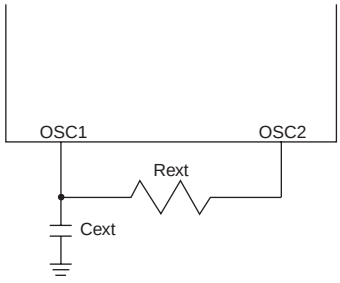


Fig.1 RC-oscillator circuit ILC00210

3. Electrical Characteristics at Ta= –30°C to +70°C

Parameter	Symbol	Pins	Conditions		Ratings			unit
				V_{DD} [V]	min.	typ.	max.	
Output high voltage	V_{OH}(1)	DB80 to DB7	•output mode •I_{OH}= –1mA	4.5 to 6.0	V_{DD}–1.0			V
			•output mode •I_{OH}= –0.1mA	2.5 to 6.0	V_{DD}–0.5			
	V_{OH}(2)	M, CL2	I_{OH}= –0.4mA	4.5 to 6.0	V_{DD}–0.4			
			I_{OH}= –0.1mA	2.5 to 6.0	V_{DD}–0.5			
Output low voltage	V_{OL}(1)	DB0 to DB7	•output mode •I_{OL}=+0.6mA	4.5 to 6.0			0.4	
			•output mode •I_{OH}=+0.1mA	2.5 to 6.0			0.4	
	V_{OL}(2)	M, CL2	I_{OL}=+0.4mA	4.5 to 6.0			0.4	
			I_{OL}=+0.1mA	2.5 to 6.0			0.5	
Pull-up resistance	RPU(1)	DB0 to DB7	•input mode •V_{IN}=0V	4.5 to 6.0	150	500	900	kΩ
			•input mode •V_{IN}=0V	2.5 to 4.5	300	750	1500	
	RPU(2)	$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, RS, $\overline{RES}$, $\overline{STB}$	VIN=0V	4.5 to 6.0	150	500	900	
			V_{IN}=0V	2.5 to 4.5	300	750	1500	
Drop voltage between V_{DD} and Ci (i : 1 to 65)	V_D(1)	C1 to C65	•–100µA at each Ci pin •V_{DD}-V_{EE}2=11V	4.5 to 6.0			150	mV
			•–15µA at each Ci pin •V_{DD}-V_{EE}2=11V	2.5 to 6.0			120	
Drop voltage between VX and Ci (X : 1, 4) (i : 1 to 65)	V_D(2)	C1 to C65	•–100µA at each Ci pin •V_{DD}-V_{EE}2=11V	4.5 to 6.0			150	mV
			•–15µA at each Ci pin •V_{DD}-V_{EE}2=11V	2.5 to 6.0			120	
Drop voltage between VX and Ci (X : 1, 4) (i : 1 to 65)	V_D(3)	C1 to C65	•+100µA at each Ci pin •V_{DD}-V_{EE}2=11V	4.5 to 6.0	–150			mV
			•+15µA at each Ci pin •V_{DD}-V_{EE}2=11V	2.5 to 6.0	–120			
Boosted voltage	VOT1	•VOT1 •Fig. 2	Load current =500µA	5.0		–4.5		V
			Load current =800µA				–4.0	
			Load current =100µA	2.9		–2.6		V
			Load current =200µA				–2.3	
	VOT2	•VOT2 •Fig. 3	Load current =500µA	5.0		–8.0		V
			Load current =800µA				–6.0	

Parameter	Symbol	Pins	Conditions		Ratings			unit
				V_{DD} [V]	min.	typ.	max.	
Hysterisis voltage	VHIS	$\overline{RES}$, $\overline{STB}$		2.5 to 6.0		0.1VDD		V
XV1 output voltage	VV1	XV1	•LCD ON •1 / 5 bias •XV5=0V •LCD clock frequency=0Hz •Fig. 4	2.5 to 6.0	0.75V_{DD}	0.80V_{DD}	0.85V_{DD}	V
XV2 output voltage	VV2	XV2		2.5 to 6.0	0.55V_{DD}	0.60V_{DD}	0.65V_{DD}	
XV3 output voltage	VV3	XV3		2.5 to 6.0	0.35V_{DD}	0.40V_{DD}	0.45V_{DD}	
XV4 output voltage	VV4	XV4		2.5 to 6.0	0.15V_{DD}	0.20V_{DD}	0.25V_{DD}	
LCD power current	ILCD1	•$V_{EE}1$, $V_{EE}2$ •1 / 5 bias	•LCD ON •$V_{EE}1$=OPEN •$V_{EE}2$=0V •XV1-XV5=OPEN •Fig. 5 •CCR0-4=0	5.0	25	50	100	μA
				2.9	15	29	60	
	ILCD2	•$V_{EE}1$, $V_{EE}2$ •1 / 7 bias		5.0	18	35.7	70	
				2.9	10	20.7	40	
	ILCD3	•$V_{EE}1$, $V_{EE}2$ •1 / 9 bias		5.0	14	27.8	56	
				2.9	8	16	32	
Contrast current	ILC1	•$V_{EE}1$, $V_{EE}2$ •CCR=01H	•LCD ON •$V_{EE}1$=OPEN •$V_{EE}2$=−3V •XV5=0V •Fig. 6	5.0	750	1000	1500	μA
				2.9	750	1000	1500	
	ILC2	•$V_{EE}1$, $V_{EE}2$ •CCR=02H		5.0	370	500	750	
				2.9	370	500	750	
	ILC3	•$V_{EE}1$, $V_{EE}2$ •CCR=04H		5.0	200	250	400	
				2.9	200	250	400	
	ILC4	•$V_{EE}1$, $V_{EE}2$ •CCR=08H		5.0	100	125	200	
				2.9	100	125	200	
	ILC5	•$V_{EE}1$, $V_{EE}2$ •CCR=10H		5.0	50	62	100	
				2.9	50	62	100	
Operation current dissipation	IDD(1)		•FRC=500kHz •LCD OFF •Fig. 7	4.5 to 6.0		200	400	μA
				2.5 to 4.5		100	300	
Stand-by current dissipation	IDD(2)		•FRC=0Hz •LCD OFF •Fig. 7	4.5 to 6.0		0.05	30	μA
				2.5 to 4.5		0.02	20	

[Notes]
The specifications above are for a die mounted in a QFP100E type package.
However, we ship this product as a die only, not a package chip.
Therefore, the operational characteristics may vary depending on the user's packaging techniques.

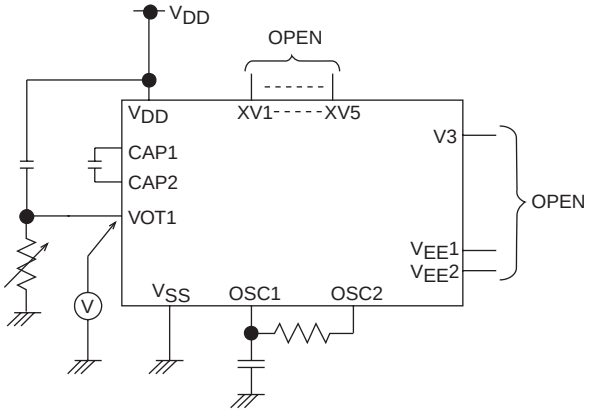


Fig.2 Measurement circuit for boosted voltage (1)

ILC00211

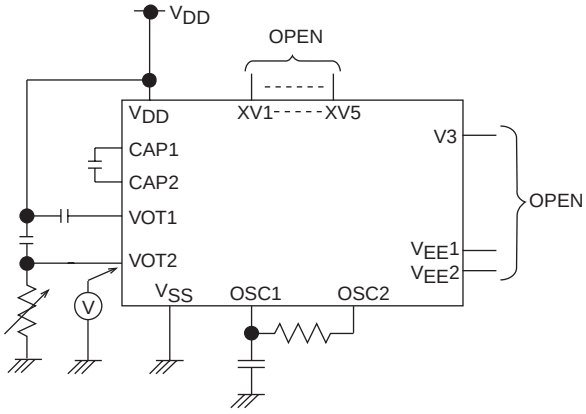


Fig.3 Measurement circuit for boosted voltage (2)

ILC00212

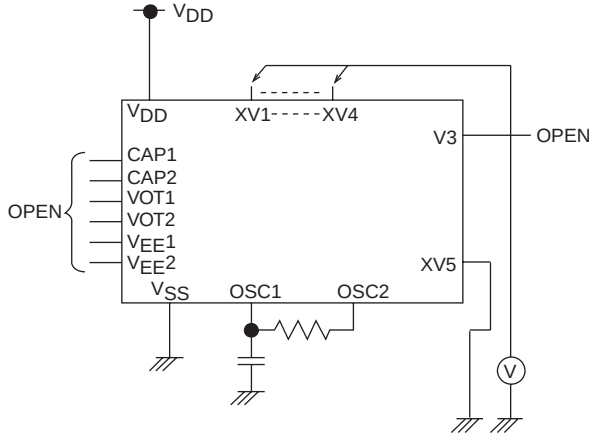


Fig.4 Measurement circuit for XV1 to XV4

ILC00213

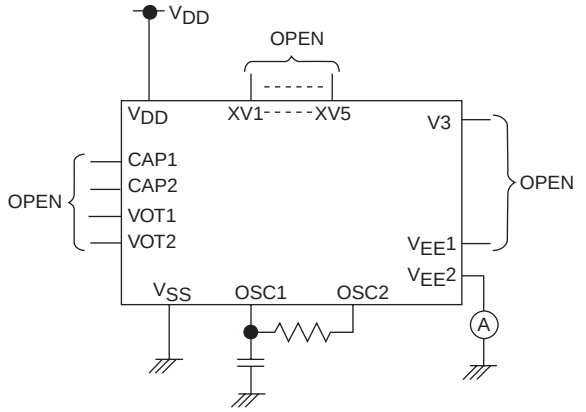


Fig.5 Measurement circuit for LCD power current

ILC00214

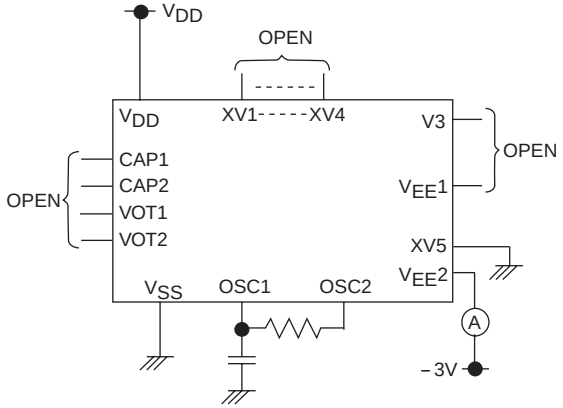


Fig.6 Measurement circuit for contrast current

ILC00215

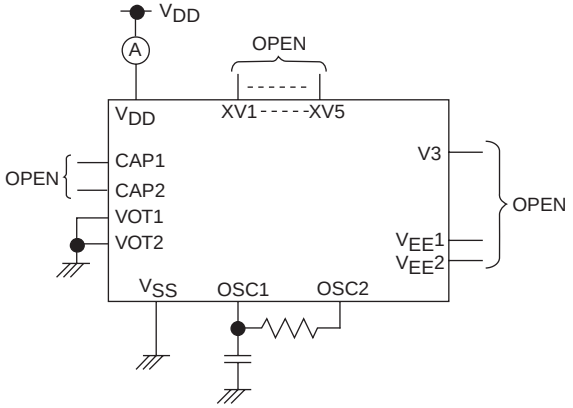
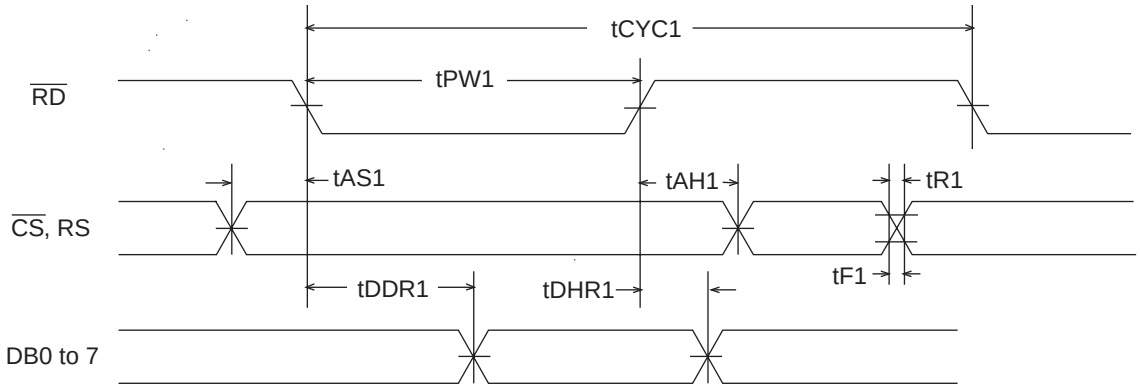


Fig.7 Measurement circuit for current dissiation

ILC00216

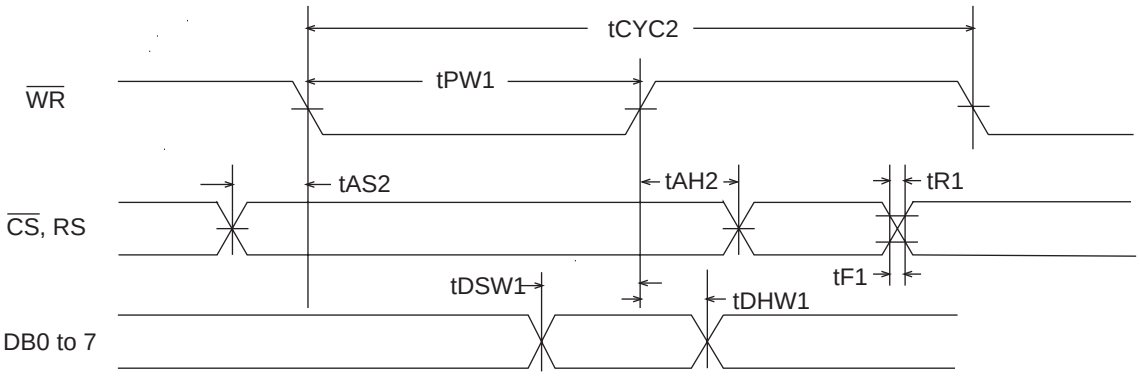
AC Characteristics at Ta= –30°C to +70°C

• Reading cycle



ILC00217

• Writing cycle

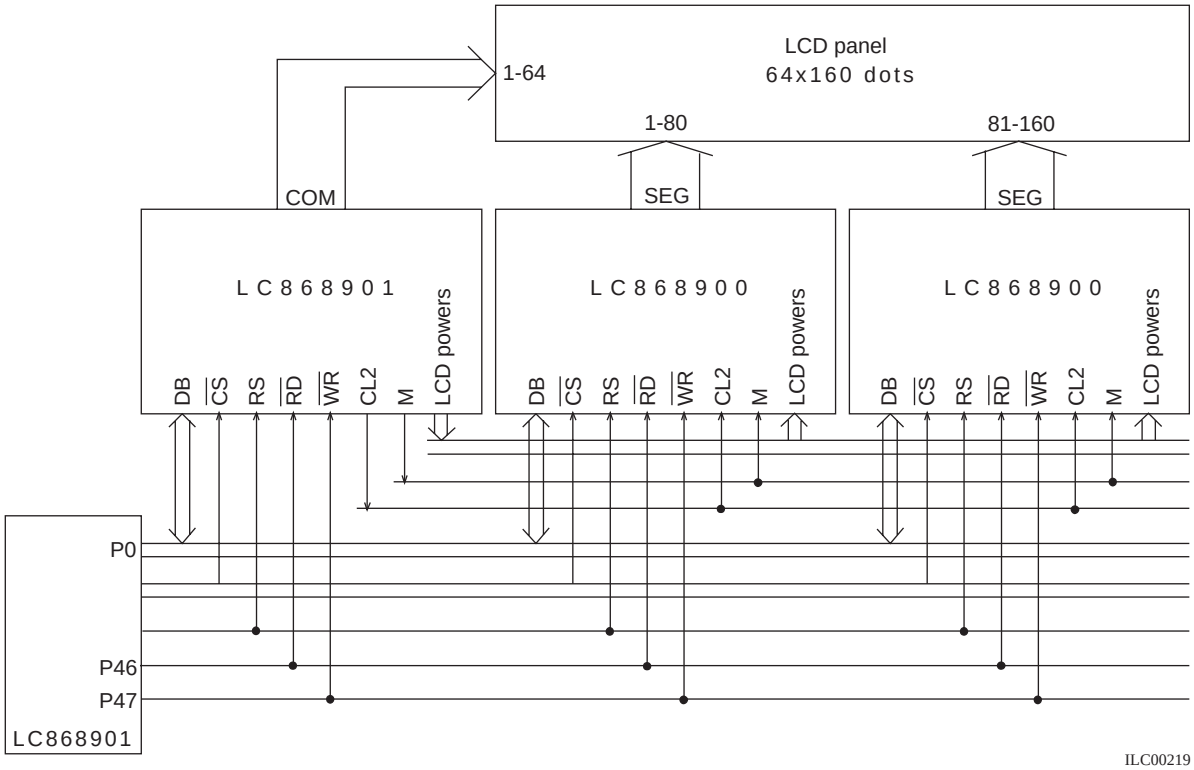


ILC00218

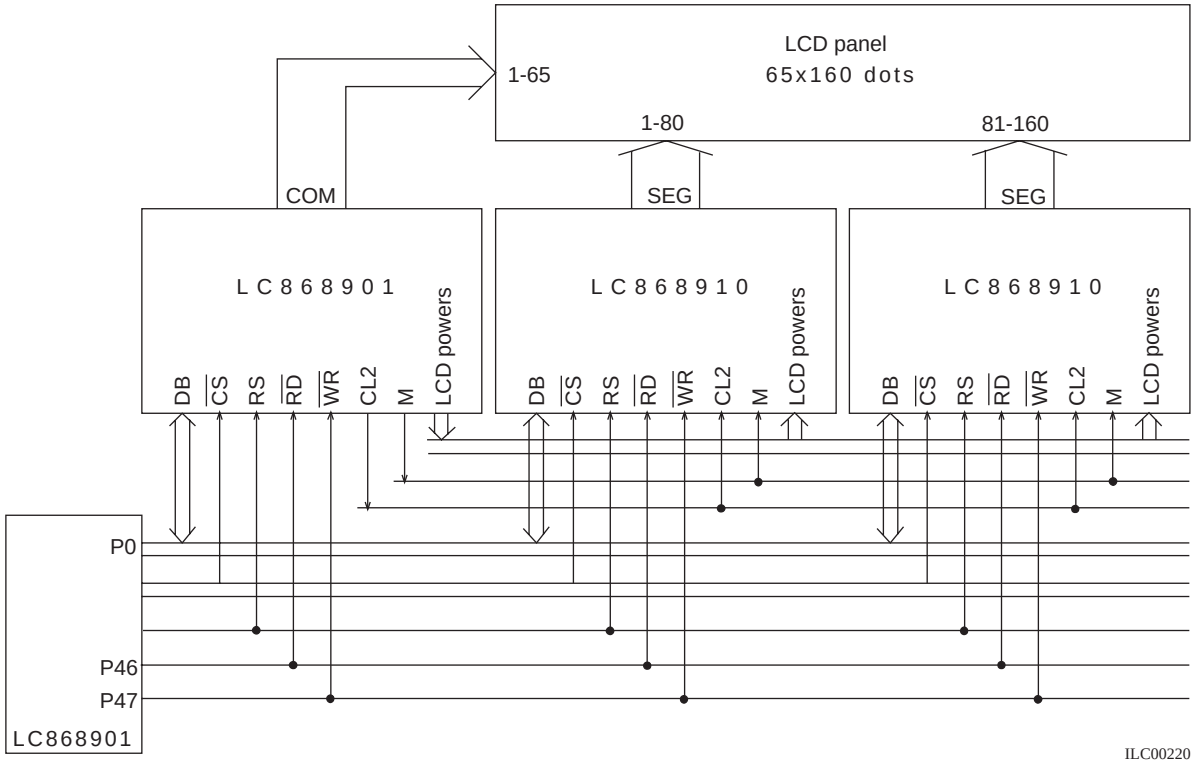
No.	Item	Symbol	Pins and Conditions		Value		unit
				VDD [V]	min.	max.	
1	$\overline{RD}$, $\overline{WR}$ cycle time	tCYC1	$\overline{RD}$	4.5 to 6.0	(500)		ns
				2.5 to 4.5			
		tCYC2	$\overline{WR}$	4.5 to 6.0	(500)		ns
				2.5 to 4.5			
2	$\overline{RD}$ pulse width $\overline{WR}$ pulse width	tPW1	$\overline{RD}$ $\overline{WR}$	4.5 to 6.0	(220)		ns
				2.5 to 4.5			
3	Rise / fall time	tR1, tF1	$\overline{RD}$	4.5 to 6.0		(20)	ns
				2.5 to 4.5			
4	Address set-up time	tAS1	$\overline{CS}$, RS, $\overline{RD}$	4.5 to 6.0	(40)		ns
				2.5 to 4.5			
		tAS2	$\overline{CS}$, RS, $\overline{WR}$	4.5 to 6.0	(40)		ns
				2.5 to 4.5			
5	Address hold time	tAH1	$\overline{CS}$, RS, $\overline{RD}$	4.5 to 6.0	(10)		ns
				2.5 to 4.5			
		tAH2	$\overline{CS}$, RS, $\overline{WR}$	4.5 to 6.0	(10)		ns
				2.5 to 4.5			
6	Data delay time	tDDR1	$\overline{RD}$, DB0 to DB7, CL=50pF	4.5 to 6.0		(120)	ns
				2.5 to 4.5			
7	Data hold time	tDHR1	$\overline{RD}$, DB0 to DB7, CL=50pF	4.5 to 6.0	(20)		ns
				2.5 to 4.5			
8	Data set-up time	tDSW1	$\overline{WR}$, DB0 to DB7, CL=50pF	4.5 to 6.0	(60)		ns
				2.5 to 4.5			
9	Data hold time	tDHW1	$\overline{WR}$, DB0 to DB7, CL=50pF	4.5 to 6.0	(10)		ns
				2.5 to 4.5			

Applications

1. 64×160-dot display



2. 65×160-dot display



Block Descriptions

1. Interfacing block

The interfacing block is composed by an instruction register and five data registers. The instruction register selects the data register to transfer the following data.

a. Instruction register

The instruction register specifies five kinds of the data registers and holds the data until other instruction data is set to the instruction register. Also, this instruction register can be read a busy flag.

- instruction setting conditions
  1. Set $\overline{CS}$ to '0' (low level). for chip selecting
  2. Set $\overline{WR}$ to '0'. for write operating
  3. Set RS to '1'. for instruction specifying
  4. Set DB to the instruction data

b. Data registers

The five data-registers specify the parameters for displaying LCD, which are five of mode, display pitches, display number, time division, and contrast.

- data setting conditions
  1. Set $\overline{CS}$ to '0' (low level). for chip selecting
  2. Set $\overline{WR}$ to '0'. for write operating
  3. Set RS to '0'. for parameter specifying
  4. Set DB to the parameter data

Note that the instruction and data can be written while the RC oscillation runs.
Busy flag should be set during writing to the data register.

The instruction data, code, is shown below.

Specified register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Notes
Mode register	0	1	0	0	0	0	0	0	0	0	addressing
	0	0	mode data								data setting
Display Pitch register	0	1	0	0	0	0	0	0	0	1	addressing
	0	0	VOPON	VRSEL	-	-	-	Dp - 1			data setting
Display Number register	0	1	0	0	0	0	0	0	1	0	addressing
	0	0	Dn - 1								data setting
Time Division register	0	1	0	0	0	0	0	0	1	1	addressing
	0	0	0	0	Nx - 1						data setting
Contrast Control register	0	1	0	0	0	0	0	1	0	0	addressing
	0	0	BIAS1	BIAS0	BOOST	contrast data					data setting
Read busy flag	1	1	Busy	no meaning							data reading

2. Timing control block

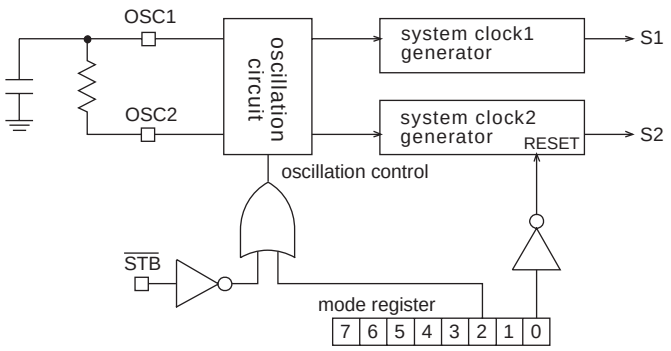
The timing control block is composed by the oscillator circuit and the timing generator circuit.

a. Oscillator

Resistor and capacitor must be mounted externally. The oscillator should be stop in stand-by state. See later chapter for more details.

b. Timing generator

The timing generator generates two system clocks and the several signals for LCD displaying. S1, system clock 1, runs for reading, writing and transferring data when the LC868901 is not in stand-by state and S2, system clock 2, runs while the LCD controller works.



ILC00221

CL2, M for LCD displaying should be generated to the LC868900 segment driver.
In stand-by state, all the generated signals freeze.

3. Busy flag

Busy flag is outputted to DB7 when reading operation is established with RS = 1.
The busy flag should be set to '1' during writing to the data register, not the instruction register.
When the writing operation is completed, the busy flag should be reset to '0'.
When the busy flag is set to '1', new parameter data cannot be written. Thus, write the data after reading the busy flag and making sure that it is '0'.

• busy-flag reading condition
1. Set $\overline{CS}$ to '0' (low level). for chip selecting
2. Set $\overline{RD}$ to '0'. for read operating
3. Set RS to '1'. for busy-flag reading

Reading operation need not to set the instruction register.

Register	R / W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Busy	1	1	Busy	no meaning						

4. Data registers

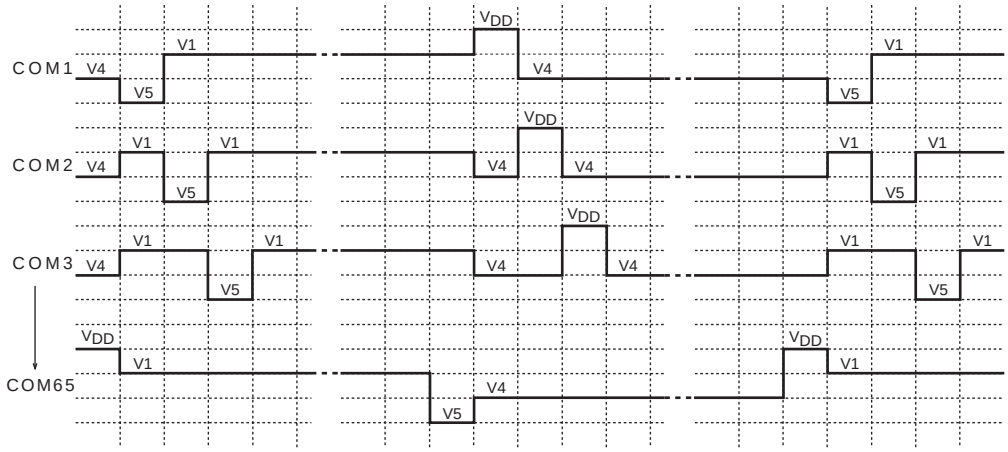
a. Mode register

Write code '00H' into the instruction register and specify the mode register.

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction	0	1	0	0	0	0	0	0	0	0
Mode	0	0	–			mode data				

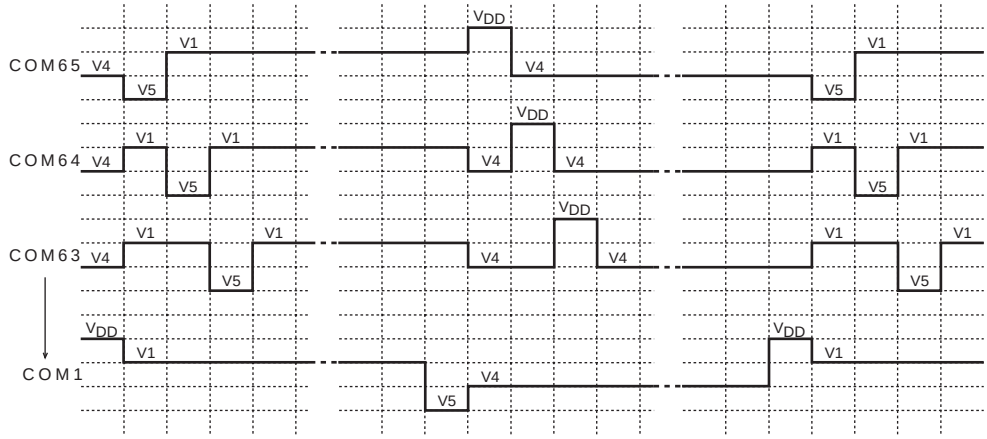
Mode0 (bit0 of mode register) LCD controller operation
Mode0=1 LCD controller starts to work. (S1 and S2 run)
Mode0=0 LCD controller stops. (S1 runs)
Mode0=0 when resetting or at stand-by state
Mode1 (bit1 of mode register) LCD display
Mode1=1 LCD display enable (ON)
Mode1=0 LCD display disable (OFF)
Mode1=0 when resetting or at stand-by state
Mode2 (bit2 of mode register) Stand-by
Mode2=1 Stand-by state
Mode2=0 Operation state
Mode3 (bit3 of mode register) Scanning direction
Mode3=1 C1 to C65 in 1 / 65 duty
Mode3=0 C65 to C1 in 1 / 65 duty
Mode3=0 when resetting

• Waveforms in case of C1 to C65



ILC00222

• Waveforms in case of C65 to C1

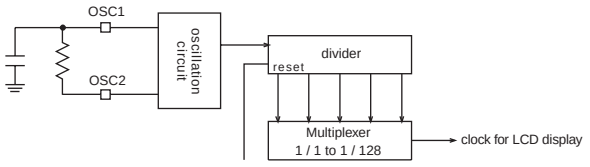


ILC00223

Mode4 to Mode6 (bit4 to bit6 of mode register) Time division

The following table shows the time division value.

Time Division	Mode6	Mode5	Mode4
1 / 1	0	0	0
1 / 2	0	0	1
1 / 4	0	1	0
1 / 8	0	1	1
1 / 16	1	0	0
1 / 32	1	0	1
1 / 64	1	1	0
1 / 128	1	1	1



ILC00224

Note that Mode1 should be set to '1' after setting the required LC868901-registers and the registers and RAM data of the equipped LC868900. Next shows the setting sequence for displaying ON.

1. Set Mode0 to '1' for starting the controller operation.
2. Set the registers of the LC868901/LC868900 and RAM data of the LC868900.
3. Set Mode1 to '1' for displaying ON.

Next shows the sequence for displaying OFF.

1. Set Mode1 to '0' for displaying OFF.
2. Set Mode0 to '0' for stopping the controller operation.

b. Horizontal pitch register

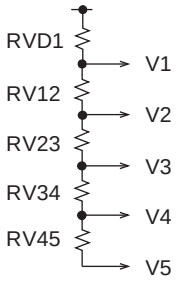
Write code ‘01H’ into the instruction register and specify the horizontal pitch register.

The horizontal pitch register specifies the horizontal pitch, the LCD power output and ladder resistor value.

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction	0	1	0	0	0	0	0	0	0	1
Pitch	0	0	VOPON	VRSEL	–	–	–	Dp-1		

- VOPON specifies the LCD power source.
  When VOPON=1, the LCD powers, XV1 to XV5, are provided through the OP-amps.
  When VOPON=0, the LCD powers are provided by the ladder resistors directly.
- VRSEL specifies resistance of the ladder resistors. See the following table.
  When VRSEL=1, all resistance of the ladder resistors is specified to 4kohms.
  When VRSEL=0, all resistance is specified to 20kohms.
- Dp indicates how many bits from the LC868900 RAM data appear in an 1-byte display.
  Dp must be set one of the following three values.

Dp	DB2	DB1	DB0	Display pitch
6	1	0	1	6
7	1	1	0	7
8	1	1	1	8



	VRSEL	
	0	1
RVD1	20kΩ	4kΩ
RV12	20kΩ	4kΩ
RV23	20kΩ	4kΩ
RV34	20kΩ	4kΩ
RV45	20kΩ	4kΩ

ILC00225

Note that RV23 varies according to the specified bias. (c.f. RV23=60k ohms at VRSEL = 0 in 1 / 7-bias specification)

c. Horizontal number register

Write code ‘02H’ into the instruction register and specify the horizontal number register.

The horizontal number register specifies the horizontal display number.

Register	R / W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction	0	1	0	0	0	0	0	0	1	0
Number	0	0	Dn - 1							

- Dn indicates the number of bytes in the horizontal direction.
- N, the total number of dots positioned horizontally on the screen, is given by the following formula.
  N=Dp * Dn (N≤80)
- Numbers in range 2 to 10 in decimal can be set as Dn.

d. Time division register

Write code ‘03H’ into the instruction register and specify the time division register.

The time division register specifies the display duty.

Register	R / W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction	0	1	0	0	0	0	0	0	1	1
Division	0	0	0	Nx - 1						

• Nx represents the number of the time divisions.
• Consequently, 1 / Nx value means the display duty.
• Numbers in range 2 to 65 in decimal can be set as Nx.

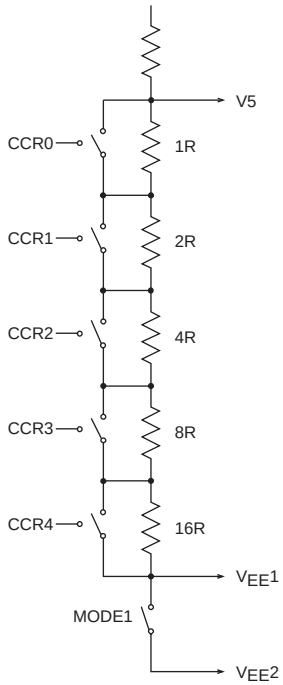
e. Contrast control register

Write code '04H' into the instruction register and specify the contrast control register.
The contrast control register specifies the contrast resistor value, the display bias and the power booster.

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction	0	1	0	0	0	0	1	0	0	0
Contrast	0	0	BIAS1	BIAS0	BOOST	CONTRAST				

• CONTRAST(CCR4-0) specifies in 32-step contrast resistor value. See the following table.

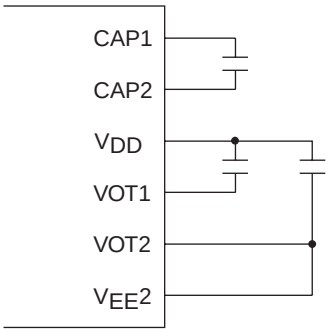
CCR4	CCR3	CCR2	CCR1	CCR0	Value
0	0	0	0	0	0
0	0	0	0	1	1R
0	0	0	1	0	2R
⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	0	30R
1	1	1	1	1	31R



• External contrast control available
  1. CONTRAST=0for setting the contrast control resistance to 0 ohm.
  2. Variable Resistor must be connected between $V_{EE}2$ and the negative LCD power to adjust the LCD contrast.
• BOOST specifies the LCD power booster function.
  When BOOST = 1, the double power booster (doubler) functions.
  When BOOST = 0, the triple power booster (tripler) functions.

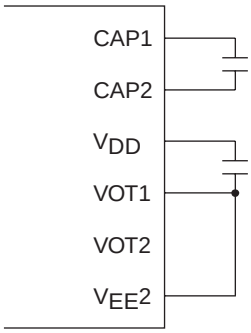
ILC00226

(a) Tripler
BOOST=0



ILC00227

(b) Doubler
BOOST=1



ILC00228

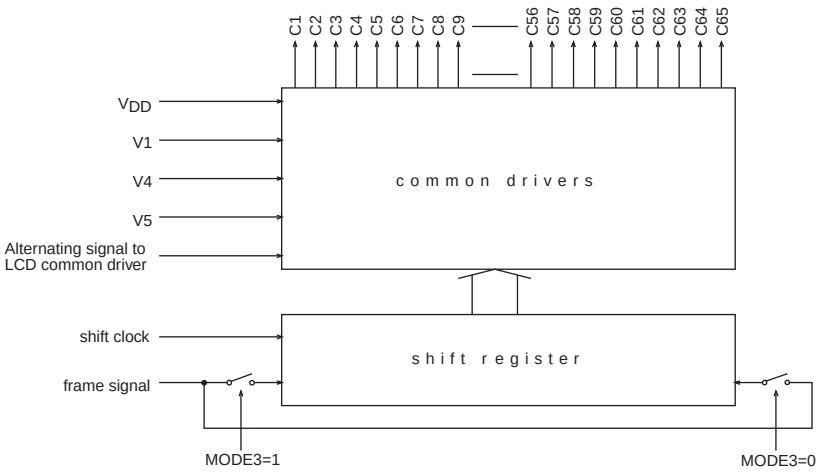
See 6. LCD power unit

• BIASes specify the displayed LCD bias.

BIAS1	BIAS0	bias
0	0	1 / 5
0	1	1 / 5
1	0	1 / 7
1	1	1 / 9

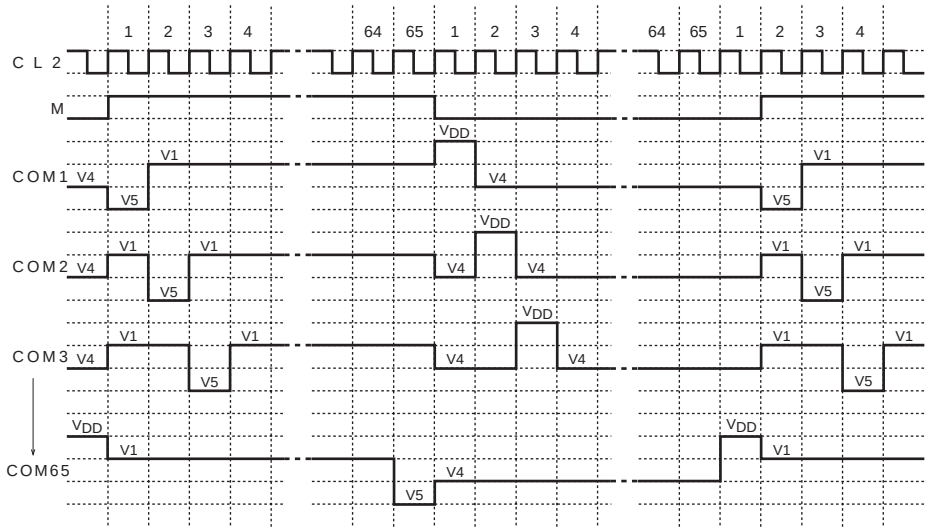
5. LCD driver unit

Next shows the common driver block diagram.



ILC00229

Common waves (MODE3=1, 1 / 65 duty)



ILC00230

Scanning direction can be set by MODE3, bit 3 of mode register.

MODE3=1 from C1 to C65

MODE3=0 from C65 to C1

Ex.1. MODE3=1 and 1 / 64 duty

Scanning direction C1 to C64

Available commons C1 to C64

Nonuse commons C65

Ex.2. MODE3=0 and 1 / 32 duty

Scanning direction C65 to C34

Available commons C34 to C65

Nonuse commons C1 to C33

Ex.3. MODE3=0 and 1 / 64 duty

Scanning direction C65 to C2

Available commons C2 to C65

Nonuse commons C1

6. LCD power unit

The LCD power unit provides the LCD powers to the attached drivers according to the specified bias. XV1 to XV5 pins are used.

• Bias

BIASes specify the displayed LCD bias.

BIAS1	BIAS0	bias
0	0	1 / 5
0	1	1 / 5
1	0	1 / 7
1	1	1 / 9

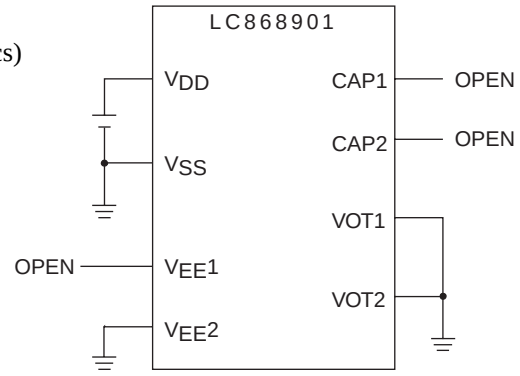
• LCD powers

The voltage of $V_{EE}2$ must be set according to the specified duty or the specification of an LCD panel.
The following four connections can be allowed.

1. $V_{EE}2=V_{SS}$

1 / 16 duty or less (according to the LCD-panel characteristics)

$V_{DD} - V_{SS} \geq 5V$



ILC00231

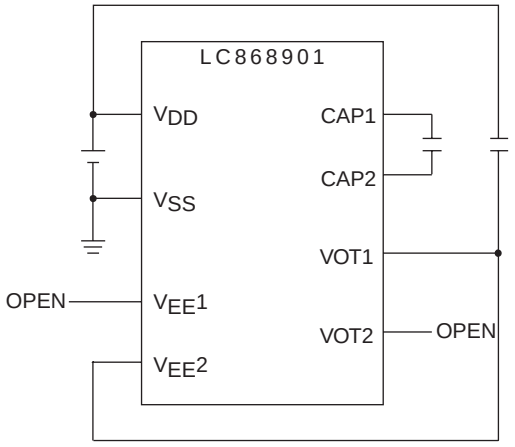
2. $V_{EE}2$=VOT1

The power booster provides two times of (V_{DD} - V_{SS}) voltage to VOT1.
The power booster must be attached two a capacitors.
The boosted powers are supplied to the following blocks.

- •LCD drivers
- •Ladder resistors
- •LCD contrast controller

The LCD-drive current is specified by the capacitance of the attached capacitor.

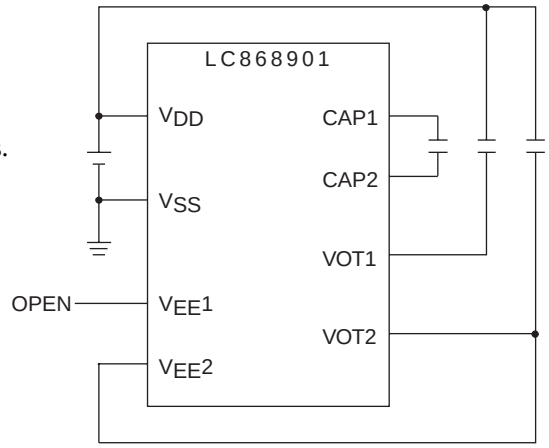
[Notes] Select doubler on program (BOOST = 1) when using VOT1.Never use VOT2 when selecting doubler.



ILC00232

3. $V_{EE}2$=VOT2

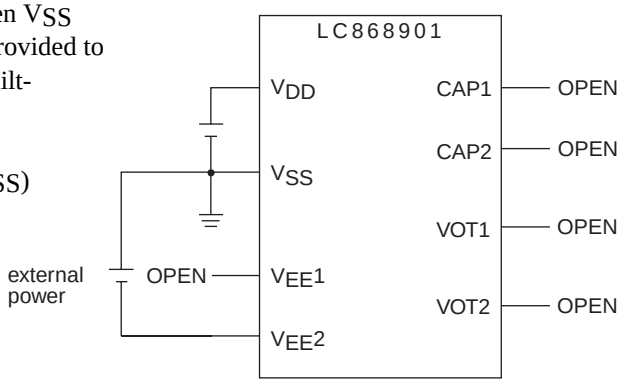
Set BOOST to '0' to use the tripler function.
The power booster provides three times of (V_{DD}–V_{SS}) voltage to VOT2.
The power booster must be attached three capacitors.
The boosted powers are supplied to the following blocks.
•LCD drivers
•Ladder resistors
•LCD contrast controller
The LCD-drive current is specified by the capacitance of the attached capacitors.



ILC00233

4. $V_{EE}2$ supplied by the external power unit

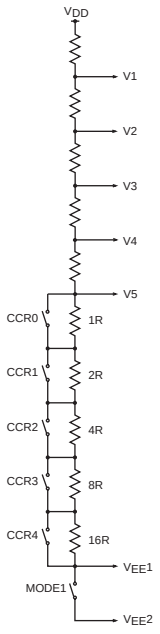
The external power unit must be attached between V_{SS} and $V_{EE}2$ if the LCD display voltage must be provided to the V_{DD}–V_{SS} voltage or more without using built-in power booster. See the following figure.
Set the external voltage as below.
0 v > [external power supply] > –3 x (V_{DD}–V_{SS})



ILC00234

• Contrast control

The LCD contrast can be specified by CCR, which is allowed to 32-step contrast.
If more than 32-step contrast must be needed, attach and adjust a variable resistor between $V_{EE}2$ and the specified power supply. See Contrast control register.



ILC00235

7. Stand-by function

Stand-by function is prepared to reduce the dissipation current while LCD off. 'Stand-by' means all the LC868901 function freeze. Thus, in stand-by state, the LCD controller and drivers stop operation. Two ways to make the LC868901 stand-by is prepared.

1) Set MODE2 (bit2 of mode register) to '1'.
2) Supply $\overline{STB}$ to low.

Also, two ways to release stand-by is prepared.

1) Reset Supply $\overline{RES}$ to low. It makes the LC868901 reset.
Supply $\overline{RES}$ to high to make the LC868901 run.
2) Reading Read the target LC868901. (i.e., $\overline{CS}$ = 0 and $\overline{RD}$ = 0)

[Notes] DB7 should be set output state at reading. So, ports connected to DB7 of the LC868901 must be set to the input state.

8. Reset function

Reset to initialize when the power is turned on.

Initialized value and state

1. busy flag reset
2. oscillator operate
3. stand-by release
4. LCD controller stop
5. LCD display off
6. LCD power XV1 to XV5=V_{DD}, $V_{EE}1=V_{DD}$
7. scanning direction C65 to C1
8. power booster stop
9. LCD power source ladder resisters directly

Note that resetting may make all bits of each register except MODE3 to MODE0 change during the operation. Re-set all of registers to re-display or re-operate.