LH5485
LH5495

Cascadeable 256 × 8 FIFO
Cascadeable 256 × 9 FIFO

FEATURES

- Fastest 256 × 8/9 Cascadeable FIFO 35/25/15 MHz
- Expandable in Word Width & FIFO Depth
- Almost-Full / Empty & Half-Full Flags
- Fully Independent Asynchronous Inputs & Outputs
- LH5485 Output Enable forces Data Outputs to High-Impedance State
- Pin Compatible & Cascadeable with LH5481/5491 64 × 8/9 FIFOs
- Industry Standard Pinout
- 28-Pin, 300-mil DIP & 28-Pin PLCC Packaging

FUNCTIONAL DESCRIPTION

The LH5485 and LH5495 are high performance, asynchronous First-In-First-Out (FIFO) memories organized 256 words deep by 8 or 9 bits wide. The 8-bit LH5485 has an Output Enable ($\overline{OE}$) function, which can be used to force the 8 data outputs (DO) to a high-impedance state. The LH5495 has 9 data outputs.

These FIFOs accept 8 or 9-bit data at the DI data inputs. A Shift In (SI) signal writes the DI data into the FIFO. A Shift Out (SO) signal shifts stored data to the DO outputs. The Output Ready (OR) signal indicates when valid data is present on the DO outputs.

If the FIFO is full and unable to accept more DI data IR will not return high and SI pulses will be ignored. If the FIFO is empty and unable to shift data to the DO outputs, OR will not return high and SO pulses will be ignored. The Almost-Full and Almost-Empty (AFE) flag is asserted (HIGH) when the FIFO is almost-full (248 words or more) or almost-empty (8 words or less). The Half-Full (HF) flag is asserted (HIGH) when the FIFO contains 128 words or more.

Reading and writing operations may be asynchronous, allowing these FIFOs to be used as buffers between digital machines of widely different operating frequencies. The high speed makes these FIFOs ideal for high performance communication and controller applications.

PIN CONNECTIONS

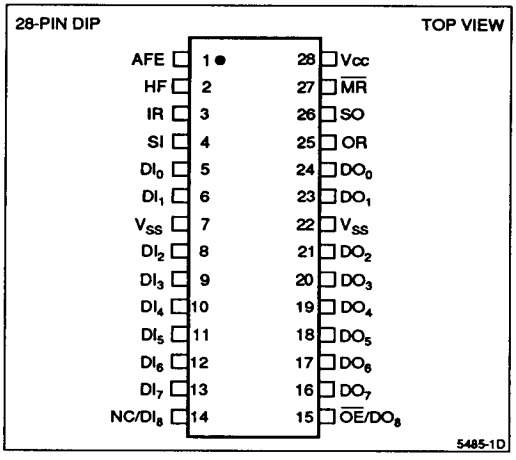

Figure 1. Pin Connections for DIP Package

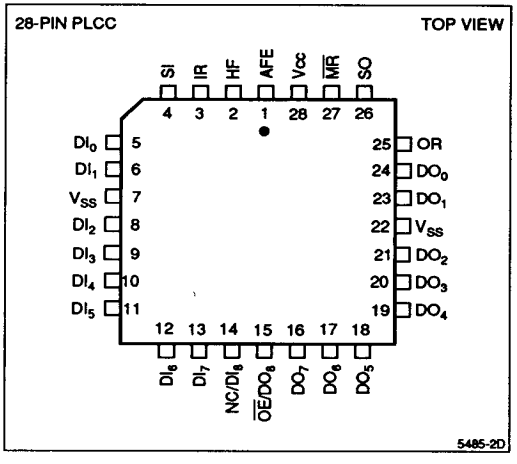

Figure 2. Pin Connections for PLCC Package

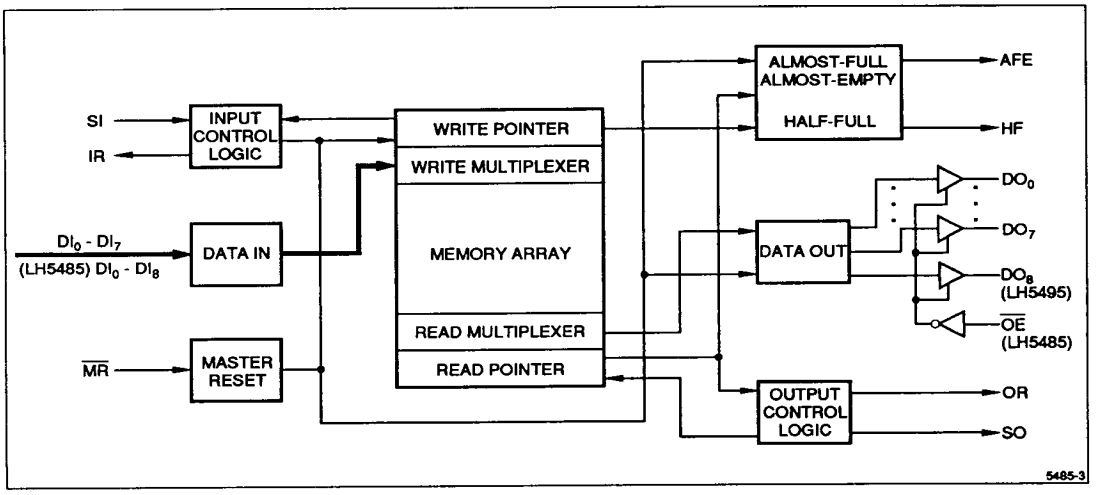

Figure 3. LH5485/95 Block Diagram

PIN DESCRIPTIONS

PIN	DESCRIPTION
$DI_0 - DI_8$	Data Inputs
$DO_0 - DO_8$	Data Outputs
SI	Shift In
SO	Shift Out
IR	Input Ready
OR	Output Ready

PIN	DESCRIPTION
HF	Half-Full Flag
AFE	Almost-Full / Almost-Empty
$\overline{MR}$	Master Reset
$\overline{OE}$	Output Enable (LH5485 only)
V_{CC}	Positive Power Supply
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS [1,2]

PARAMETER	RATING
Vcc Range	−0.5 V to 7 V
Input Voltage Range	−0.5 V to Vcc + 0.5 V (not to exceed 7 V)
DC Output Current [3]	± 40 mA
Storage Temperature	−65°C to 150°C
DC Voltage Applied To Outputs In High-Z state	−0.5 V to Vcc + 0.5 V (not to exceed 7 V)
Static Discharge Voltage [4]	> 2000 V
Power Dissipation (Package Limit)	1.0 W

NOTES:

1. All voltages are measured with respect to Vss.
2. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions above those indicated in the "Operating Range" of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
3. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.
4. Sample tested only.

OPERATING RANGE [1]

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
T_A	Temperature, Ambient	0.0	70	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{SS}	Ground	0.0	0.0	V
V_{IL}	Input Low Voltage (Logic "0") [2]	−0.5	0.8	V
V_{IH}	Input High Voltage (Logic "1")	2.0	Vcc + 0.5	V

NOTES:

1. All voltages are measured with respect to Vss.
2. FIFO inputs are able to withstand a −1.5 V undershoot for less than 10 ns per cycle.

DC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range, Unless Otherwise Noted)

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN	MAX	UNIT
I_{LI}	Input Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	−10	10	µA
I_{LO}	Output Leakage Current (High-Z)	V_{CC} = 5.5 V, V_{OUT} = 0 V to V_{CC}	−10	10	µA
V_{OH}	Output High Voltage	V_{CC} = 4.5 V, I_{OH} = −4 mA	2.4		V
V_{OL}	Output Low Voltage	V_{CC} = 4.5 V, I_{OL} = 8.0 mA		0.4	V
I_{CCQ}	Power Supply Quienscent Current	V_{CC} = 5.5 V, I_{OUT} = 0 mA $V_{IN} \le V_{IL}$, $V_{IN} \ge V_{IH}$		25	mA
I_{CC}	Power Supply Current [2]	fsi = 35 MHz, fso = 35 MHz		70	mA

NOTES:

1. All voltages are measured with respect to Vss.
2. Icc is dependent upon actual output loading and cycle rates. Specified values are with outputs open.

AC TEST CONDITIONS [1]

PARAMETER	RATING
Input Pulse Levels	0 to 3 V
Input Rise and Fall Times (10% / 90%)	Figure 4a
Input Timing Reference Levels	1.5 V
Output Timing Reference Levels	1.5 V
Output Load for AC Timing Tests	Figure 4b

NOTE:
1. All voltages are measured with respect to Vss.

CAPACITANCE [1,2]

PARAMETER	DESCRIPTION	TEST CONDITIONS	RATING
C_{IN}	Input Capacitance	T_A = 25°C, f = 1MHz, Vcc = 4.5 V	5 pF
C_{OUT}	Output Capacitance	TA = 25°C, f = 1MHz, Vcc = 4.5 V	7 pF

NOTES:
1. All voltages are measured with respect to Vss.
2. Sample tested only.

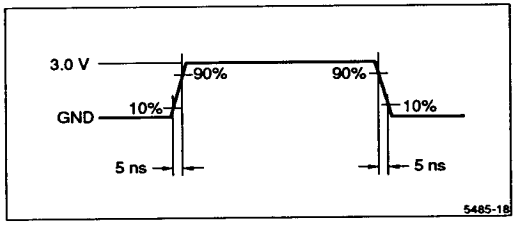

Figure 4a. Input Rise and Fall Times

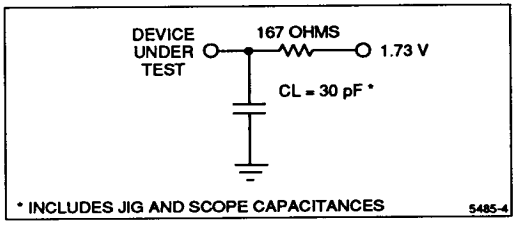

Figure 4b. Output Load Circuit

AC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range)

SYMBOL	PARAMETER	15MHz		25MHz		35MHz		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_O	Operating Frequency [2]		15		25		35	MHz
t_{PHSI}	SI HIGH Time [3,8]	15		11		9		ns
t_{PLSI}	SI LOW Time [3,8]	20		15		13		ns
t_{SSI}	Data Setup to SI [4]	–1		–1		–1		ns
t_{HSI}	Data Hold from SI [4]	14		12		10		ns
t_{DLIR}	Delay, SI HIGH to IR LOW		20		18		16	ns
t_{DHIR}	Delay, SI LOW to IR HIGH		24		20		18	ns
t_{PHSO}	SO HIGH Time [3]	15		11		9		ns
t_{PLSO}	SO LOW Time [3]	20		15		13		ns
t_{DLOR}	Delay, SO HIGH to OR LOW		20		18		16	ns
t_{DHOR}	Delay, SO LOW to OR HIGH		24		20		18	ns
t_{SOR}	Data Setup to OR HIGH	–1		–1		–1		ns
t_{HSO}	Data Hold from SO LOW	0		0		0		ns
t_{FT}	Fallthrough Time		40		34		30	ns
t_{BT}	Bubblethrough Time		28		26		25	ns
t_{SIR}	Data Setup to IR [5]	5		5		5		ns
t_{HIR}	Data Hold from IR [5]	5		5		5		ns
t_{PIR}	Input Ready Pulse HIGH [8]	7		7		7		ns
t_{POR}	Output Ready Pulse HIGH [8]	7		7		7		ns
t_{DLZOE}	OE LOW to LOW Z (LH5485) [6,9]		35		30		25	ns
t_{DHZOE}	OE HIGH to HIGH Z (LH5485) [6,9]		35		30		25	ns
t_{DHHF}	SI LOW to HF HIGH		45		45		40	ns
t_{DLHF}	SO LOW to HF LOW		45		45		40	ns
t_{DLAFE}	SO or SI LOW to AFE LOW		45		45		40	ns
t_{DHAFE}	SO or SI LOW to AFE HIGH		45		45		40	ns
t_{PMR}	$\overline{MR}$ Pulse Width	35		35		35		ns
t_{DSI}	$\overline{MR}$ HIGH to SI HIGH		25		25		22	ns
t_{DOR}	$\overline{MR}$ LOW to OR LOW [7]		25		25		20	ns
t_{DIR}	$\overline{MR}$ LOW to IR HIGH [7]		25		25		20	ns
t_{LXMR}	$\overline{MR}$ LOW to Output LOW [7]		25		25		20	ns
t_{AFE}	$\overline{MR}$ LOW to AFE HIGH		30		30		30	ns
t_{HF}	$\overline{MR}$ LOW to HF LOW		30		30		30	ns

NOTES:

1. All time measurements performed at "AC Test Conditions".
2. $f_O = f_{SI} = f_{SO}$.
3. $t_{PHSI} + t_{PLSI} = t_{PHSO} + t_{PLSO} = 1/f_O$.
4. t_{SSI} and t_{HSI} apply when memory is not full.
5. t_{SIR} and t_{HIR} apply when memory is full and SI is HIGH.
6. High-Z transitions are referenced to the steady-state V_{OH} – 500 mV and V_{OL} + 500 mV levels on the output.
7. After reset goes LOW, all Data outputs will be at LOW level, IR goes HIGH and OR goes LOW.
8. Common dash number devices are guaranteed by design to function properly in a cascaded configuration.
9. Sample tested only.

OPERATIONAL DESCRIPTION

Unlike earlier versions of FIFOs, the LH5485 and LH5495 use dual-port Random-Access-Memory, write and read pointers, and special control logic. The write pointer is incremented by the falling edge of the Shift In (SI) signal, while the read pointer is incremented by the falling edge of the Shift Out (SO) signal. The Input Ready (IR) signal enables data writing to the FIFO, while Output Ready (OR) indicates valid read information is available on the Data Output (DO) pins.

Resetting the FIFO

The FIFO must be reset, upon Power-Up, using the Master Reset ($\overline{MR}$) signal. This causes the FIFO to enter an empty state, indicated by the Output Ready (OR) being LOW and Input Ready (IR) being HIGH. All Data Output (DO) pins will be LOW in this state. The AFE flag will be HIGH and the HF flag will be LOW.

If Shift In (SI) is HIGH, when the Master Reset ($\overline{MR}$) signal is ended, then the data on the Data Input (DI) pins will be written into the FIFO and Input Ready (IR) will return LOW until Shift In (SI) is brought LOW.

If Shift In (SI) is LOW when the Master Reset ($\overline{MR}$) is ended, then Input Ready (IR) will go HIGH, but the data on the Data Input (DI) pins will not enter the FIFO until Shift In (SI) goes HIGH.

Shifting Data In

Data Input (DI) is shifted into the FIFO on the rising edge of Shift In (SI). This loads input data into the FIFO and causes Input Ready (IR) to go LOW. When a falling edge of Shift In (SI) occurs, the write pointer increments to the next word position and Input Ready (IR) goes HIGH, indicating that the FIFO is ready to accept new data. When the FIFO is full, Input Ready (IR) remains LOW after the negative edge of Shift In (SI) signal; Shift Out (SO) action is required to unload a word of data and bring Input Ready (IR) HIGH – see Bubblethrough description.

Shifting Data Out

Data is shifted out of the FIFO on the falling edge of Shift Out (SO). The read pointer increments to the next word location and FIFO data, if present, will appear on the Data Output (DO) pins and the Output Ready (OR) signal will go HIGH. If FIFO data is not present, Output Ready (OR) will stay LOW, indicating the FIFO is empty; in this case, the last valid data read from the FIFO will remain on the Data Output (DO) pins. When the FIFO is not empty, Output Ready (OR) will go LOW after the rising edge of Shift Out (SO). The previous data remains on the Data Output (DO) pins until a falling edge of Shift Out (SO).

Fallthrough Condition

When the FIFO is empty, a data word entering through the Shift In (SI) action will follow one of two sequences.

If Shift Out (SO) is LOW, the data will propagate to the Data Output (DO) pins and Output Ready (OR) will go HIGH and stay HIGH until the next rising edge of Shift Out (SO).

If Shift Out (SO) is held HIGH while data is shifted into an empty FIFO (as occurs in depth cascading of FIFOs), data will propagate to the Data Output (DO) pins and Output Ready (OR) will pulse HIGH for a minimum time duration specified by t_{POR} and then go back LOW again. The stored word will remain on the Data Output (DO) pins. If more words are written into the FIFO, they will line up behind the first word and not appear on the Data Output (DO) pins until Shift Out (SO) has returned LOW.

Bubblethrough Condition

When the FIFO is full, Shift Out (SO) action will initiate one of the following two sequences.

If Shift In (SI) is LOW, Input Ready (IR) will go HIGH and stay HIGH until the next rising edge of Shift In (SI).

If Shift In (SI) is held HIGH while data is shifted out of a full FIFO (as occurs in depth cascading of FIFOs), Input Ready (IR) will pulse HIGH for a minimum time duration specified by t_{PIR} and then go back LOW again. Special Data Input (DI) setup and hold times (t_{SIR} and t_{HIR}, respectively) are defined for this condition.

TIMING DIAGRAMS

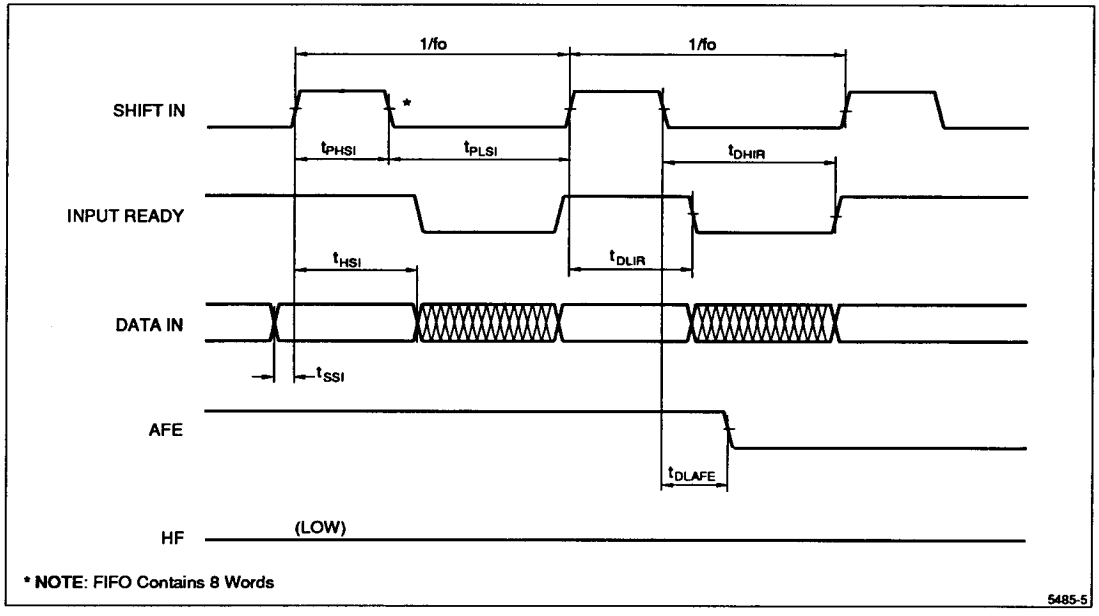

Figure 5. Data In Timing

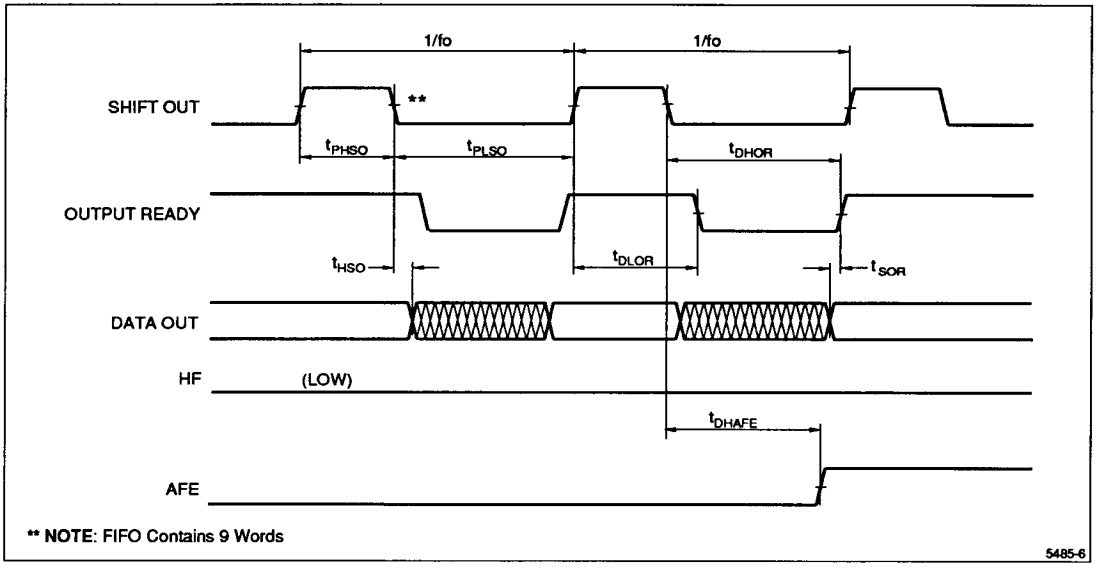

Figure 6. Data Out Timing

TIMING DIAGRAMS (cont'd)

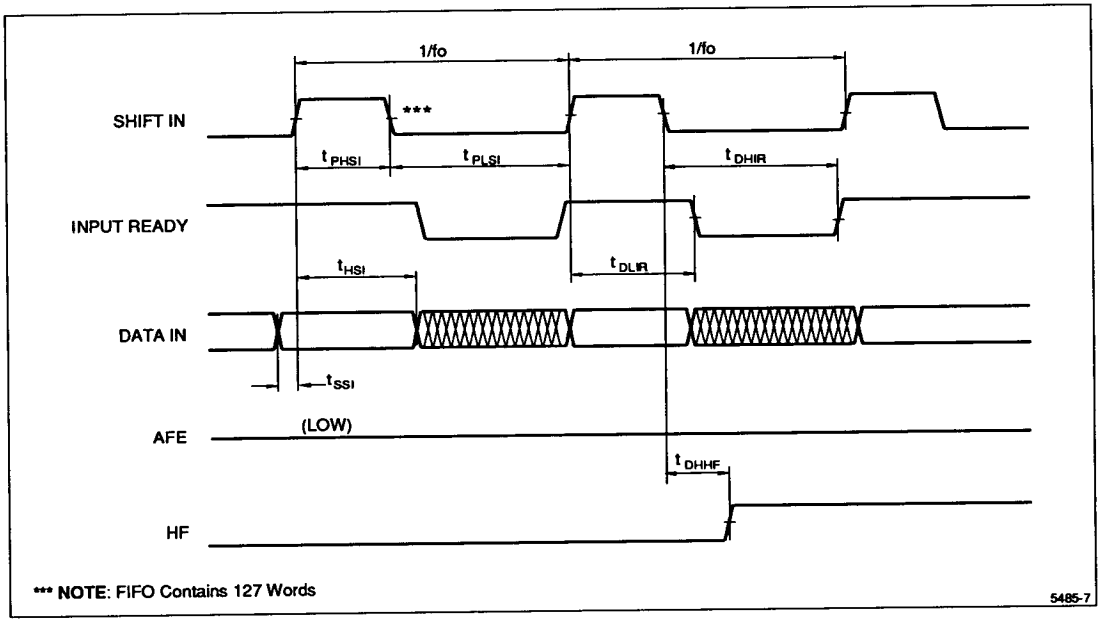

Figure 7. Data In Timing

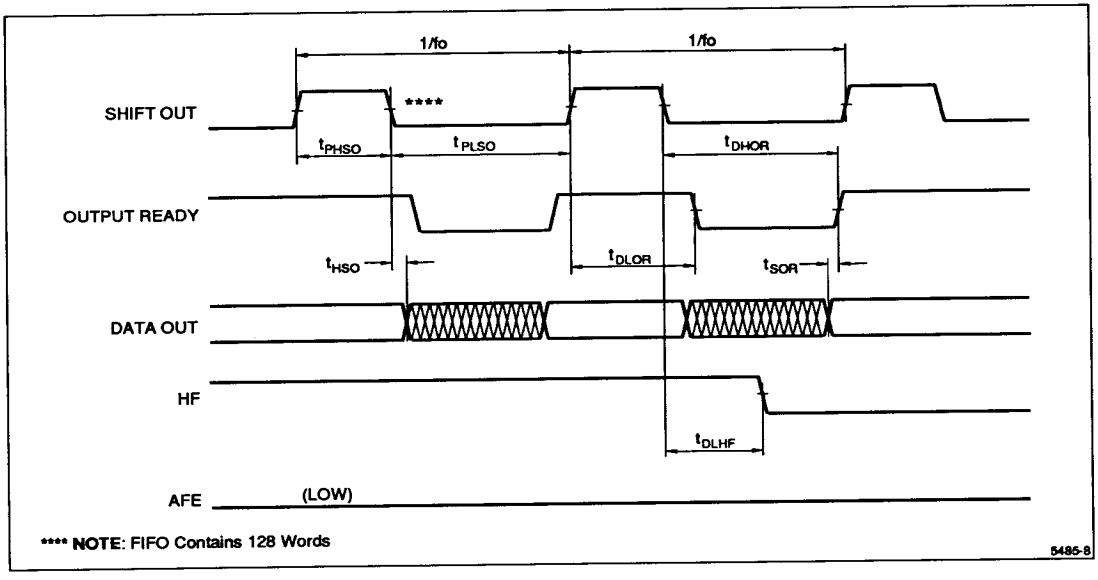

Figure 8. Data Out Timing

TIMING DIAGRAMS (cont'd)

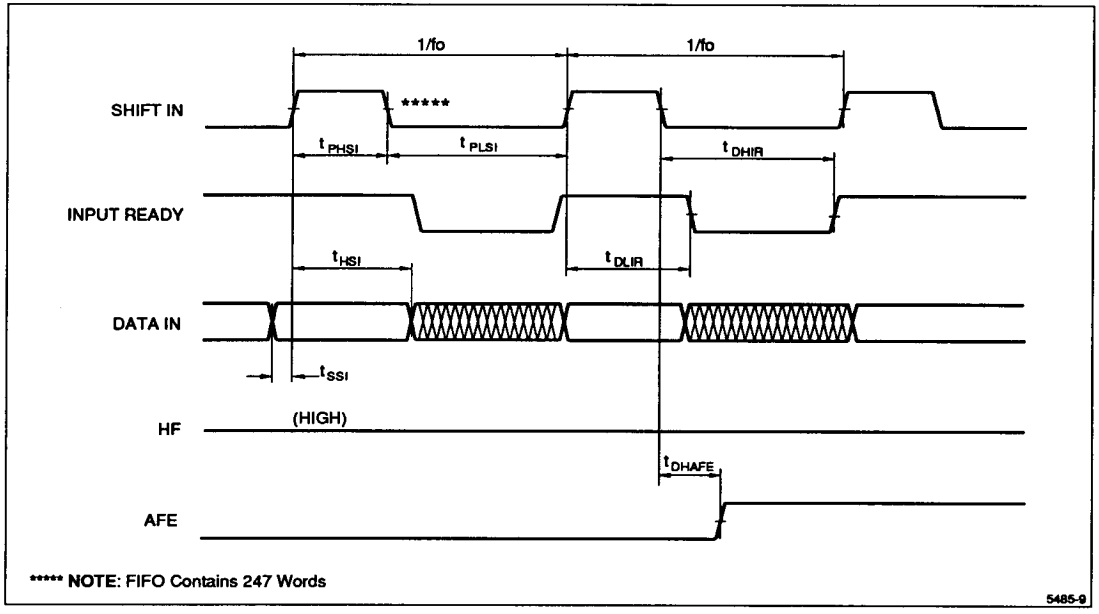

Figure 9. Data In Timing

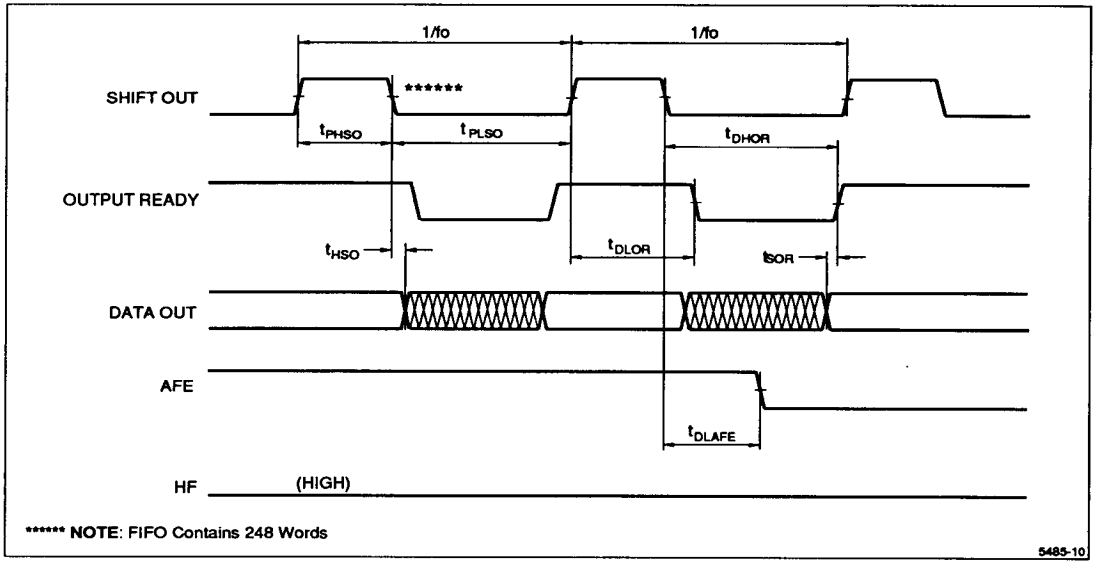

Figure 10. Data Out Timing

TIMING DIAGRAMS (cont'd)

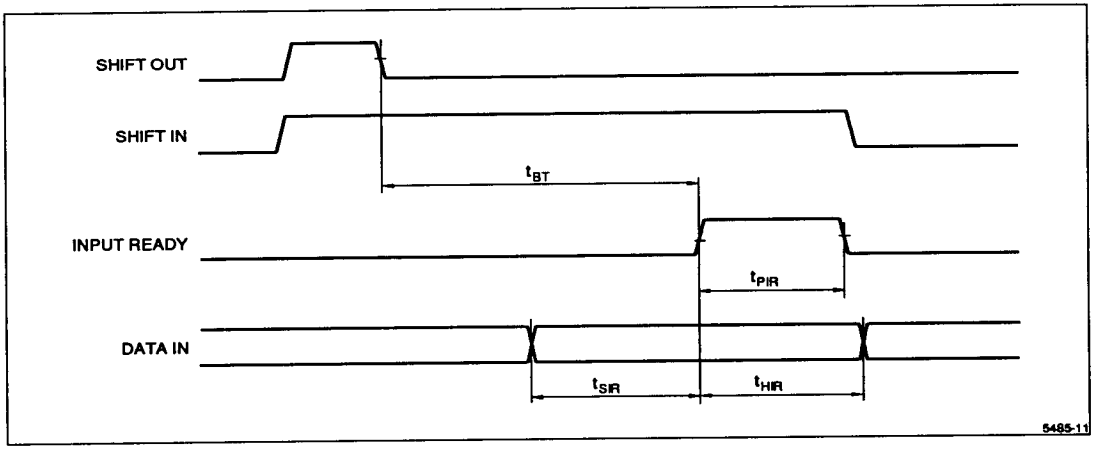

Figure 11. Bubblethrough Timing (Reading a Full FIFO)

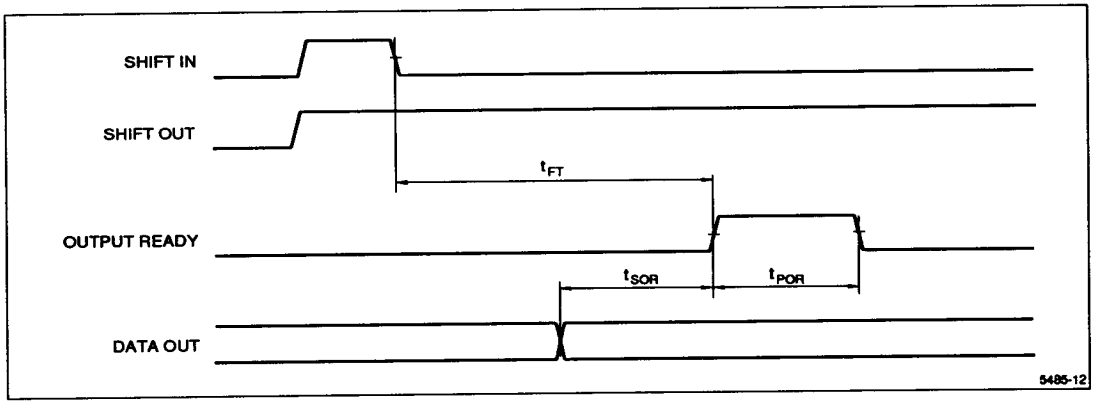

Figure 12. Fallthrough Timing (Writing an Empty FIFO)

TIMING DIAGRAMS (cont'd)

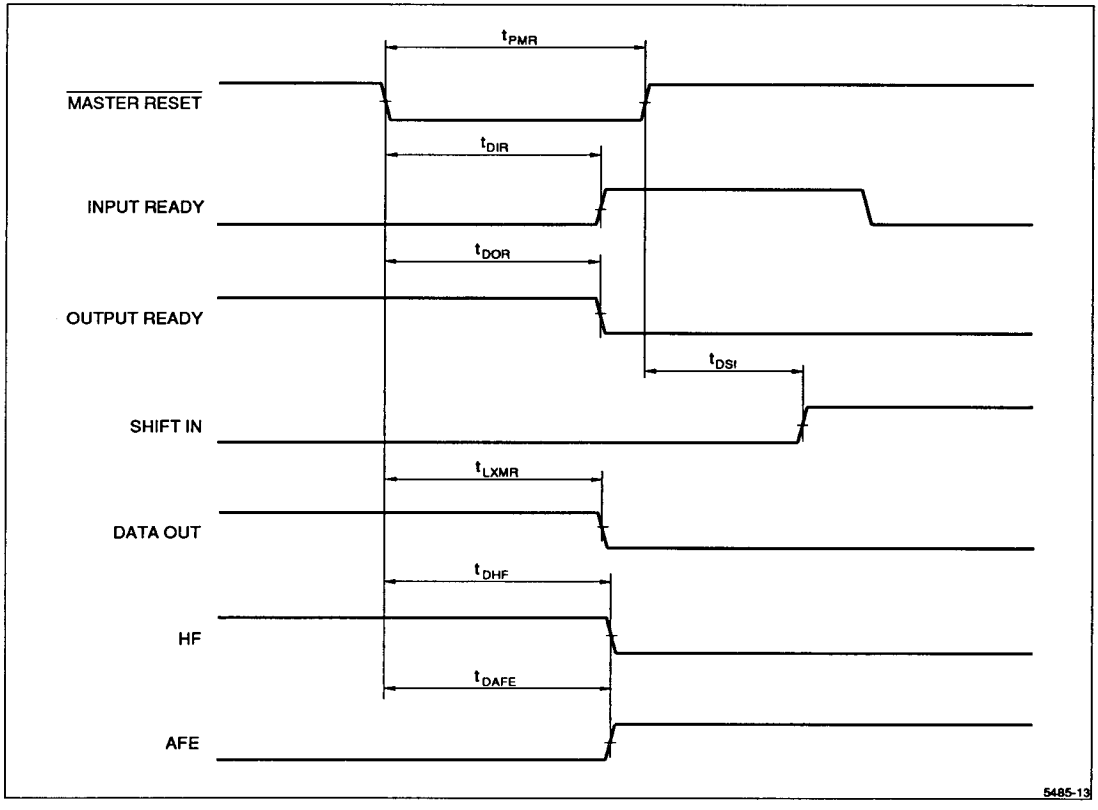

Figure 13. Master Reset Timing

TIMING DIAGRAMS (cont'd)

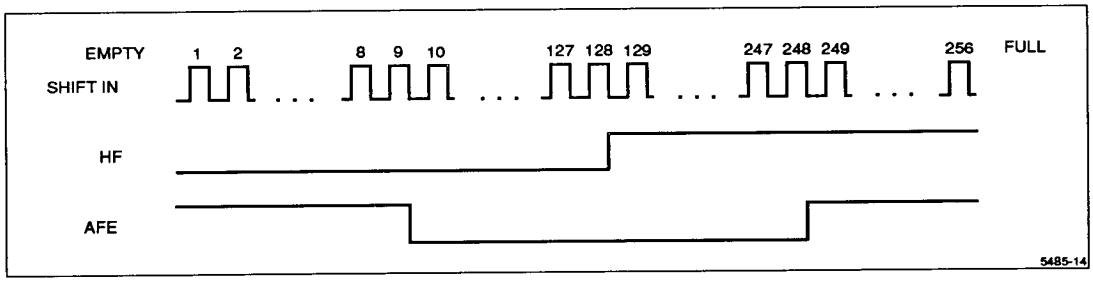

Figure 14. Shifting Words In

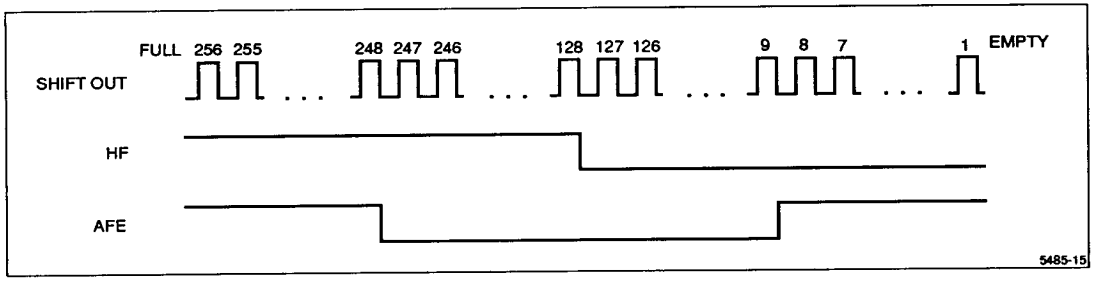

Figure 15. Shifting Words Out

FIFO EXPANSION

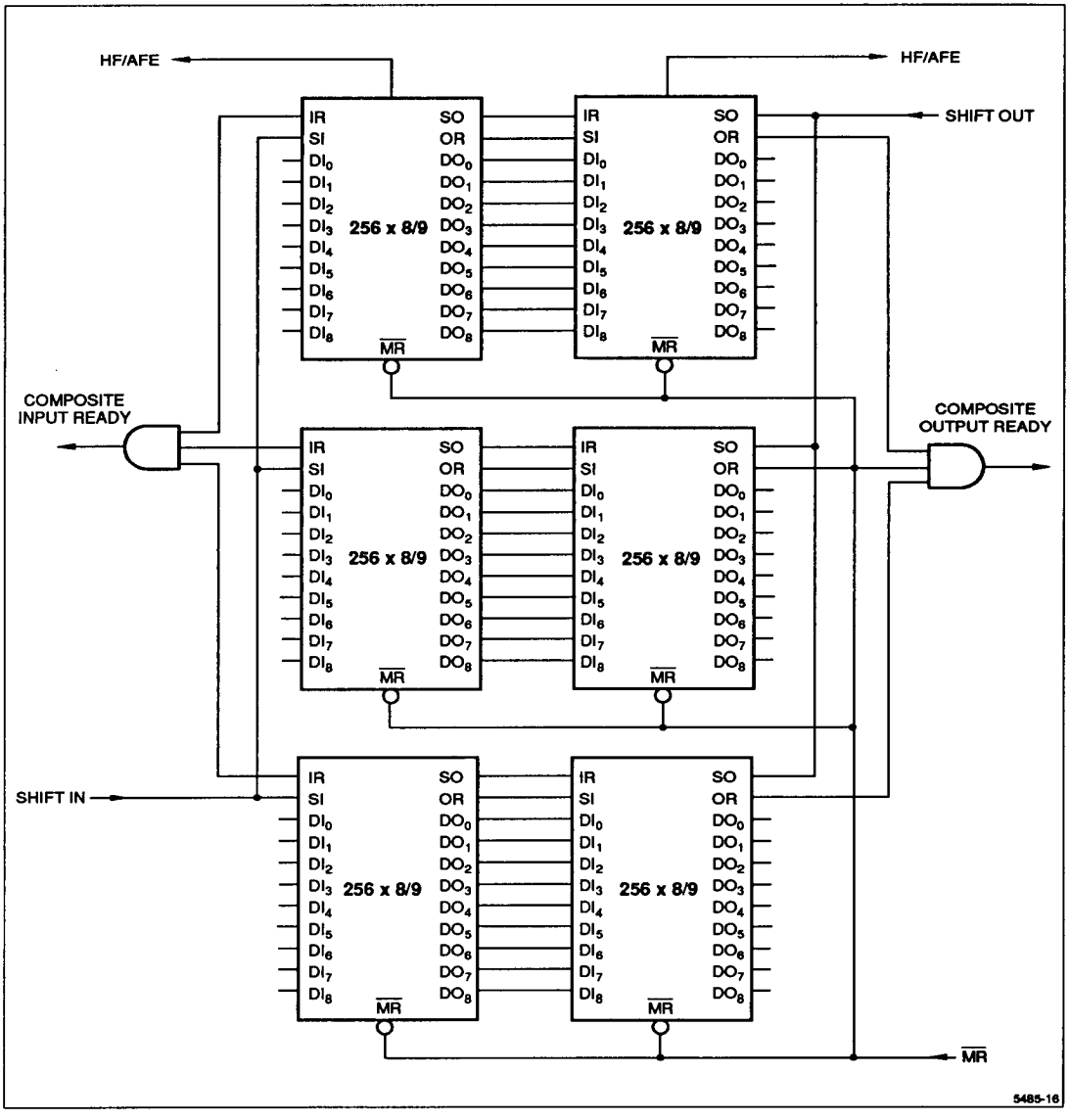

Figure 16. 512 × 24/27 Configuration Using 256 × 8/9 (LH5485/95) FIFOs.

FIFO EXPANSION (cont'd)

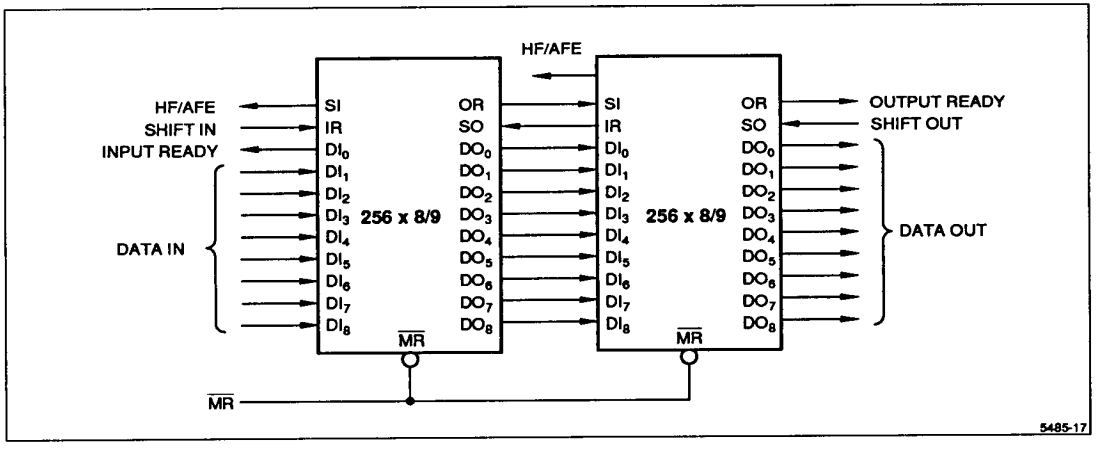

Figure 17. 512 × 8/9 Configuration

FIFOs are expandable in depth and width. However, in forming wider words, external logic is required to generate composite Input and Output Ready flags. This is due to the variation of delays of the FIFOs. The example circuit in Figure 16 uses simple AND gates as the external IR and OR generators. More complex logic may be required if fallthrough and bubblethrough pulses are needed by the external system.

FIFOs can easily cascaded to any desired depth as illustrated in Figure 17. The handshaking and associated timing between the FIFOs are handled by the inherent timing of the devices.

NOTES:

1. When the memory is empty the last word read will remain on the outputs until the master reset is strobed or a new data word bubbles through to the output. However, OR will remain LOW, indicating data at the output is not valid.
2. When the output data changes as a result of a pulse on SO, the OR signal always goes LOW before there is any change in output data and stays LOW until the new data has appeared on the outputs. Anytime OR is HIGH, there is valid stable data on the outputs.
3. All SHARP FIFOs will cascade with other SHARP FIFOs of the same architecture (i.e., 64 × 8/9 with 64 × 8/9 or 64 × 8/9 with 256 × 8/9). However, they may not cascade with FIFOs from other manufacturers.

ORDERING INFORMATION