- ☐ Low power dissipation:
  28 mW max-Standby
  19 mW max-Self refresh
- ☐ TTL-compatible
- ☐ 28-pin SRAM/ROM/EPROM compatible packa
- ☐ Built-in refresh multiplexer and refresh address
  counter
- ☐ Power-down self-refresh mode
- ☐ Automatic precharge allows cycle time to be in
  pendent of system skews
- ☐ Latched address, CS, and $\overline{OE}$ functions allow
  on multiplexed address/data bus
- ☐ Read, early write, late write, external refresh, p
  refresh, and self-refresh cycles

Performance Ranges
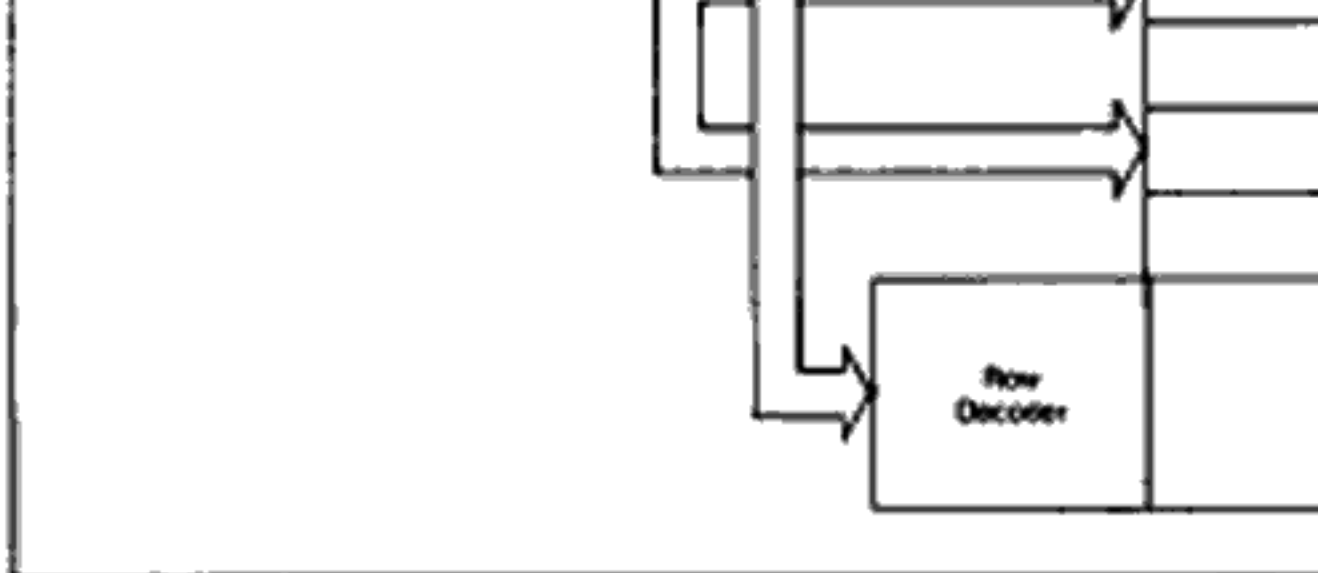
Device	t_{CEA}	t_{OEA}	t_C	
µPD4168C-12	120 ns	45 ns	220 ns	65
µPD4168C-15	150 ns	55 ns	260 ns	60
µPD4168C-20	200 ns	70 ns	330 ns	55

	H	C'	H
Early write	H	C'	H
Late Write	H	C'	H
External refresh	H	C'	H
	H	C'	L
Pulse refresh	C'	H	X
	C'	C'	H
	C'	C'	H
	C'	C'	H
	C'	C'	H
Power down self-refresh	L	H	X
Standby	H	H	X

H = V_{IH}, L = V_{IL}, C' = negative edge of clock pulse, X = V_{IH} or V_{IL}

Note:
(1) Depends on previous cycle

Absolute Maximum Ratings

Voltage on any pin relative to GND	-1.0
Operating temperature, T_{OPR}	0
Storage temperature, T_{STG}	-55 t
Short circuit output current, I_{OS}	
Power dissipation, P_D	

Comment: Exposing the device to stresses above those listed
lute Maximum Ratings could cause permanent damage. The
not meant to be operated under conditions outside the l
scribed in the operational sections of the specification. Exp
absolute maximum rating conditions for extended periods m
device reliability.

Access time from CE	t_{CEA}	
Data off time from $\overline{CE}$	t_{CEZ}	
Access time from $\overline{OE}$	t_{OEA}	
Data off time from $\overline{OE}$	t_{OEZ}	
$\overline{CE}$ pulse width	t_{CE}	120
$\overline{CE}$ precharge time	t_P	90
Address setup time to $\overline{CE}$	t_{ASC}	0
Address hold time from $\overline{CE}$	t_{AHC}	35
CS setup time to $\overline{CE}$	t_{CSC}	0
CS hold time from $\overline{CE}$	t_{CHC}	35
Data setup time to $\overline{CE}$, early write	t_{DSC}	-10
Data hold time from $\overline{CE}$, early write	t_{DHC}	90
Data setup time to $\overline{WE}$, late write	t_{DSW}	0
Data hold time from $\overline{WE}$, late write	t_{DHW}	50
$\overline{WE}$ setup time to $\overline{CE}$, early write	t_{WSC}	-30
$\overline{WE}$ hold time from $\overline{CE}$, early write	t_{WHC}	90
$\overline{WE}$ pulse duration	t_{WO}	60
$\overline{CE}$ hold time from $\overline{WE}$, late write	t_{CHW}	90
$\overline{WE}$ setup time to $\overline{CE}$, read cycle	t_{RCS}	0
$\overline{WE}$ hold time from $\overline{CE}$, read cycle	t_{RCH}	0
$\overline{CE}$ hold time from $\overline{OE}$, read cycle	t_{CHO}	45
$\overline{OE}$ setup time to $\overline{CE}$, write cycle	t_{OES}	0
$\overline{OE}$ hold time from $\overline{CE}$, write cycle	t_{OEH}	0

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(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring inp

(5) Load = 2 TTL loads and 50 pF.

(6) t_{CEZ} (max) and t_{OEZ} (max) define the time at which the output

(7) $t_{WSC} \leqslant t_{WSC}$ (min), the cycle is a late write cycle.

(8) A power down self-refresh cycle is initiated when the $\overline{RFSH}$ i

Figure 1. Power-up Dummy Cycles

Pulse Refresh Cycle after Read Cycle Comple[