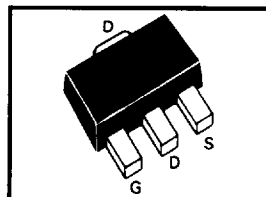


SOT89 N CHANNEL ENHANCEMENT MODE VERTICAL DMOS FET

ZVN4206Z

PARTMARKING DETAIL – ZVN4206Z – N26

* FOR TYPICAL CHARACTERISTIC GRAPHS SEE
ZVN4206G DATASHEET



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Drain-Source Voltage	V_{DS}	60	V
Continuous Drain Current @ $T_{amb}=25^{\circ}\text{C}$	I_D	0.9	A
Pulsed Drain Current	I_{DM}	8	A
Gate-Source Voltage	V_{GS}	± 20	V
Max Power Dissipation @ $T_{amb}=25^{\circ}\text{C}$	P_{TOT}	1.5	W
Operating And Storage Temperature Range	$t_j:t_{stg}$	-55 TO +150	$^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS (at $T_{amb}=25^{\circ}\text{C}$ unless otherwise stated)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS.
Drain-Source Breakdown Voltage	BV_{DSS}	60			V	$I_D=1\text{mA}$, $V_{GS}=0$
Gate-Source Threshold Voltage	$V_{GS(TH)}$	1.3		3	V	$I_D=1\text{mA}$, $V_{DS}=V_{GS}$
Gate Body Leakage	I_{GSS}			100	nA	$V_{GS}=\pm 20\text{V}$, $V_{DS}=0$
Zero Gate Voltage Drain Current (2)	I_{DSS}			10 100	μA μA	$V_{DS}=\text{max rating}$, $V_{GS}=0$ $V_{DS}=0.8 \times \text{max. rating}$, $V_{GS}=0$ ($T=125^{\circ}\text{C}$)
On-State Drain Current *	$I_{D(ON)}$	3			mA	$V_{DS}=25\text{V}$, $V_{GS}=10\text{V}$
Static Drain-Source On-State Resistance *	$R_{DS(ON)}$			1 1.5	Ω Ω	$I_D=1.5\text{A}$, $V_{GS}=10\text{V}$ $I_D=0.5\text{A}$, $V_{GS}=5\text{V}$
Forward Transconductance (2)	G_{FS}	0.3			S	$V_{DS}=25\text{V}$, $I_D=250\text{mA}$
Input Capacitance (2)	C_{ISS}			100	pF	$V_{DS}=25\text{V}$, $V_{GS}=0$ $f=1\text{MHz}$
Common Source Output Capacitance (2)	C_{OSS}			60	pF	
Reverse Transfer Capacitance (2)	C_{RSS}			20	pF	
Turn-On Delay Time (1) (2)	$T_{D(ON)}$			8	ns	$V_{DD}=25\text{V}$, $I_D=250\text{mA}$
Rise Times (1) (2)	T_R			12	ns	
Turn-Off Delay Time (1) (2)	$T_{D(OFF)}$			12	ns	
Fall Time (1) (2)	T_F			15	ns	

DRAIN-SOURCE DIODE CHARACTERISTICS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS.
Forward on voltage *	V_{SD}		0.85		V	$V_{GS}=0$, $I_S=-0.6\text{A}$
Reverse Recovery Time	T_{RR}		70		ns	$V_{GS}=0$, $I_F=0.6$ $I_R=0.1\text{A}$

(1) Switching times measured with 50Ω source impedance and $<5\text{ns}$ rise time on a pulse generator.

(2) Sample test.

(3) Measured under pulsed conditions. Pulse width=300 μs . Duty cycles $\leq 2\%$.

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