

DATA SHEET

ABT22V10-7 (COMMERCIAL)

ABT22V10A/B (MILITARY)

Low noise, high drive, metastable immune,
PLD

Product specification (Commercial)
Preliminary specification (Military)

April 22, 1994
March 1994

Philips Semiconductors



PHILIPS

Low noise, high drive, metastable immune, PLD

ABT22V10-7

DESCRIPTION

The ABT22V10 is a versatile PAL® device fabricated with the Philips BiCMOS process known as QUBiC. The QUBiC process produces a very high speed device (7.5ns worst case) which has excellent noise characteristics. The ground bounce, with 9 outputs switching and the 10th held low is less than 0.8V (see page 10).

The ABT22V10 is designed so the outputs can never display a metastable state due to set up and hold time violations. If set up and hold times are violated, the outputs will not glitch or display a metastable state (the propagation delays may, however, be extended).

The ABT22V10 uses the familiar AND/OR logic array structure, which allows direct implementation of sum-of-product equations. This device has a programmable AND array which drives a fixed OR array. The AND array is programmed to create custom product terms while the fixed OR array sums selected terms at the output.

The OR sum of the products feeds the "Output Macro Cell" (OMC), which can be individually configured as a dedicated input, a combinatorial output, or a registered output with internal feedback. In other words, the architecture provides maximum design flexibility by allowing the Output Macro Cell to be configured by the user.

This device is pin and JEDEC file compatible with industry standard 22V10 and can be used in all standard applications where speed is to be maximized.

FEATURES

- Ultra fast 7.5ns t_{PD} and 6ns t_{CO}
- High output drive; 48mA = I_{OL} (complete specification, page 3)
- Metastable immune flip-flops, $\tau = 83pS$ (complete specification, page 9)

- Low ground bounce (<0.8V)
- Varied product term distribution with up to 16 product terms per output for complex functions
- Programmable output polarity
- Power-up reset on all registers
- Synchronous Preset/Asynchronous Reset
- Programmable on standard PAL-type device programmers
- Design support provided using SNAP software development package and other CAD tools for PLDs
- Available in 300mil-wide 24-Pin Plastic small outline package
- Military conditions supported (see page 18).

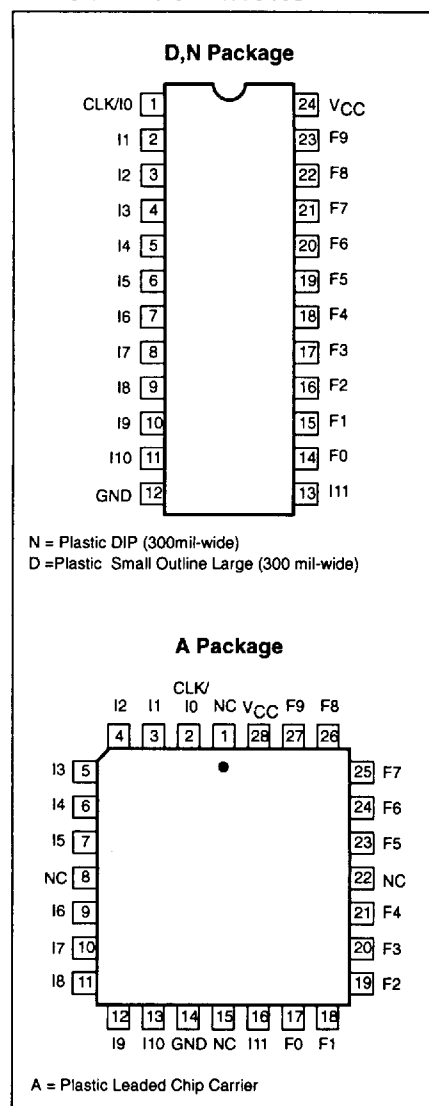
APPLICATIONS

- DMA control
- State machine implementation
- High speed graphics processing
- Counters/shift registers
- SSI/MSI random logic replacement
- High speed memory decoder

PIN LABEL DESCRIPTIONS

I1 – I11	Dedicated Input
NC	Not Connected
F0 – F9	Macro Cell Input/Output
CLK/I0	Clock Input/Dedicated Input
V _{CC}	Supply Voltage
GND	Ground

PIN CONFIGURATIONS



ORDERING INFORMATION

DESCRIPTION	ORDER CODE	DRAWING NUMBER
24-Pin Plastic Dual-In-Line Package 300mil-wide	ABT22V10-7N	0410D
28-Pin Plastic Leaded Chip Carrier	ABT22V10-7A	0401F
24-Pin Plastic Small Outline Large	ABT22V10-7D	0173D

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ABSOLUTE MAXIMUM RATINGS¹

SYMBOL	PARAMETER	RATINGS		UNIT
		MIN	MAX	
V _{CC}	Supply voltage	-0.5	+7.0	V _{DC}
V _{IN}	Input voltage	-1.2	V _{CC} + 0.5	V _{DC}
V _{OUT}	Output voltage	-0.5	V _{CC} + 0.5	V _{DC}
I _{IN}	Input currents	-30	+30	mA
I _{OUT}	Output currents		+100	mA
T _{stg}	Storage temperature range	-65	+150	°C

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

NOTE:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

OPERATING RANGES

SYMBOL	PARAMETER	RATINGS		UNIT
		MIN	MAX	
V _{CC}	Supply voltage	+4.75	+5.25	V _{DC}
T _{amb}	Operating free-air temperature	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS (OVER OPERATING RANGES)

SYMBOL	PARAMETER	TEST CONDITIONS ¹	LIMITS		UNIT
			MIN	MAX	
Input voltage					
V _{IL}	Low	V _{CC} = MIN		0.8	V
V _{IH}	High	V _{CC} = MAX	2.0		V
V _I	Clamp	V _{CC} = MIN, I _{IN} = -18mA		-1.2	V
Output voltage					
V _{OL}	Low	V _{CC} = MIN, V _{IN} = V _{IH} or V _{IL} I _{OL} = 48mA		0.5	V
V _{OH}	High	I _{OH} = -16 mA	2.4		V
Input current					
I _{IL}	Low	V _{CC} = MAX, V _{IN} = 0.40V		-10	μA
I _{IH}	High	V _{CC} = MAX, V _{IN} = 2.7V		10	μA
Output current					
I _{OL}	Low	V _{CC} = MIN V _{IN} or V _{IL} V _{OL} = .5 (MAX)		48	mA
I _{OH}	High	V _{OH} = 2.4 (MIN)		-16	mA
I _{OZH}	Output leakage ²	V _{CC} = MAX V _{IN} = V _{IL} or V _{IH} , V _{OUT} = 2.7V		100	μA
I _{OZL}	Output leakage ²	V _{IN} = V _{IL} or V _{IH} , V _{OUT} = 0.4V		-100	μA
I _{SC}	Short circuit ³	V _{OUT} = 0.5 V	-30	-190	mA
I _{CC}	V _{CC} supply current	V _{CC} = MAX		170	mA

NOTES:

1. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
 2. I/O pin leakage is the worst case of I_{OZX} or I_{IX} (where X = H or L).
 3. No more than one output should be tested at a time. Duration of the short-circuit test should not exceed one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.

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AC ELECTRICAL CHARACTERISTICS

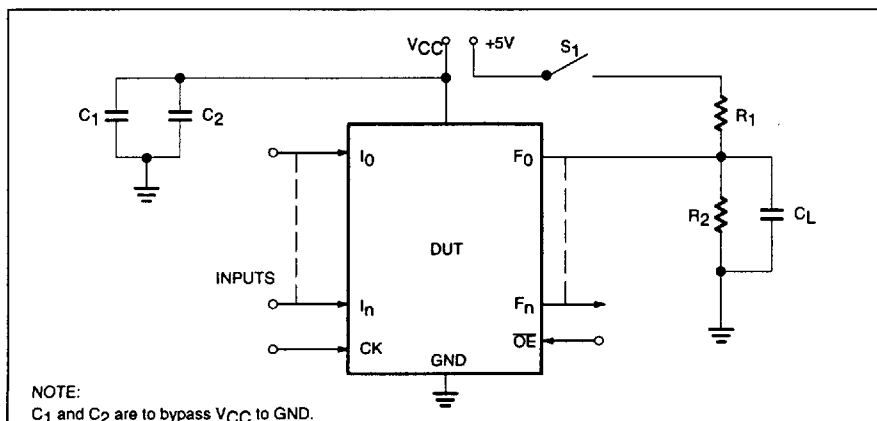
Over commercial operating range unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS ¹			UNIT
			MIN	TYP	MAX	
t_{PD}	Input or feedback to non-registered output ²	Active-LOW			7.5	
		Active-HIGH			7.5	ns
t_S	Setup time from input, feedback or SP to Clock		5.5			ns
t_H	Hold time		0			ns
t_{CO}	Clock to output ⁷				6.0/6.5	ns
t_{CF}	Clock to feedback ³				2.5	ns
t_{AR}	Asynchronous Reset to registered output				10.0	ns
t_{ARW}	Asynchronous Reset width		7.5			ns
t_{ARR}	Asynchronous Reset recovery time		5.5			ns
t_{SPR}	Synchronous Preset recovery time		5.0			ns
t_{WL}	Width of Clock LOW		3.0			ns
t_{WH}	Width of Clock HIGH		3.0			ns
f_{MAX}	Maximum frequency; External feedback $1/(t_S + t_{CO})^{4,7}$		87/83			MHz
	Maximum frequency; Internal feedback $1/(t_S + t_{CF})^4$		125			MHz
t_{EA}	Input to Output Enable ⁵				7.5	ns
t_{ER}	Input to Output Disable ⁵				7.5	ns
Capacitance⁶						
C_{IN}	Input Capacitance (Pin 1)	$V_{IN} = 2.0V$	$V_{CC} = 5.0V$ $T_{amb} = 25^\circ C$		6	pF
	Input Capacitance (Others)	$V_{IN} = 2.0V$			6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 2.0V$	$f = 1MHz$		8	pF

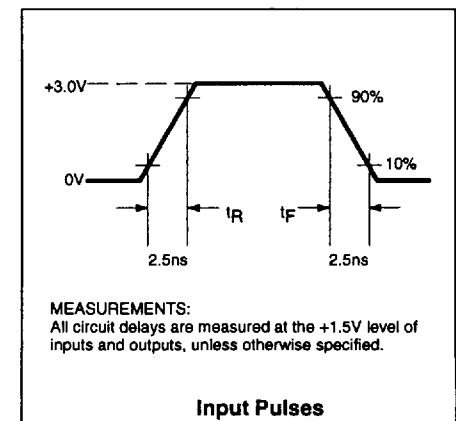
NOTES:

- Commercial Test Conditions: $R_1 = 300\Omega$, $R_2 = 390\Omega$ (see Test Load Circuit).
- t_{PD} is tested with switch S_1 closed and $C_L = 50pF$ (including jig capacitance). $V_{IH} = 3V$, $V_{IL} = 0V$, $V_T = 1.5V$.
- Calculated from measured f_{MAX} internal.
- These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
- For 3-State output; output enable times are tested with $C_L = 50pF$ to the 1.5V level, and S_1 is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with $C_L = 5pF$. High-to-High impedance tests are made to an output voltage of $V_T = (V_{OH} - 0.5V)$ with S_1 open, and Low-to-High impedance tests are made to the $V_T = (V_{OL} + 0.5V)$ level with S_1 closed.
- These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.
- For PLCC package, $t_{CO}=6.0ns$; for DIP and SOL package, $t_{CO}=6.5ns$

TEST LOAD CIRCUIT



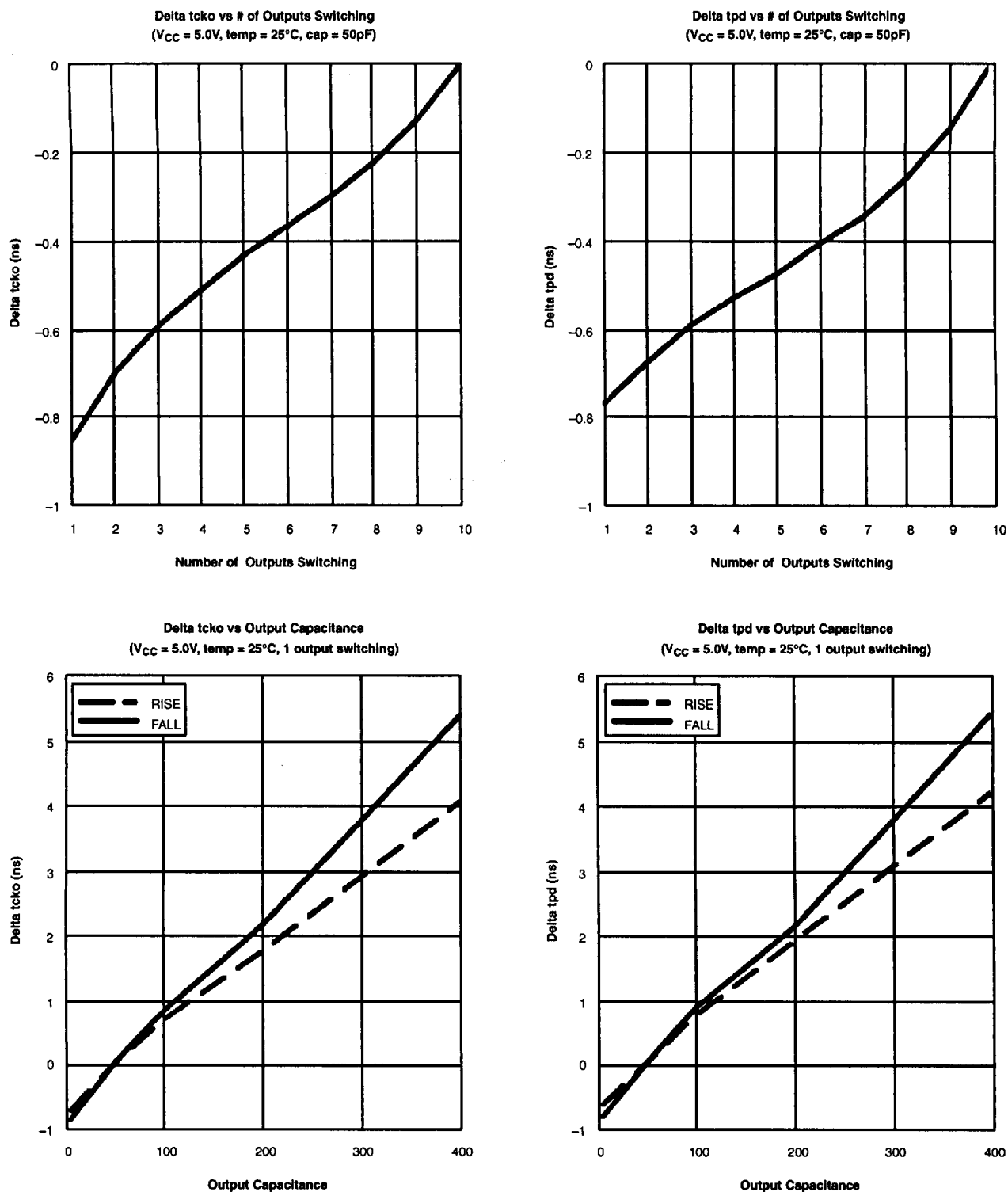
VOLTAGE WAVEFORM



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TIMING CHARACTERIZATION



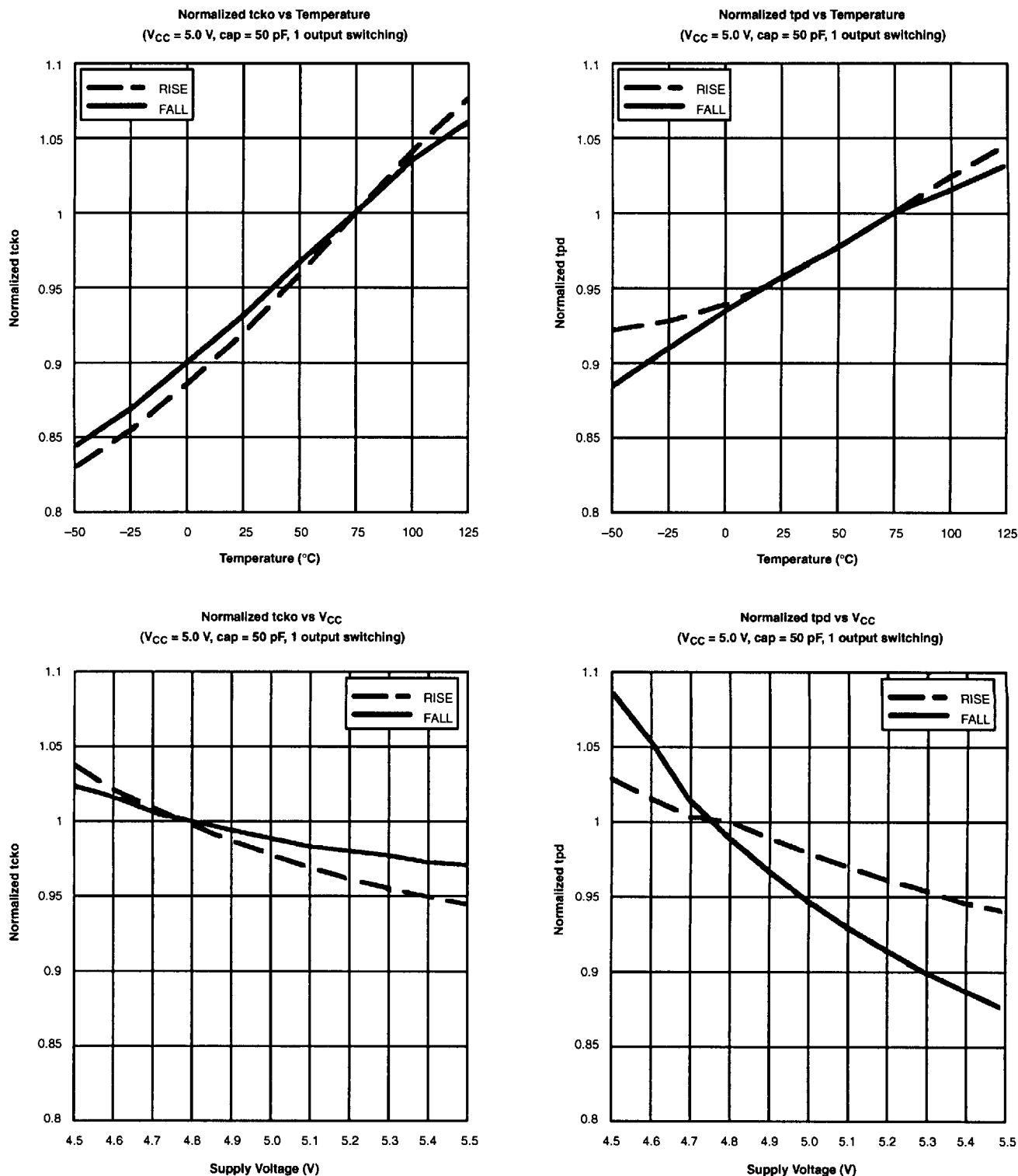
The timing characterization represents the average values of a representative sample for each parameter. The data can be used to derate the MAX AC CHARACTERIZATION based upon the specific user design. Philips guarantees the MAX AC CHARACTERIZATION specifications.

Figure 1. Device Characterization

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TIMING CHARACTERIZATION



The timing characterization represents the average values of a representative sample for each parameter. The data can be used to derate the MAX AC CHARACTERIZATION based upon the specific user design. Philips guarantees the MAX AC CHARACTERIZATION specifications.

Figure 1. Device Characterization (continued)

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PRODUCT FEATURES

Metastable Immune Flip-flops

The D-type flip-flops have been designed such that the outputs will not glitch or display an output anomaly if the input set up or hold times are violated. Based on a τ of < 90 pS, and sampling the output 8ns after the clock edge, the typical MTBF is 170.3 years. If the sample is taken 10ns after the clock, the MTBF is 5.6 trillion years. (See page 9.)

Low Ground Bounce

The Philips Semiconductors BiCMOS QUBiC process produces exceptional noise immunity. The typical ground bounce, with 9 outputs simultaneously switching and the 10th output held low, is less than 0.8V. (See page 10.)

Military Device, ABT22V10-A/B

A military version of the ABT22V10 will be provided. A two page preliminary specification of the military version follows this commercial specification.

Programmable 3-stage Outputs

Each output has a 3-Stage output buffer with 3-State control. A product term controls the buffer, allowing enable and disable to be a function of any product of device inputs or output feedback. The combinatorial output provides a bidirectional I/O pin, and may be configured as a dedicated input if the buffer is always disabled.

Programmable Output Parity

The polarity of each macro cell output can be Active-HIGH or Active-LOW, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save "DeMorganizing" efforts.

Selection is controlled by programmable bit S_0 in the Output Macro Cell, and affects both registered and combinatorial outputs. Selection is automatic, based on the design specification and pin definitions. If the pin definition and output equation have the same polarity, the output is programmed to be Active-HIGH ($S_0 = 1$). (See page 13.)

Preset/Reset

For initialization, the ABT22V10 has additional Preset and Reset product terms.

These terms are connected to all registered outputs. When the Synchronous Preset (SP) product term is asserted high, the output registers will be loaded with a HIGH on the next LOW-to-HIGH clock transition. When the Asynchronous Reset (AR) product term is asserted high, the output registers will be immediately loaded with a LOW, independent of the clock.

Note that Preset and Reset control the flip-flop, not the output pin. The output level is determined by the output polarity selected. (See page 14.)

Power-Up Reset

All flip-flops power-up to a logic LOW for predictable system initialization. Outputs of the ABT22V10 will depend on the programmed output polarity. The V_{CC} rise must be monotonic and the reset delay time is 1–10 μ s maximum. (See page 16.)

Security Fuse

After programming and verification, a ABT22V10 design can be secured by programming the security fuse link. Once programmed, this fuse defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. When the security fuse is programmed, the array will read as if every fuse is programmed.

Quality and Testability

The ABT22V10 offers a very high level of built-in quality. Extra programmable fuses provide a means of verifying performance of all AC and DC parameters. In addition, this verifies programmability and functionality of the device to provide the highest programming and post-programming functional yields.

Technology

The BiCMOS ABT22V10 is fabricated with the Philips Semiconductors process known as QUBiC. QUBiC combines an advanced, state-of-the-art 1.0 μ m (drawn feature size) CMOS process with an ultra fast bipolar process to achieve superior speed and drive capabilities. QUBiC incorporates three layers of Al/Cu interconnects for reduced chip size, and our proven Ti-W fuse technology ensures highest programming yields.

Programming

The ABT 22V10-7 is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Philips Semiconductors SNAP design software package. ABEL™ CUPL™ and PALASM® 90 design software packages also support the ABT22V10-7 architecture.

All packages allow Boolean and state equation entry formats, SNAP, ABEL and CUPL also accept, as input, schematic capture format.

PROGRAMMING/SOFTWARE SUPPORT

Refer to Section 9 (*Development Software*) and Section 10 (*Support material*) of the 1994 PLD data handbook for additional information.

OUTPUT REGISTER PRELOAD

The register on the ABT22V10 can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery. The procedure for preloading follows:

1. Raise V_{CC} to 5.0V \pm 0.25V.
2. Set pin 2 or 3 to V_{HH} to disable outputs and enable preload.
3. Apply the desired value (V_{ILP}/V_{IHP}) to all registered output pins. Leave combinatorial output pins floating.
4. Clock Pin 1 from V_{ILP} to V_{IHP} .
5. Remove V_{ILP}/V_{IHP} from all registered output pins.
6. Lower pin 2 or 3 to V_{ILP} .
7. Enable the output registers according to the programmed pattern.
8. Verify V_{OL}/V_{OH} at all registered output pins. Note that the output pin signal will depend on the output polarity.

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Metastable Immune Characteristics

What is metastable immunity?

Philips Semiconductors uses the term 'metastable immune' to describe the output characteristics of registered logic devices. This term means that the outputs will not glitch or display an output anomaly under any circumstances, including set up and hold time violations.

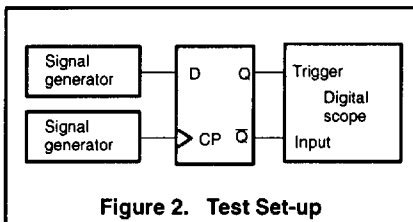


Figure 2. Test Set-up

For example, a typical metastable condition could result by running two independent signal generators (see Figure 2) at nearly the

same frequency (in this case 10MHz clock and 10.02MHz data). The device-under-test can often be driven into a metastable state, if the Q output is used to trigger a digital scope set to infinite persistence, the \bar{Q} output will build a waveform.

Figure 3 shows that the \bar{Q} output can vary in time with respect to the Q trigger point. This also implies that the Q or \bar{Q} output waveshapes may be distorted. This can be verified on an analog scope with a charge plate CRT. Of even greater interest are the dots running along the 3.5V volt line in the upper right hand quadrant. These show that the \bar{Q} output did not change state even though the Q output glitched to at least 1.5 volts, the trigger point of the scope.

When the device-under-test is a metastable immune part, the waveform will appear as in Figure 4. The output will not vary with respect to the Q trigger point even when the

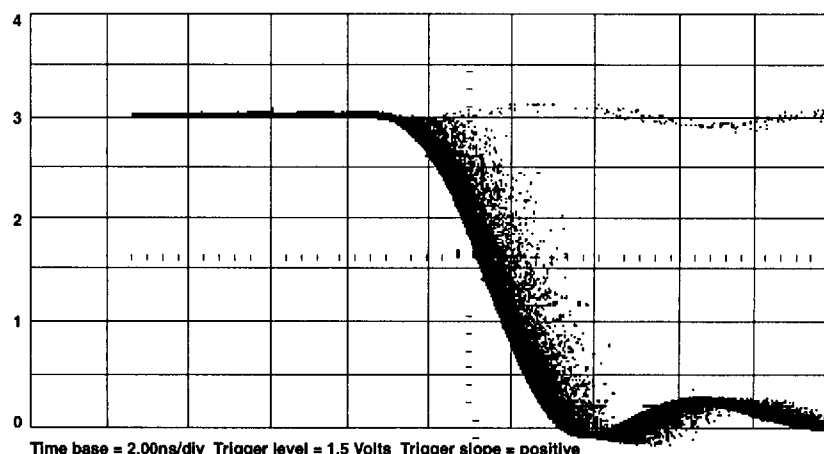
part is driven into a metastable state. Any tendency towards internal metastability is resolved by Philips Semiconductors patented circuitry. If a metastable event occurs within the flop the only outward manifestation of the event will be an increased clock-to-Q/ \bar{Q} propagation delay. This propagation delay is, a function of the metastability characteristics of the part defined by τ and T_0 ,

$$\text{where: MTBF} = e^{(t'/\tau)/T_0 F_c F_1}$$

t' = Time given to resolve contention between inputs after they are asserted and τ and T_0 are device parameters derived from tests and can be most nearly be defined as:

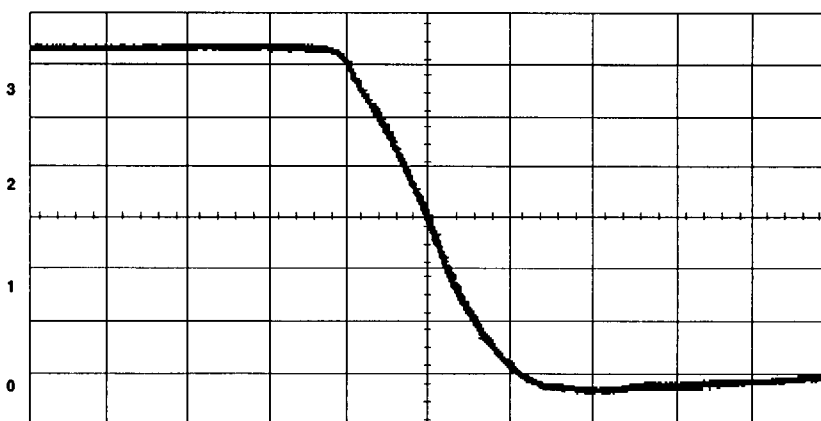
τ = A function of the rate at which a latch in a metastable state resolves that condition and T_0 = A function of the measurement of the propensity of a latch to enter a metastable state. T_0 is also a very strong function of the normal propagation delay of the device. Note one century = $3E9$ seconds.

COMPARISON OF METASTABLE IMMUNE AND NON-IMMUNE CHARACTERISTICS



Time base = 2.00ns/div Trigger level = 1.5 Volts Trigger slope = positive

Figure 3. Non-immune \bar{Q} output triggered by Q output, Setup and Hold times violated



Time base = 2.00ns/div Trigger level = 1.5 Volts Trigger slope = positive

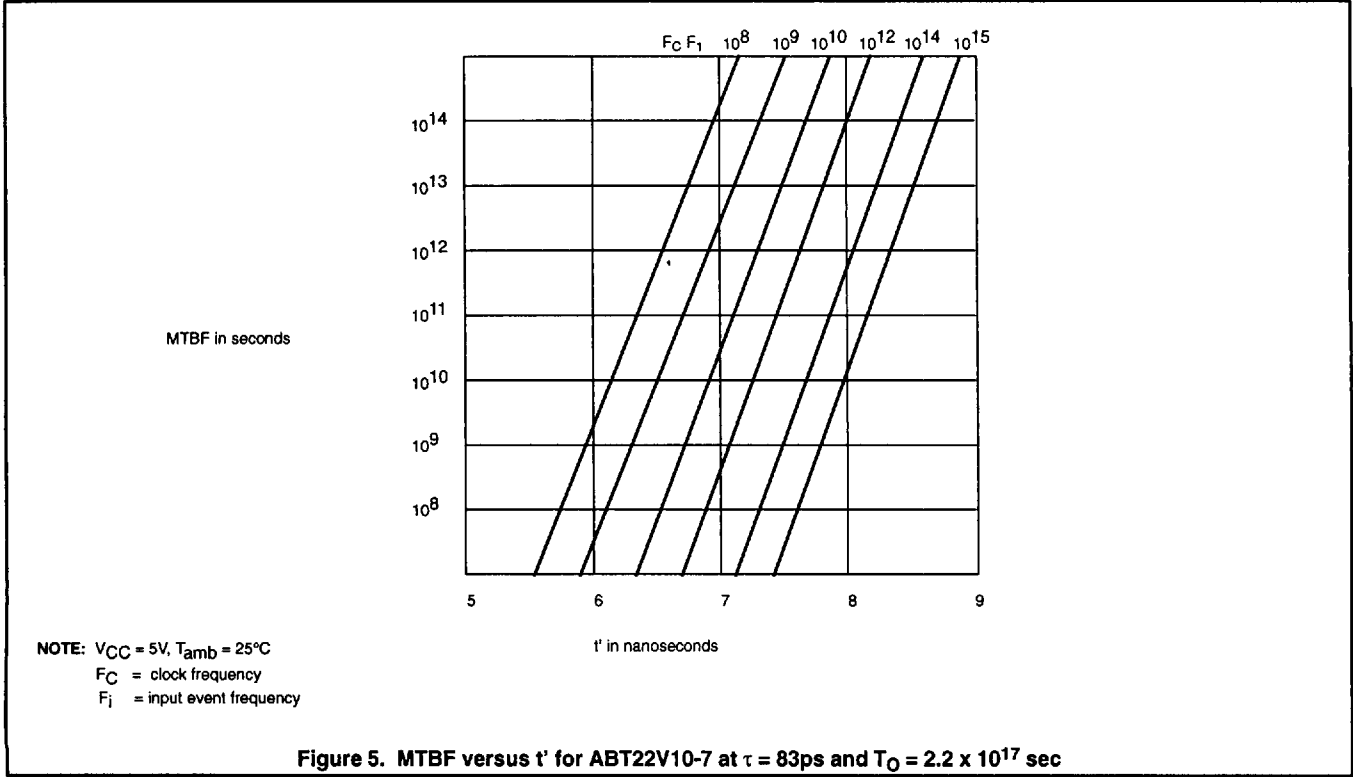
Figure 4. Metastable Immune \bar{Q} output triggered by Q output, Setup and Hold times violated

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ABT22V10-7 METASTABILITY

MEAN TIME BETWEEN FAILURES (MTBF) VERSUS t'



ABT22V10-7 VALUES FOR τ AND T_0

V_{CC}	$T_{amb} = 0^{\circ}C$		$T_{amb} = 25^{\circ}C$		$T_{amb} = 70^{\circ}C$	
	τ	T_0	τ	T_0	τ	T_0
5.5V	83ps	$8.1 \times 10^{18} sec$	82ps	$7.5 \times 10^{18} sec$	101ps	$3.0 \times 10^{12} sec$
5.0V	80ps	$4.0 \times 10^{18} sec$	83ps	$2.2 \times 10^{17} sec$	98ps	$4.4 \times 10^{11} sec$
4.5V	85ps	$3.4 \times 10^{14} sec$	91ps	$2.5 \times 10^{12} sec$	106ps	$1.1 \times 10^8 sec$

Design example

Suppose a designer wants to use the ABT22V10 for synchronizing asynchronous data that is arriving at 10MHz (as measured by a frequency counter), has a clock frequency of 50MHz, and has decided that he would like to sample the output of the ABT22V10 10ns after the clock edge. He

simply plugs his number into the equation below:

$$MTBF = e(t'/\tau)/T_0 F_C F_i$$

In this formula, F_C is the frequency of the clock, F_i is the average input event frequency, and t' is the time after the clock pulse that the output is sampled ($t' > h$, h

being the normal propagation delay). In this situation the F_i will be twice the data frequency of (20 MHz) because input events consist of both of low and high transitions. Multiplying F_i by F_C gives an answer of $10^{15} Hz^2$. Using the above formula the actual MTBF is 5.6 trillion years for the ABT22V10-7.

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LOW NOISE

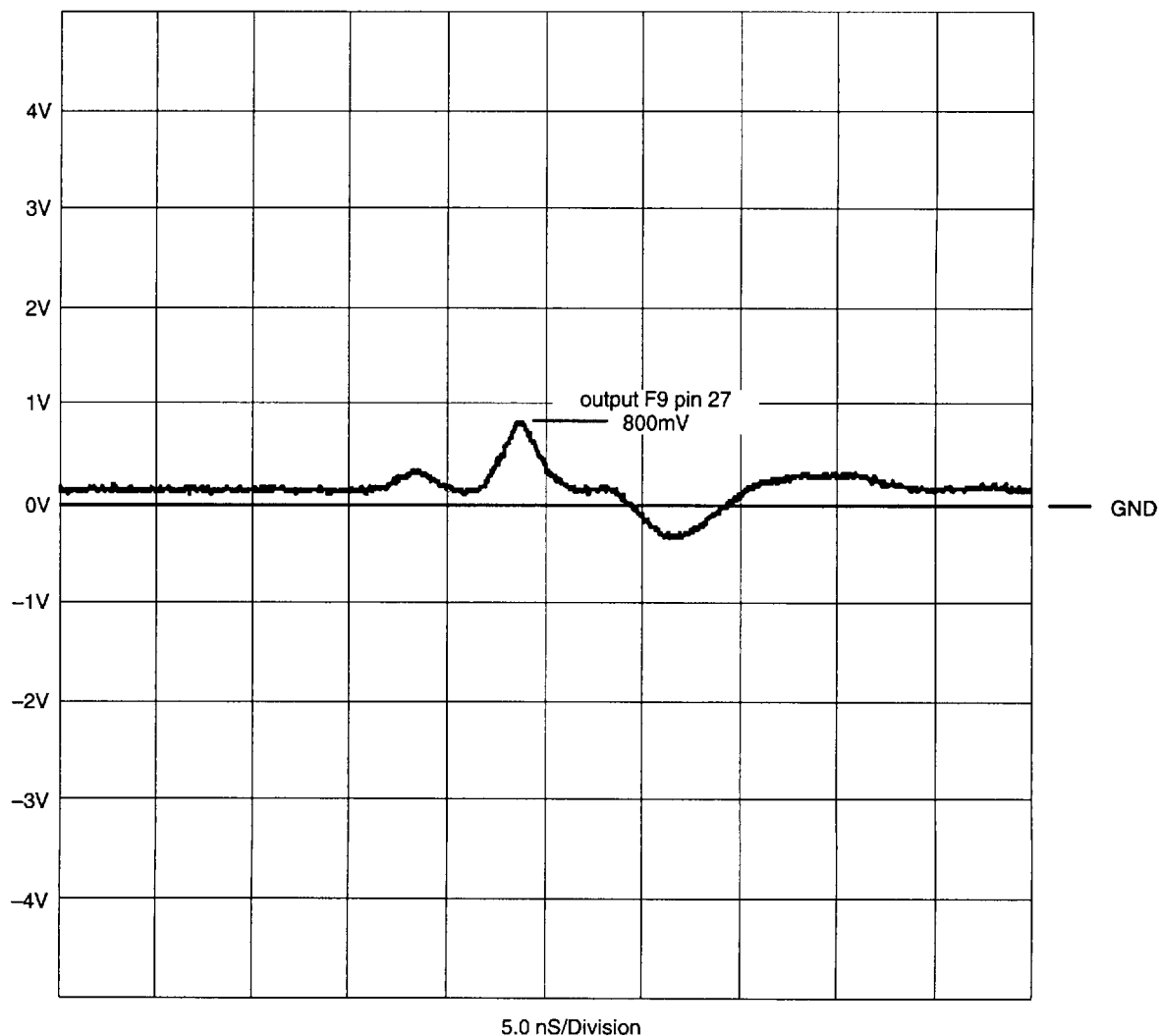


Figure 6. Device Characterization

Ground Bounce

Figure 6 shows the low ground (V_{OLP}) bounce (0.8V) observed on the 10th output of the ABT22V10 under the following conditions: 9 remaining outputs switching, each driving 50 pF loads, in PLCC non-socketed device,

at 5.25V, 25°C. Similar testing of comparable EECMOS 22V10 devices resulted in ground bounce in the 1.5 – 2.0 V range.

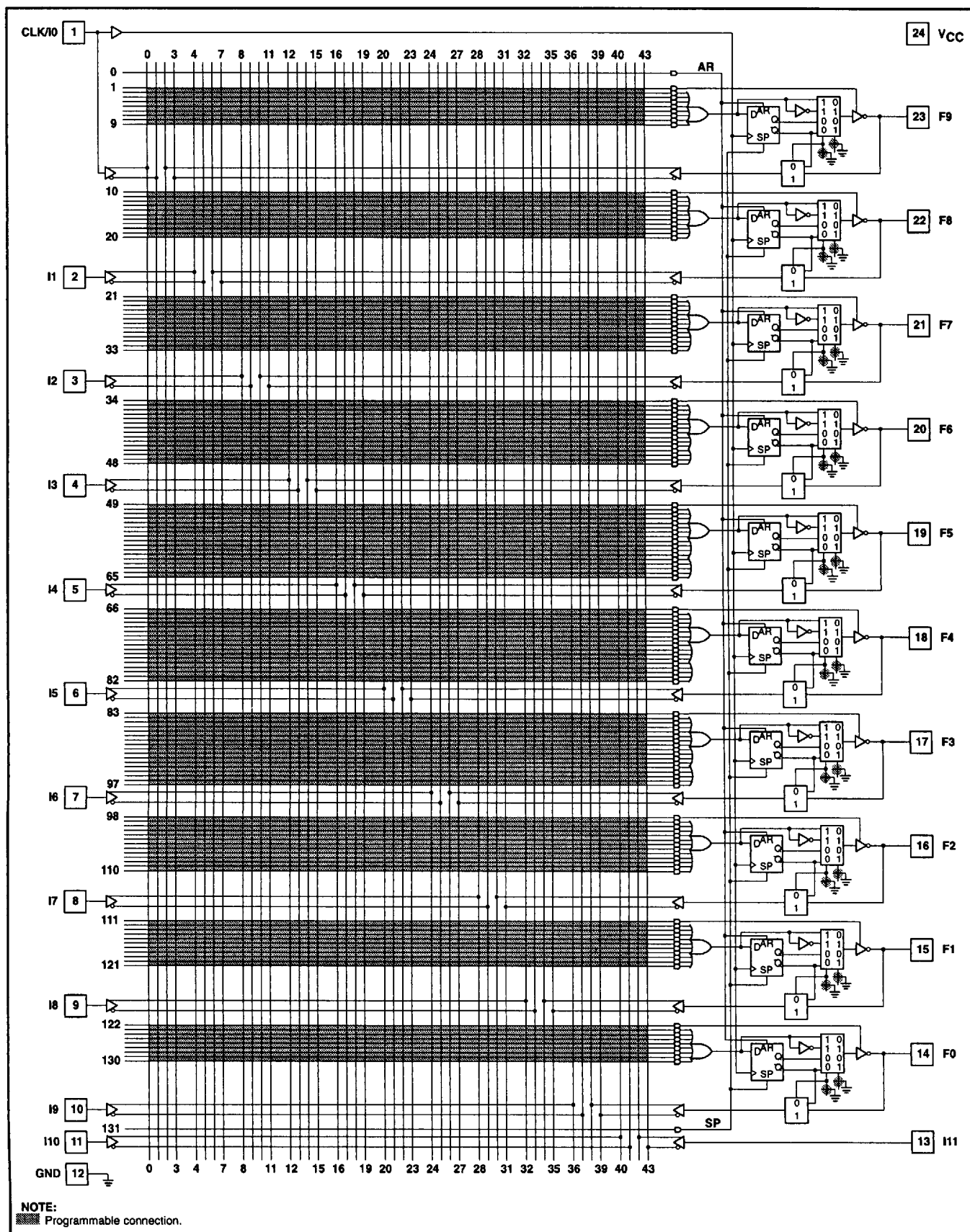
At Philips the utilization of our advanced BiCMOS process, QUIBIC, enables the

production of high performance devices with the lowest output noise to ensure first pass system reliability. Quiet your concerns on ground bounce with Philips ABT22V10-7.

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LOGIC DIAGRAM



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FUNCTIONAL DIAGRAM

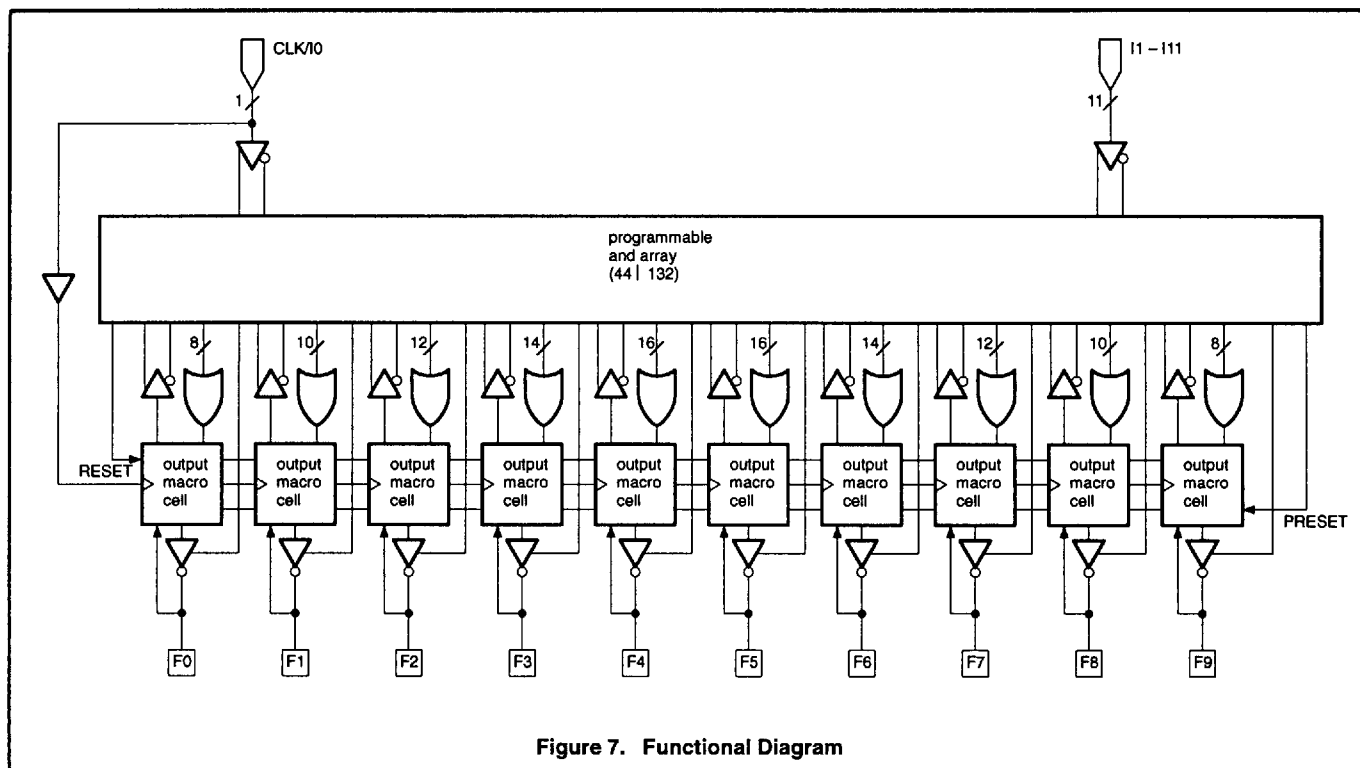


Figure 7. Functional Diagram

FUNCTIONAL DESCRIPTION

The ABT22V10 allows the systems engineer to implement the design on-chip, by opening fuse links to configure AND and OR gates within the device, according to the desired logic function.

Product terms with all fuses opened assume the logical HIGH state; product terms connected to both True and Complement of any single input assume the logical LOW state.

The ABT22V10 has 12 inputs and 10 I/O Macro Cells (Figure 7). The Macro Cell

allows one of four potential output configurations, registered output or combinatorial I/O, Active-HIGH or Active-LOW (see Figure 8). The configuration choice is made according to the user's design specification and corresponding programming of the configuration bits $S_0 - S_1$. Multiplexer controls are connected to ground (0) through a programmable fuse link, selecting the "0" path through the multiplexer. Programming the fuse disconnects the control line from GND and it floats to V_{CC} (1), selecting the "1" path.

The device is produced with a fuse link at each input to the AND gate array, and connections may be selectively removed by applying appropriate voltages to the circuit. Utilizing an easily-implemented programming algorithm, these products can be rapidly programmed to any customized pattern. Information on approved programmers can be found in the Programmer Reference Guide. Extra test fuses are pre-programmed during manufacturing to ensure extremely high field programming yields, and provide extra test paths to achieve parametric correlation.

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OUTPUT MACRO CELL

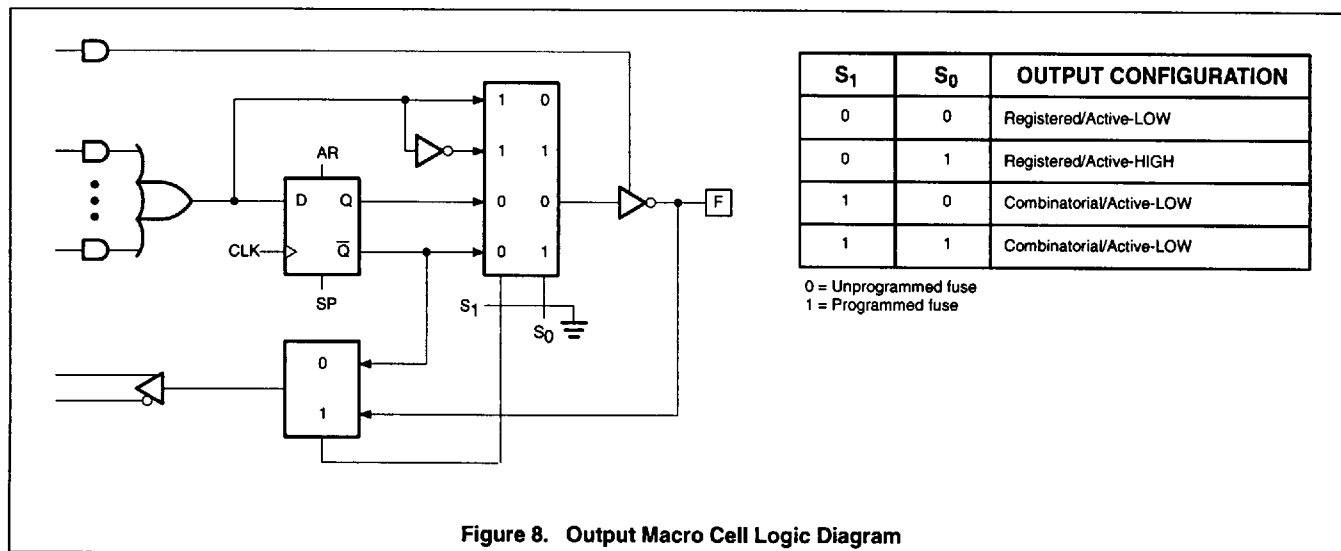


Figure 8. Output Macro Cell Logic Diagram

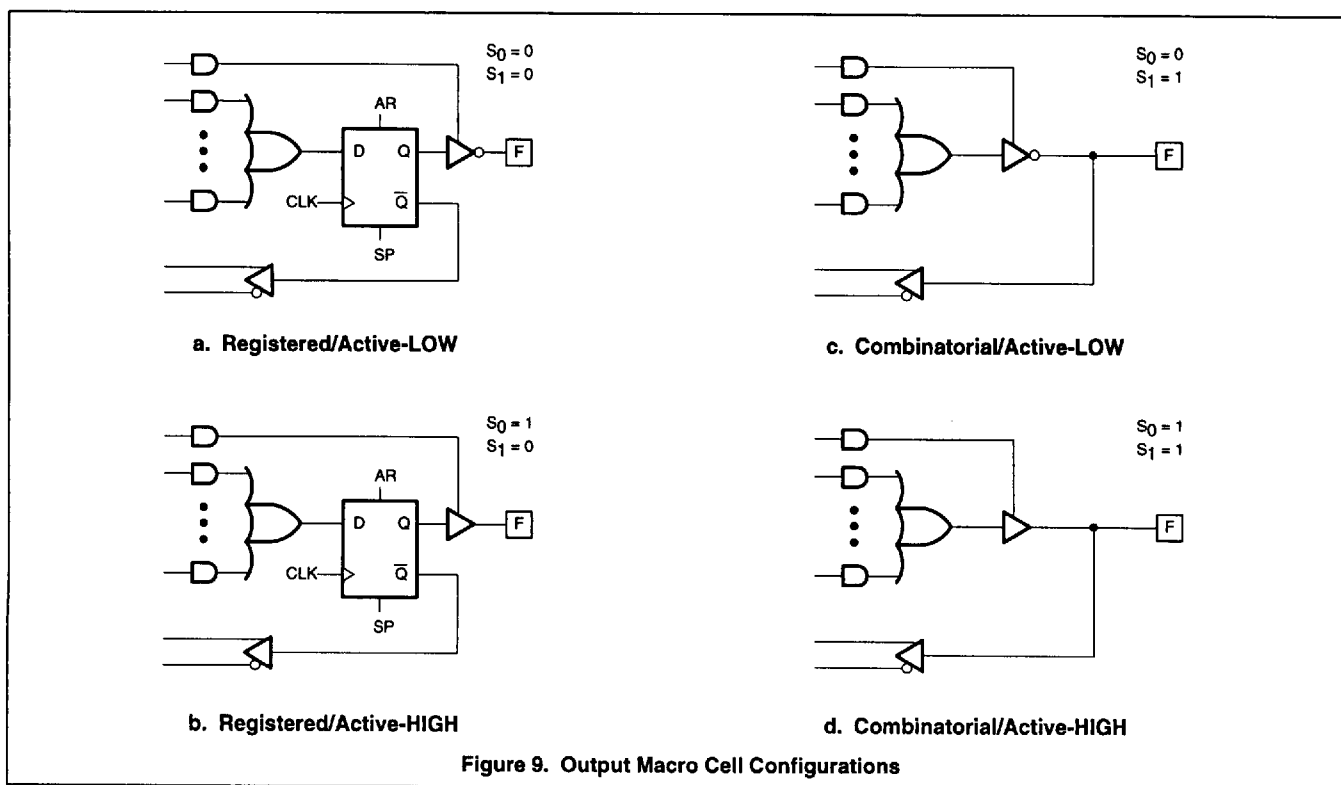


Figure 9. Output Macro Cell Configurations

Registered Output Configuration

Each Macro Cell of the ABT22V10 includes a D-type flip-flop for data storage and synchronization. The flip-flop is loaded on the LOW-to-HIGH transition of the clock input. In the registered configuration ($S_1 = 0$), the array feedback is from \bar{Q} of the flip-flop.

Combinatorial I/O Configuration

Any Macro Cell can be configured as combinatorial by selecting the multiplexer path that bypasses the flip-flop ($S_1 = 1$). In the combinatorial configuration, the feedback is from the pin.

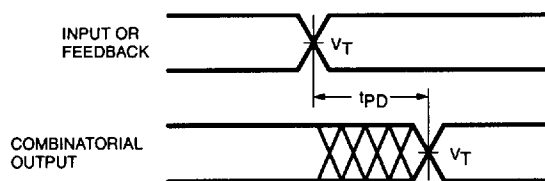
Variable Input/Output Pin Ratio

The ABT22V10 has twelve dedicated input lines, and each Macro Cell output can be an I/O pin. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Unused input pins should be tied to V_{CC} or GND.

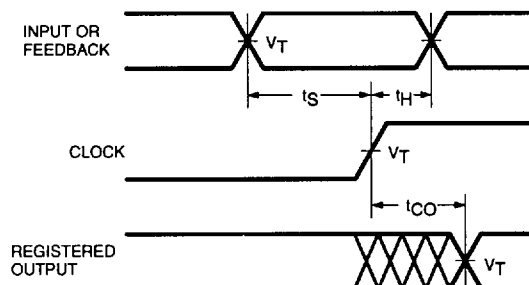
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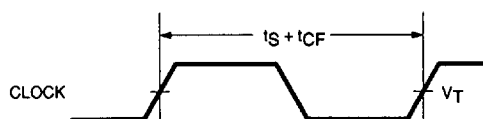
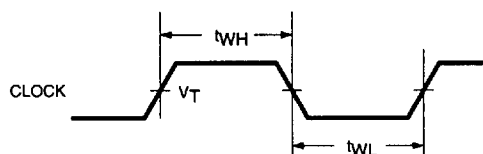
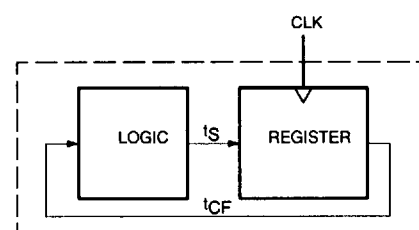
SWITCHING WAVEFORMS



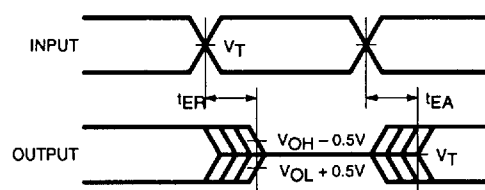
Combinatorial Output



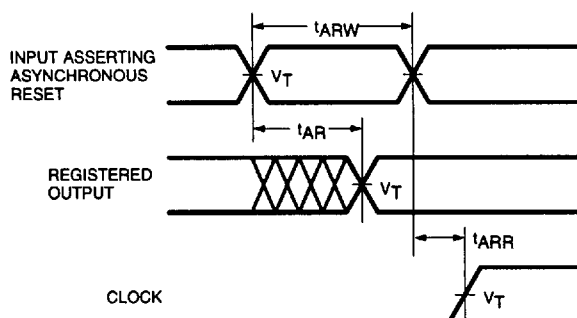
Registered Output

Clock to Feedback (t_{MAX} Internal)
(See Path at Right)

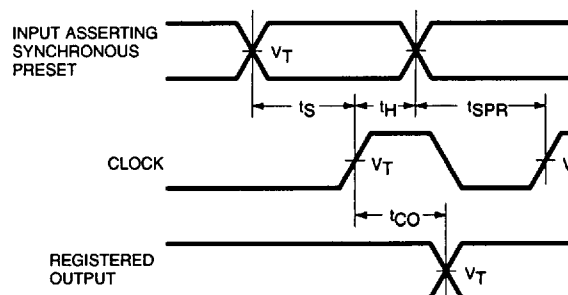
Clock Width



Input to Output Disable/Enable



Asynchronous Reset



Synchronous Preset

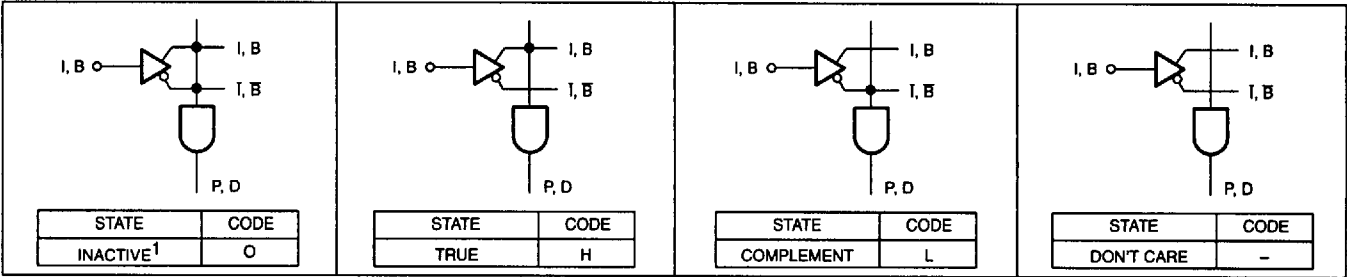
NOTES:

1. $V_T = 1.5V$.
2. Input pulse amplitude 0V to 3.0V.
3. Input rise and fall times 2.5ns max.

Low noise, high drive, metastable immune, PLD

ABT22V10-7

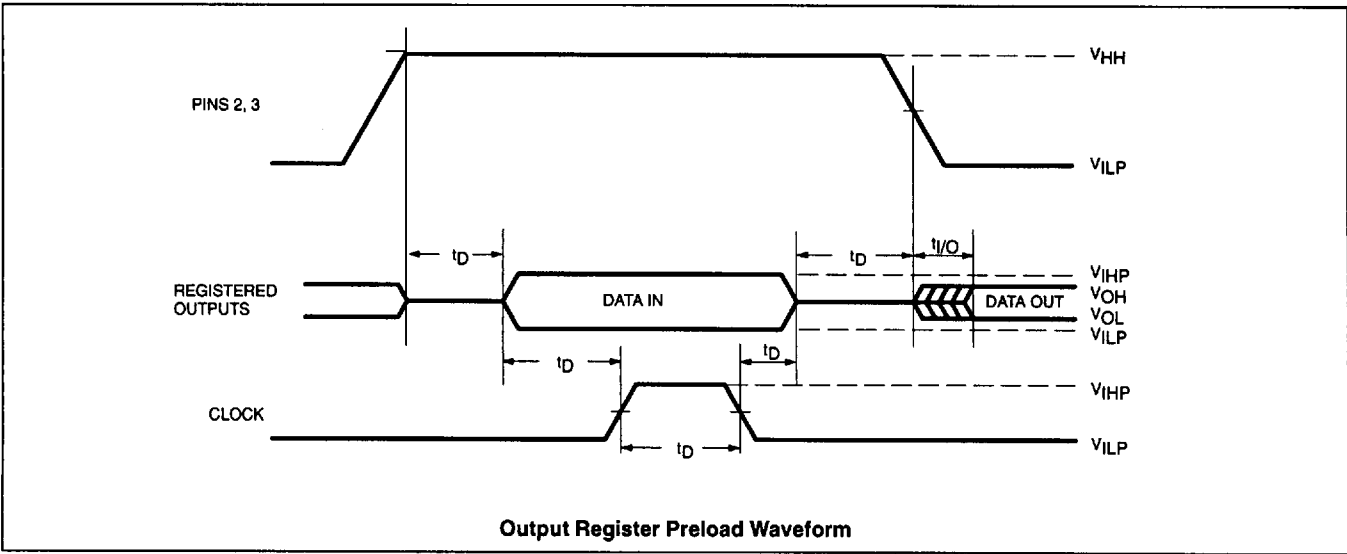
“AND” ARRAY – (I, B)



NOTE:
1. This is the initial state.

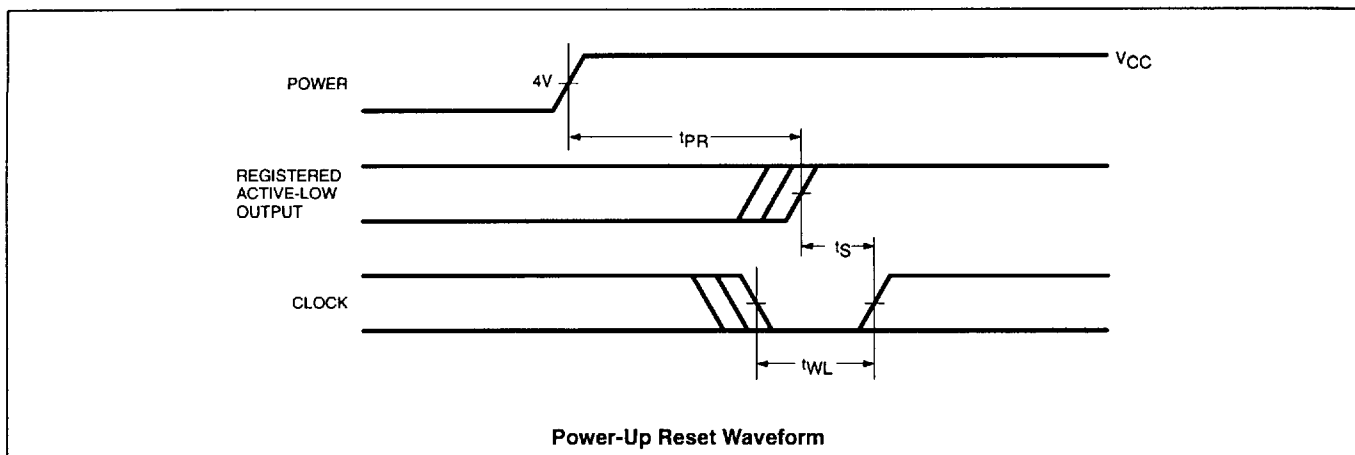
PRELOAD SET-UP

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	REC	MAX	
V _{HH}	Super-level input voltage	9.5	9.5	10	V
V _{ILP}	Low-level input voltage	0	0	0.8	V
V _{IHP}	High-level input voltage	2.4	5.0	5.5	V
t _D	Delay time	100	200	1000	ns
t _{I/O}	I/O valid after Pin 2 or 3 drops from V _{HH} to V _{ILP}	100			ns



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ABT22V10-7



SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
t _{PR}	Power-up Reset Time		1	μs
t _S	Input or Feedback Setup Time	See AC Electrical Characteristics		
t _{WL}	Clock Width LOW			

POWER-UP RESET

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. The output state will depend on the programmed pattern. This feature is valuable in simplifying state machine initialization. A timing diagram and

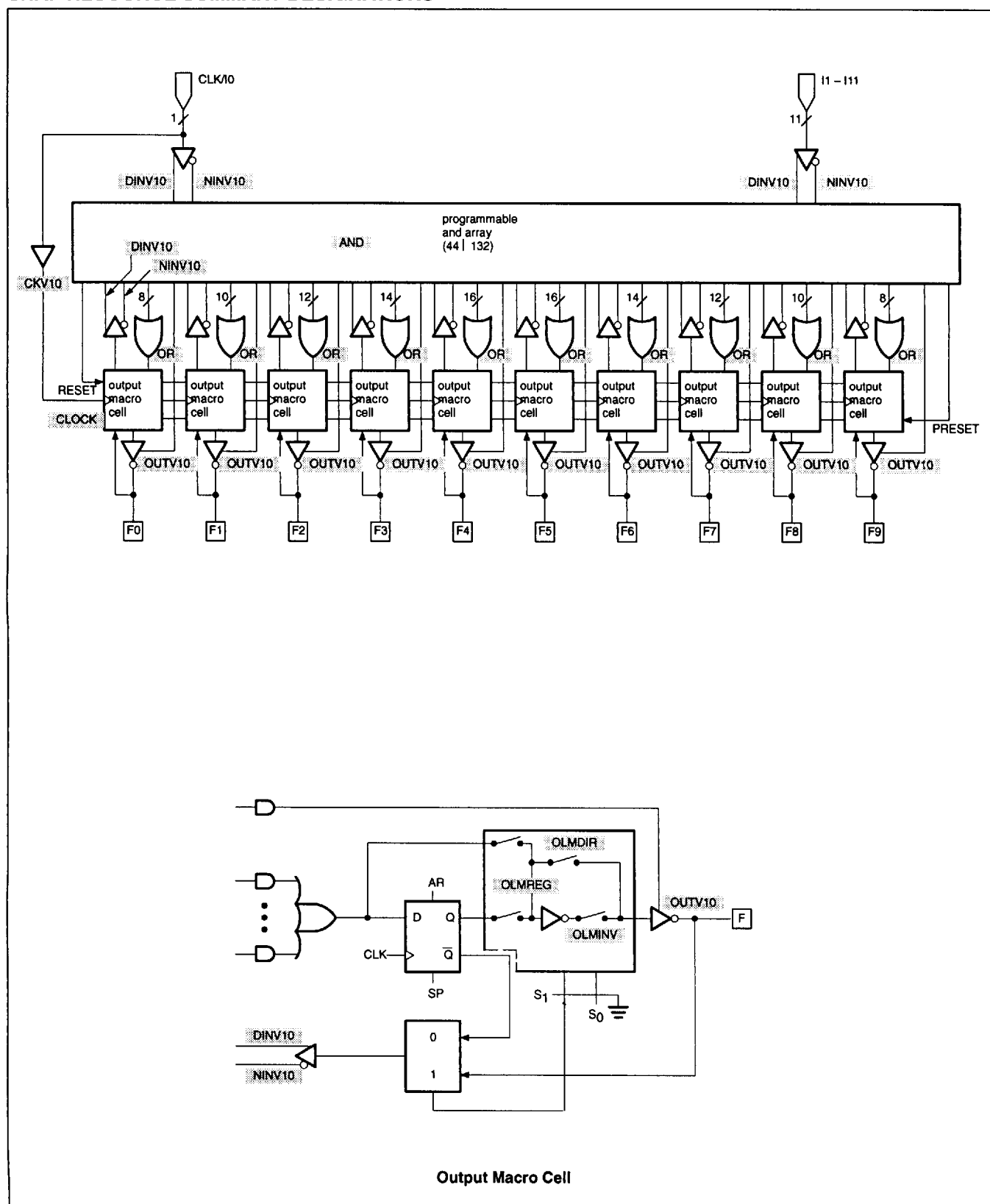
parameter table are shown above. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Low noise, high drive, metastable immune, PLD

ABT22V10-7

SNAP RESOURCE SUMMARY DESIGNATIONS



Low noise, high drive, metastable immune, PLD

ABT22V10A/B

MILITARY VERSION

DESCRIPTION

This page along with the following page covers the significant characteristics of the military ABT22V10 device. These differences include package, operating temperature range, V_{CC} range, and changes in the electrical characteristics.

Two speed versions of the ABT22V10 are available, the "A" and "B" versions of the device. The ABT22V10A/BLA has a T_{pd} of 10ns and the ABT22V10B/BLA has a T_{pd} of 8.5ns making this the fastest 22V10 part available to a full military temperature range.

For further information on the military 883 compliant devices, please contact the Military and Special Products Group or our local authorized sales representative

Order codes can be found in the Ordering Information table.

FEATURES

- Ultra fast 8.5ns t_{PD} and 7.5ns t_{CO}
- Pin and JEDEC file compatibility to industry standard 22V10
- 10 input/output macro cells for architectural flexibility
- Metastable immune flip-flops

- Low ground bounce (<0.8V typical)
- Varied product term distribution with up to 16 product terms per output for complex functions
- Programmable output polarity
- Power-up reset on all registers
- Synchronous Preset/Asynchronous Reset
- Programmable on standard PAL-type device programmers
- Design support provided using SNAP software development package and other CAD tools for PLDs

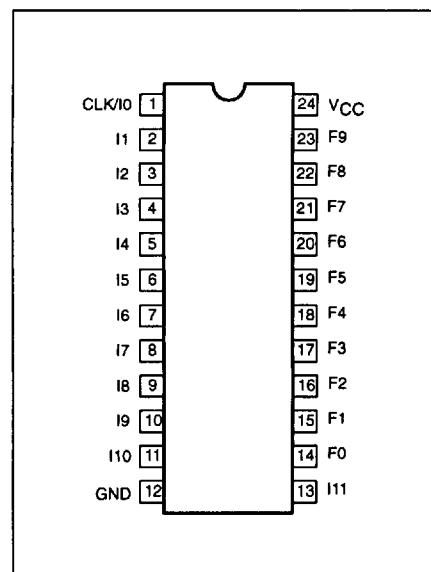
APPLICATIONS

- DMA control
- State machine implementation
- High speed graphics processing
- Counters/shift registers
- SSI/MSI random logic replacement
- High speed memory decoder

PIN LABEL DESCRIPTIONS

I1 – I11	Dedicated Input
NC	Not Connected
F0 – F9	Macro Cell Input/Output
CLK/I0	Clock Input/Dedicated Input
V_{CC}	Supply Voltage
GND	Ground

PIN CONFIGURATIONS



ORDERING INFORMATION

DESCRIPTION	ORDER CODE	PROPAGATION DELAY
24-Pin Plastic Dual-In-Line Package 300mil-wide	ABT22V10A/BLA	10ns
28-Pin Plastic Leaded Chip Carrier	ABT22V10B/BLA	8.5ns

Low noise, high drive, metastable immune, PLD

ABT22V10A/B

MILITARY VERSION

ABSOLUTE MAXIMUM RATINGS¹

SYMBOL	PARAMETER	RATINGS		UNIT
		MIN	MAX	
V _{CC}	Supply voltage	-0.5	+7.0	V _{DC}
V _{IN}	Input voltage	-1.2	V _{CC} + 0.5	V _{DC}
V _{OUT}	Output voltage	-0.5	V _{CC} + 0.5	V _{DC}
I _{IN}	Input currents	-30	+30	mA
I _{OUT}	Output currents		+100	mA
T _{stg}	Storage temperature range	-65	+150	°C

THERMAL RATINGS

TEMPERATURE	
Maximum junction	175°C
Maximum ambient	125°C
Allowable thermal rise ambient to junction	50°C

NOTE:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

OPERATING RANGES

SYMBOL	PARAMETER	RATINGS		UNIT
		MIN	MAX	
V _{CC}	Supply voltage	+4.5	+5.5	V _{DC}
T _{amb}	Operating free-air temperature	-55	+125	°C

DC ELECTRICAL CHARACTERISTICS (OVER OPERATING RANGES)

SYMBOL	PARAMETER	TA = -55°C to 125°C unless otherwise noted TEST CONDITIONS ¹	LIMITS		UNIT
			MIN	MAX	
Input voltage					
V _{IL}	Low	V _{CC} = MIN		0.8	V
V _{IH}	High	V _{CC} = MAX	2.0		V
V _I	Clamp	V _{CC} = MIN, I _{IN} = -18mA		-1.2	V
Output voltage					
V _{OL}	Low	V _{CC} = MIN, V _{IN} = V _{IH} or V _{IL} I _{OL} = 30mA		0.5	V
V _{OH}	High	I _{OH} = -16 mA	2.4		V
Input current					
I _{IL} (except Pin 1)	Low	V _{CC} = MAX V _{IN} = 0.40V		-25	μA
I _{IL} (Pin 1)	Low	V _{IN} = 0.40V		-50	μA
I _{IH}	High	V _{IN} = 2.7V		25	μA
I _I	Maximum input current	V _{IN} = 5.5V		1.0	mA
Output current					
I _{OZL}	Output leakage ²	V _{CC} = MAX V _{IN} = V _{IL} or V _{IH} , V _{OUT} = 0.4V		-100	μA
I _{SC}	Short circuit ³	V _{OUT} = 0.5 V	-30	-200	mA
I _{CC}	V _{CC} supply current	V _{CC} = MAX		190	mA

NOTES:

1. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
 2. I/O pin leakage is the worst case of I_{OZX} or I_{IX} (where X = H or L).
 3. No more than one output should be tested at a time. Duration of the short-circuit test should not exceed one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.

Metastable immune, low noise, universal PLD

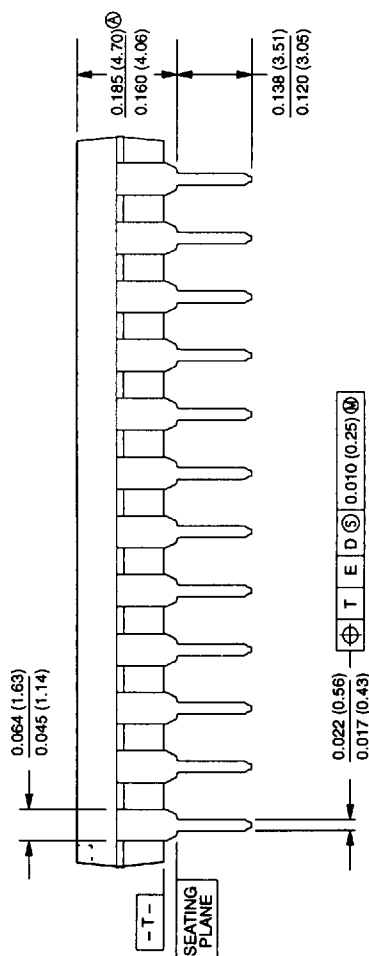
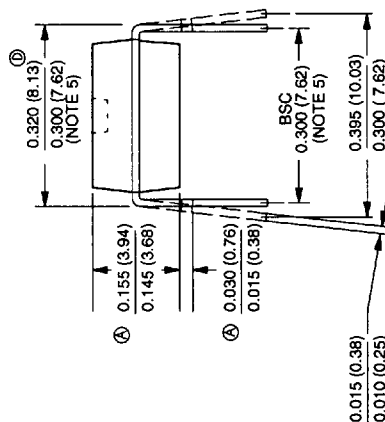
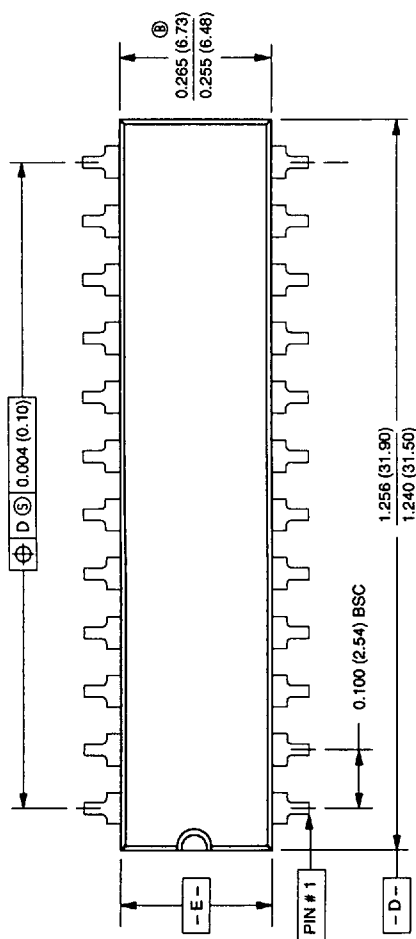
ABT22V10-7

SOT101/0410D

24-PIN (300 mils wide) PLASTIC DUAL IN-LINE (N) PACKAGE

NOTES:

1. Controlling dimension: Inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC Specification MS-001-AF for standard Dual In-Line (DIP) package 0.300 inch row spacing (plastic) 24 leads (Issue B, 7/85).
3. Dimension and tolerancing per ANSI Y14, 5M – 1982.
4. "T", "D", and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with Pin #1 and continue counterclockwise to Pin #24 when viewed from the top.



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Metastable immune, low noise, universal PLD

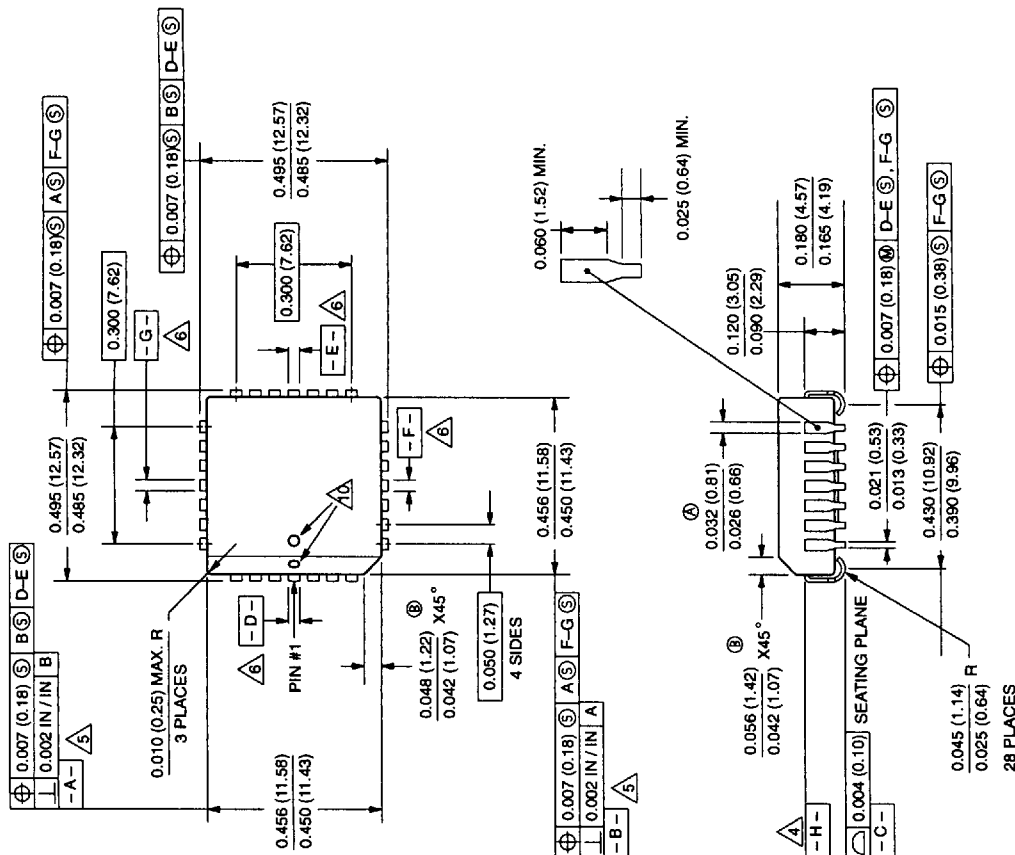
ABT22V10-7

SOT261/0401F

28-PIN (300 mils wide) PLASTIC LEADED CHIP CARRIER (A) PACKAGE

NOTES

- Package dimensions conform to JEDEC Specification MO-047-AB for Plastic Leaded Chip Carrier 28 leads, 0.050 inch (1.27mm) lead spacing, square. (Issue A, 10/31/84.)
- Controlling dimensions: inches. Metric dimensions in mm are shown in parentheses.
- Dimensioning and tolerancing per ANSI Y14.5M-1982.
- Datum plane "H" located at the top of mold parting line and coincident with top of lead, where lead exits plastic body.
- Location to datum "A" and "B" to be determined at plane "H". These datums do not include mold flash. Mold flash protrusion shall not exceed 0.010" (0.25mm) on any side.
- Datum "D-E" and "F-G" are determined where these center leads exit from the body at plane "H".
- Pin numbers continue counterclockwise to Pin 28 (top view).
- Signetics order code for product packaged in a PLCC is the suffix "A" after the product number.
- Applicable to packages with pedestal only.
- Location of Pin #1 mark is optional. Mark on chamfered side is preferred.



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ABT22V10-7

NOTES

1. Package dimensions conform to JEDEC Specification MS-013-AD for standard Small Outline (SO) package, 24 leads, 7.50mm (0.300") body width (Issue A. June 1985).
2. Controlling dimensions are mm. Inch dimensions in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M-1982.
4. "D" and "E" are reference datums on the molded body and do not include mold flash/protrusions. Mold flash/protrusions at "D" shall not exceed 0.15mm (0.006") per side. Inter-lead flash/protrusions at "E" shall not exceed 0.25mm (0.010") per side.
5. The lead width above the seating plane shall not exceed a maximum value of 0.61mm (0.024").
6. Pin numbers start with Pin #1 and continue counterclockwise to Pin #24 when viewed from top.
7. Signetics ordering code for a product packaged in a plastic Small Outline (SO) package is the suffix D after the product number.

