HY524400 Series
1M x 4-bit CMOS DRAM

DESCRIPTION

The HY524400 is the new generation and fast dynamic RAM organized 1,048,576 x 4 bits. The HY524400 utilizes CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins to the users. Multiplexed address inputs permit the HY524400 to be packaged in a standard 20/26 pin plastic SOJ. The package size provides high system bit densities and is compatible with widely available automated-test equipments. System oriented-feature includes single power supply of 5V± 10% tolerence and direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- **Low power dissipation**
  Max. CMOS standby 5.5mW
  Max. TTL standby 11.0mW
  Max. operating

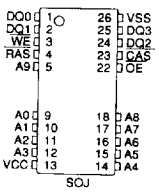
Speed	Power
70	742.5mW
80	632.5mW
10	577.5mW

- **Single power supply of 5V± 10%**
- **TTL compatible inputs and outputs**
- **Fast access Time**

Speed	tRAC	tCAC	tPC
70	70ns	20ns	45ns
80	80ns	20ns	50ns
10	100ns	25ns	60ns

- **Fast page mode operation**
- **Read-Modify-Write capability**
- **$\overline{CAS}$-before-$\overline{RAS}$, $\overline{RAS}$-only, refresh**
- **1024 refresh cycles / 16ms**

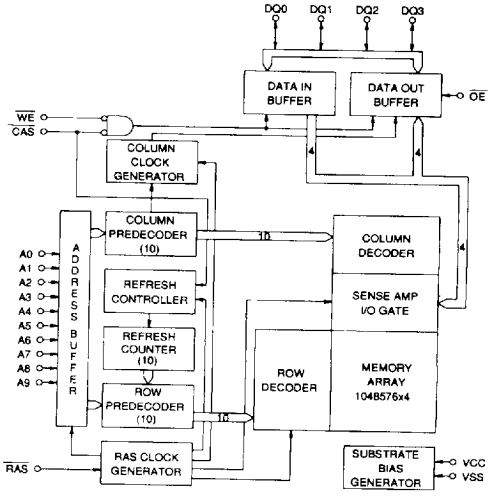
PIN CONNECTION



PIN DESCRIPTION

$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
A0-A9	Address Input
DQ0-DQ3	Data Input/Output
Vcc	Power (+ 5V)
Vss	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	°C
T_{STG}	Storage Temperature	-55 to 125	°C
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to V_{SS}	-0.7 to V_{CC} + 0.7	V
V_{CC}	Voltage on V_{CC} Relative to V_{SS}	-0.5 to 6.5	V
I_{OS}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	1.0	W
T_{SOLDER}	Soldering Temperature• Time	260• 10	°C• sec

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A= 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	-	V_{CC}+ 1.0	V
V_{IL}	Input Low Voltage	0.0	-	0.8	V

NOTE : All voltages are referenced to V_{SS}.

Noise on $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ must be within Application Specification limits.
This can be accomplished with adding in your design a series 33 ohm resistor for the above input near the DRAMs.

DC CHARACTERISTICS

(T_A= 0°C to 70°C, V_{CC}= 5V± 10%, V_{SS}= 0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED	MIN.	MAX.	UNIT	NOTE
I_{LI}	Input Leakage Current (Any Input Pins)	$V_{SS} \le V_{IN} \le 6.5V$, All other pins not under test= V_{SS}		-10	10	µA	
I_{LO}	Output Leakage Current (High Impedance State)	$V_{SS} \le V_{OUT} \le 5.5V$, $\overline{RAS}$ & $\overline{CAS}$ at V_{IH}		-10	10	µA	
I_{CC1}	V_{CC} Supply Current, Operating	t_{RC}= t_{RC} (min.)	70 80 10	- - -	135 115 105	mA	1,2,3
I_{CC2}	V_{CC} Supply Current, TTL Standby	$\overline{RAS}$ & $\overline{CAS}$ at V_{IH}		-	2	mA	
I_{CC3}	V_{CC} Supply Current, $\overline{RAS}$-only refresh	t_{RC}= t_{RC} (min.)	70 80 10	- - -	135 115 105	mA	1,3
I_{CC4}	V_{CC} Supply Current, Fast Page mode	t_{PC}= t_{PC} (min.)	70 80 10	- - -	65 60 50	mA	1,2,3
I_{CC5}	V_{CC} Supply Current, CMOS Standby	$\overline{RAS}$ & $\overline{CAS} \ge V_{CC}$–0.2V		-	1	mA	
I_{CC6}	V_{CC} Supply Current, $\overline{CAS}$-before-$\overline{RAS}$ refresh	t_{RC}= t_{RC} (min.)	70 80 10	- - -	135 115 105	mA	1,3
V_{OL}	Output Low Voltage	I_{OL}= 4.2mA		-	0.4	V	
V_{OH}	Output High Voltage	I_{OH}= –5mA		2.4	-	V	

NOTE :
1. I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC6} depend on cycle rate.
2. I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. It depends on user whether column address is changed or not at least once while $\overline{RAS}$= V_{IL} and $\overline{CAS}$= V_{IH}.

AC CHARACTERISTICS

(TA= 0°C to 70°C, Vcc= 5V± 10%, Vss= 0V, unless otherwise noted.) NOTE : 1, 2, 3

#	SYMBOL	PARAMETER	HY524400J						UNIT	NOTE
			-70		-80		-10			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	130	-	150	-	180	-	ns	3
2	tRWC	Read-Modify-Write Cycle Time	180	-	205	-	245	-	ns	3,11
3	tPC	Fast Page Mode Cycle Time	45	-	50	-	60	-	ns	3
4	tPRWC	Fast Page Mode Read-Modify-Write Cycle Time	90	-	100	-	115	-	ns	3,11
5	tRAC	Access Time from $\overline{RAS}$	-	70	-	80	-	100	ns	4,5,6
6	tCAC	Access Time from $\overline{CAS}$	-	20	-	20	-	25	ns	4,5,6
7	tAA	Access Time from Column Address	-	35	-	40	-	50	ns	5,6
8	tCPA	Access Time from $\overline{CAS}$ Precharge	-	40	-	45	-	55	ns	6
9	tCLZ	$\overline{CAS}$ to Output Low Impedance	0	-	0	-	0	-	ns	8
10	tOFF	Output Buffer Turn-off Delay	0	15	0	15	0	20	ns	
11	tT	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	
12	tRP	$\overline{RAS}$ Precharge Time	50	-	60	-	70	-	ns	
13	tRAS	$\overline{RAS}$ Pulse Width	70	16K	80	16K	100	16K	ns	3
14	tRASP	$\overline{RAS}$ Pulse Width (Fast Page Mode)	70	16K	80	16K	100	16K	ns	
15	tRSH	$\overline{RAS}$ Hold Time	20	-	20	-	25	-	ns	
16	tCSH	$\overline{CAS}$ Hold Time	70	-	80	-	100	-	ns	
17	tCAS	$\overline{CAS}$ Pulse Width	20	-	20	-	25	-	ns	
18	tRCD	$\overline{RAS}$ to $\overline{CAS}$ Delay	20	50	20	60	20	75	ns	4
19	tRAD	$\overline{RAS}$ to Column Address Delay Time	15	-	15	-	17	-	ns	7
20	tCRP	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	-	10	-	10	-	ns	
21	tCP	$\overline{CAS}$ Precharge Time	10	-	10	-	10	-	ns	
22	tASR	Row Address Set-up Time	0	-	0	-	0	-	ns	
23	tRAH	Row Address Hold Time	10	-	10	-	15	-	ns	
24	tASC	Column Address Set-up Time	0	-	0	-	0	-	ns	
25	tCAH	Column Address Hold Time	15	-	15	-	20	-	ns	
26	tAR	Column Address Hold Time from $\overline{RAS}$	50	-	55	-	70	-	ns	
27	tRAL	Column Address to $\overline{RAS}$ Lead Time	35	-	40	-	50	-	ns	
28	tRCS	Read Command Set-up Time	0	-	0	-	0	-	ns	
29	tRCH	Read Command Hold Time Referenced to $\overline{CAS}$	0	-	0	-	0	-	ns	
30	tRRH	Read Command Hold Time Referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	
31	tWCH	Write Command Hold Time	15	-	15	-	20	-	ns	
32	tWCR	Write Command Hold Time from $\overline{RAS}$	55	-	60	-	65	-	ns	
33	tWP	Write Command Pulse Width	15	-	15	-	20	-	ns	
34	tRWL	Write Command to $\overline{RAS}$ Lead Time	20	-	20	-	25	-	ns	
35	tCWL	Write Command to $\overline{CAS}$ Lead Time	20	-	20	-	25	-	ns	
36	tDS	Data-In Set-up Time	0	-	0	-	0	-	ns	9
37	tDH	Data-In Hold Time	15	-	15	-	20	-	ns	9
38	tDHR	Data-In Hold Time Referenced to $\overline{RAS}$	55	-	60	-	65	-	ns	
39	tREF	Refresh Period (1024 cycles)	-	16	-	16	-	16	ms	2,3
40	tWCS	Write Command Set-up Time	0	-	0	-	0	-	ns	

AC CHARACTERISTICS

(continued)

#	SYMBOL	PARAMETER	HY524400J						UNIT	NOTE
			-70		-80		-10			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
41	tCWD	$\overline{CAS}$ to $\overline{WE}$ Delay Time	40	-	45	-	55	-	ns	11
42	tRWD	$\overline{RAS}$ to $\overline{WE}$ Delay Time	90	-	105	-	130	-	ns	11
43	tAWD	Column Address to $\overline{WE}$ Delay Time	55	-	65	-	80	-	ns	11
44	tCSR	$\overline{CAS}$ Set-up Time (CBR Cycle)	10	-	10	-	10	-	ns	10
45	tCHR	$\overline{CAS}$ Hold Time (CBR Cycle)	15	-	20	-	20	-	ns	
46	tRPC	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	10	-	10	-	10	-	ns	
47	tROH	$\overline{RAS}$ Hold Time Referenced to $\overline{OE}$	10	-	10	-	15	-	ns	
48	tOEA	$\overline{OE}$ Access Time	-	20	-	20	-	25	ns	5,6
49	tOED	$\overline{OE}$ to Data Delay	20	-	20	-	25	-	ns	
50	tOEZ	Output Buffer Turn Off Delay Time from $\overline{OE}$	-	15	-	15	-	20	ns	8
51	tOEH	$\overline{OE}$ Command Hold Time	15	-	15	-	20	-	ns	
52	tCPWD	$\overline{WE}$ Delay Time from $\overline{CAS}$ Precharge	65	-	70	-	80	-	ns	
53	tRHCP	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	35	-	40	-	45	-	ns	
54	tWRP	$\overline{WE}$ to $\overline{RAS}$ Precharge Time (CBR Cycle)	5	-	5	-	5	-	ns	10
55	tWRH	$\overline{WE}$ to $\overline{RAS}$ Hold Time (CBR Cycle)	10	-	10	-	15	-	ns	10

NOTE :

1. An initial pause of at least 500μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. These must be either $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ irefresh cycles. After the initialization cycles the DRAM is ready for normal use.
2. 1024 refreshes are required every 16ms. A burst of eight consecutive refreshes are allowed to keep t_{RAS}= 16ms average.
3. All AC timings assume t_T(max.)= 5ns. If the actual t_T is greater than t_T(max.), then the cycle times need to be greater than that specified by the amount each transition exceeds t_T(max.). HY524400 will support a t_T up to 50ns. The transition time is defined between the V_{IH} and V_{IL}. All timings are refrenced to a V_{IL} or V_{IH}.
4. t_{RCD}(max.) is specified as a reference point only. If t_{RCD}> t_{RCD}(max.), then this parameter is increased by the amount exceeds t_{RCD}(max.)
5. t_{RAC}, t_{CAC}, t_{AA} and t_{OEA} must be satisified to guarantee access. Please check that all parameters are met for your application.
6. Access assumes a load equivalent to 100pF.
7. t_{RAD} is specified as a reference point only. If t_{RAD}> t_{RAC}-t_{AA}, then the access is increased by the difference.
8. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to the output voltage levels.
9. Data in set-up and holds are measured from the later of falling signal $\overline{CAS}$ or $\overline{WE}$.
10. t_{CP},t_{CSR},t_{WRP} and t_{WRH} all need to be valid for CBR users.
11. A 5ns delta is used between data reaching high impedance and having valid data in for these numbers.

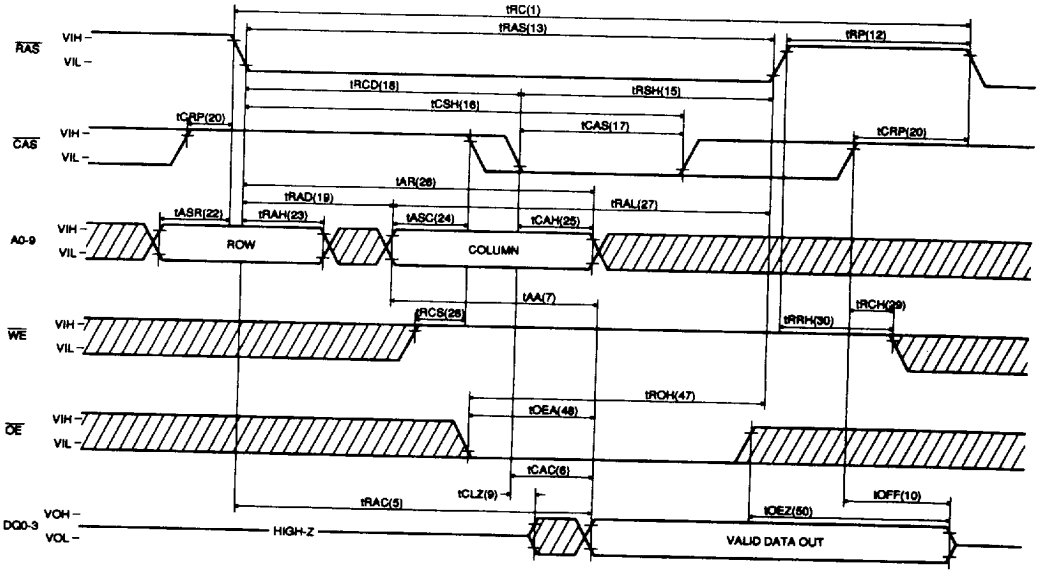
CAPACITANCE

(T_A= 25°C, V_{CC}= 0V± 10%, V_{SS}= 0V, f= 1MHz, unless otherwise noted.)

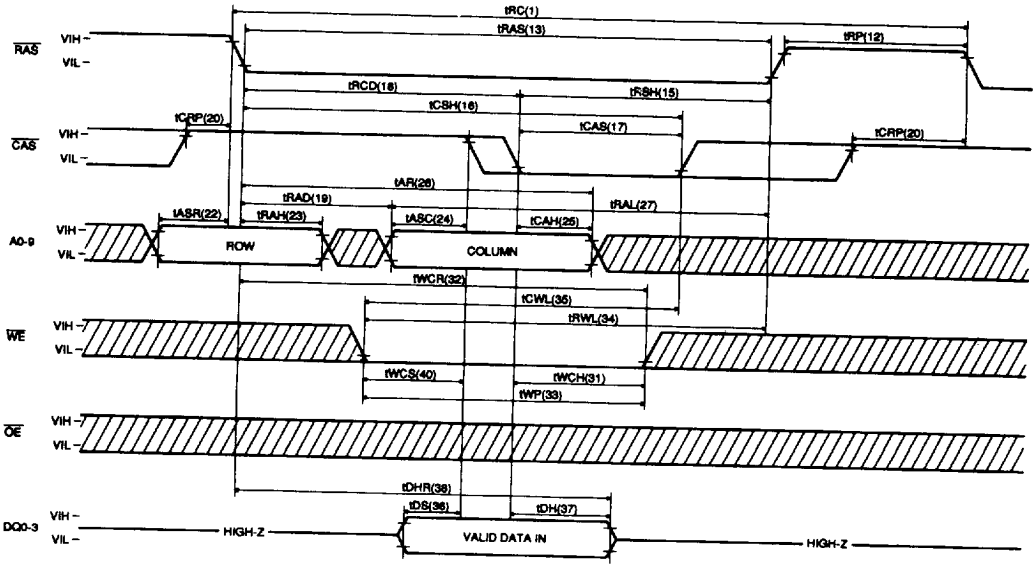
SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance (A0-A9, D)	-	5	pF
C_{IN2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	-	5	pF
C_{OUT}	Output Capacitance (Q)	-	8	pF

TIMING DIAGRAM

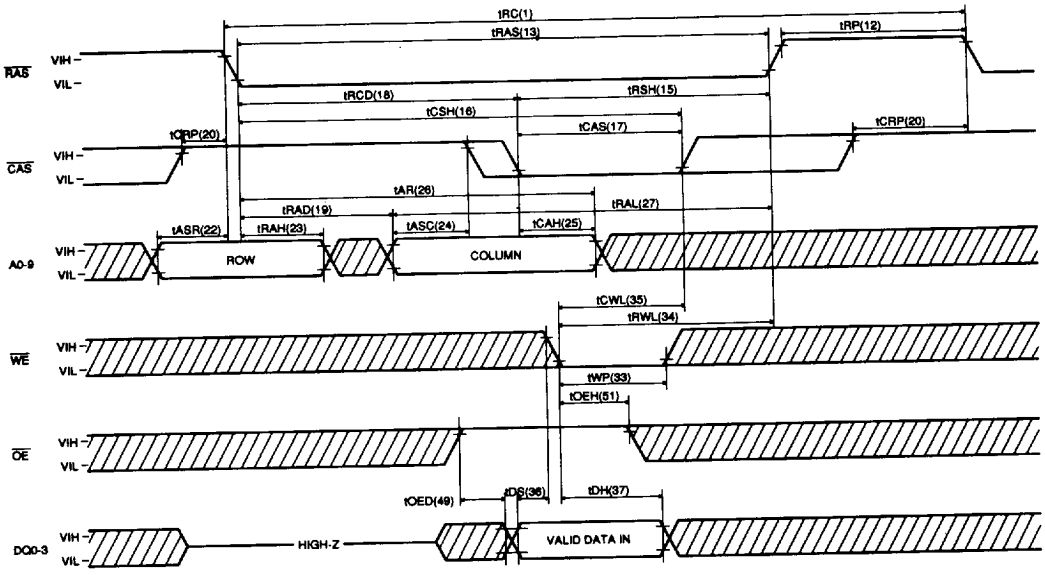
READ CYCLE



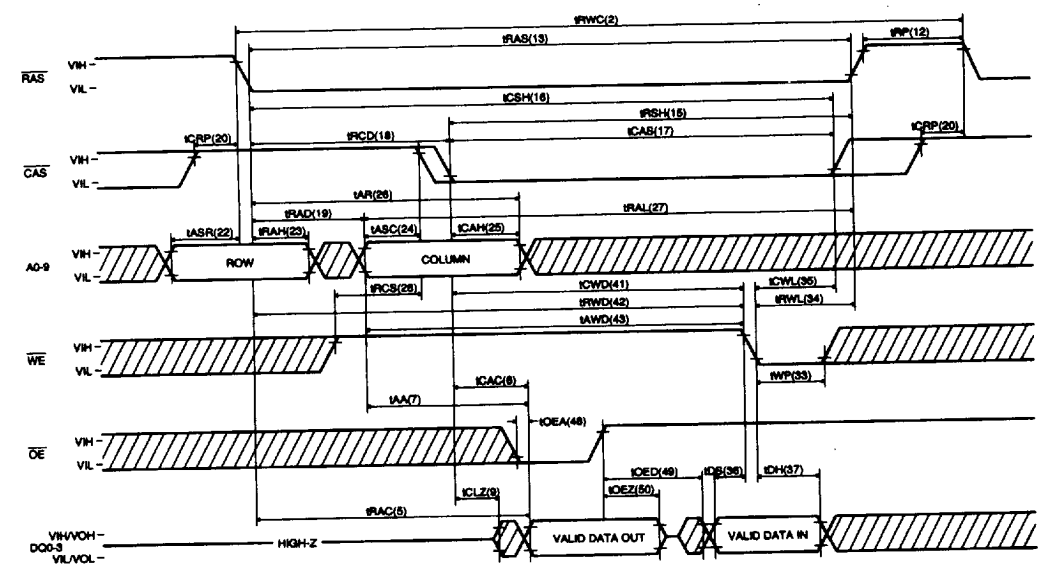
EARLY WRITE CYCLE



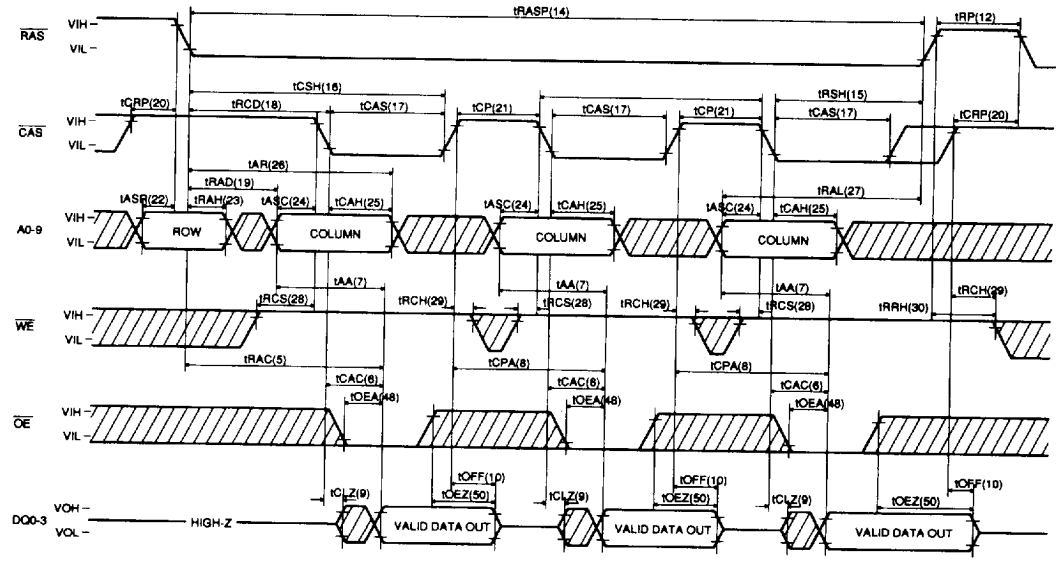
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



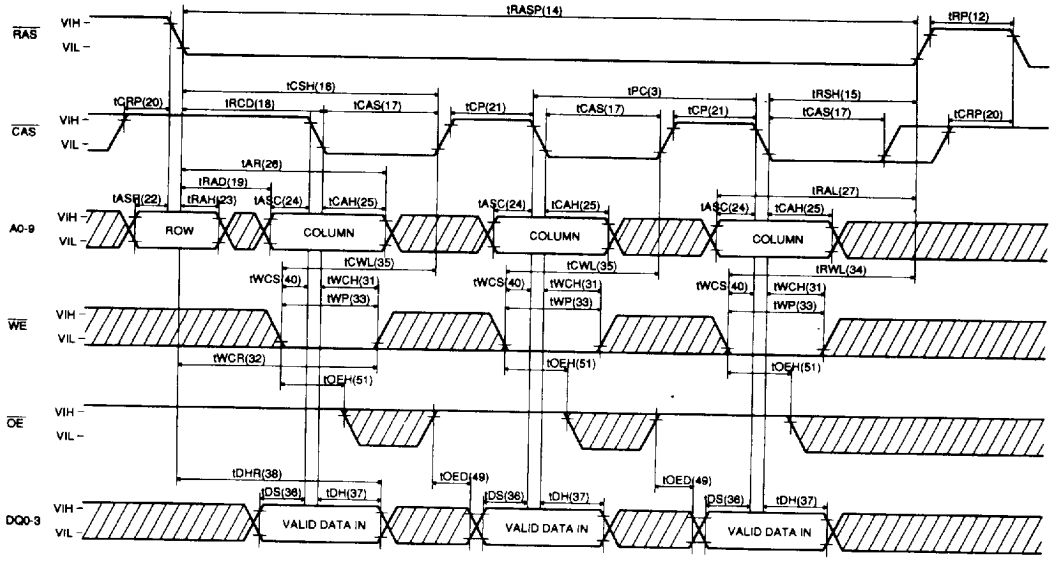
READ-MODIFY-WRITE CYCLE



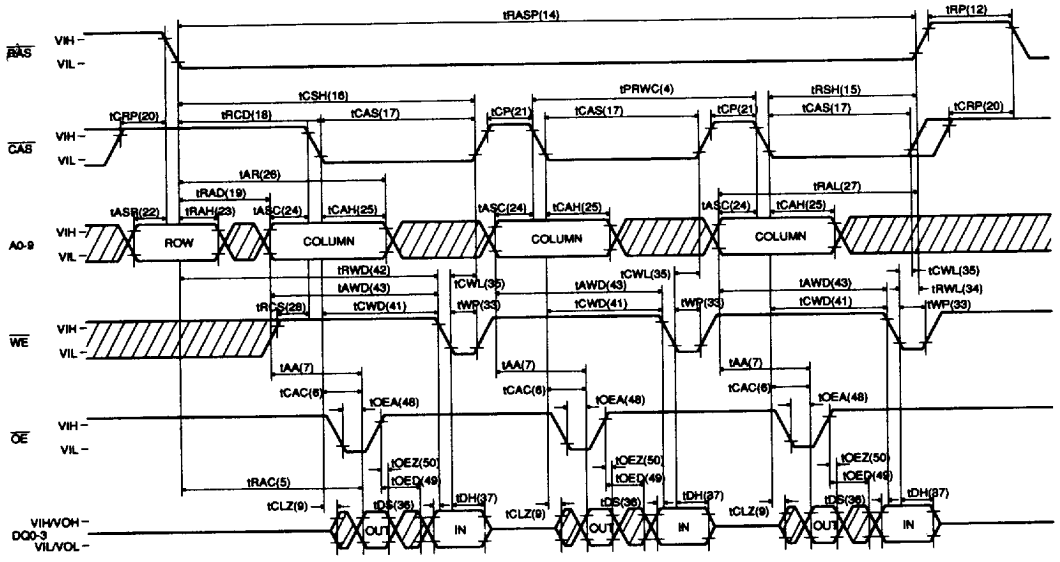
FAST PAGE MODE READ CYCLE



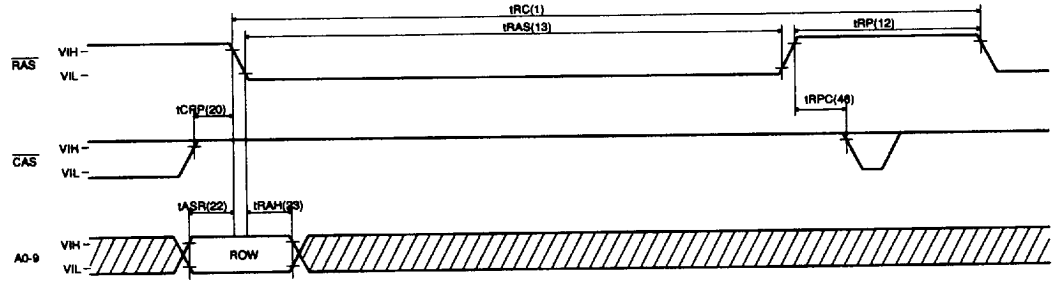
FAST PAGE MODE EARLY WRITE CYCLE



FAST PAGE MODE READ-MODIFY-WRITE CYCLE

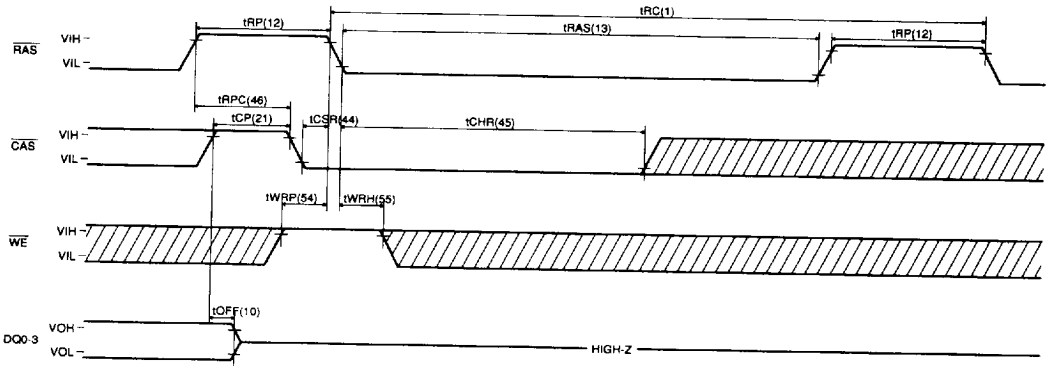


RAS-ONLY REFRESH CYCLE



NOTE : $\overline{OE}$ and $\overline{WE}$ = "H" or "L"

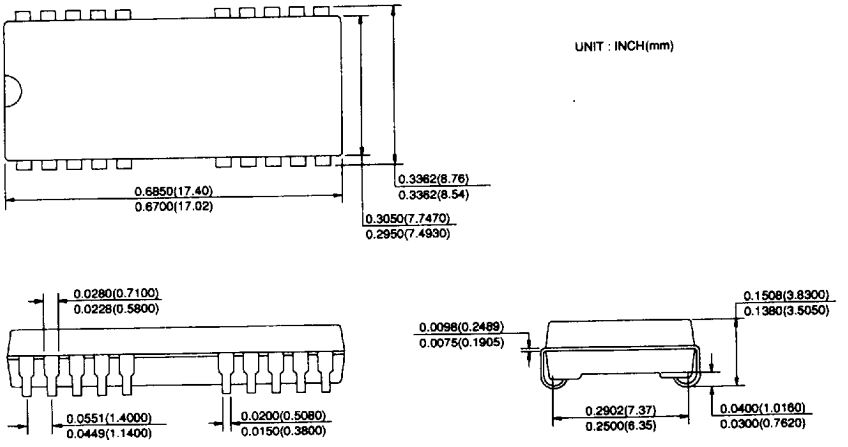
CAS-BEFORE-RAS REFRESH CYCLE



NOTE : A0-9 and $\overline{OE}$ = "H" or "L"

PACKAGE INFORMATION

300 mil 20/26 pin Small Outline J-form Package (J)



ORDERING INFORMATION

PART NO	SPEED	POWER	PACKAGE
HY524400J	70/80/10		SOJ