Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS ECL STATIC RAM 64K (64K x 1-BIT) SRAM

IDT10490
IDT100490
IDT101490

FEATURES:

- 65,536-words x 1-bit organization
- Address access time: 8/10/12/15
- Low power dissipation: 420mW (typ.)
- Guaranteed Output Hold time
- Fully compatible with ECL logic levels
- Separate data input and output
- JEDEC standard through-hole and surface mount packages

DESCRIPTION:

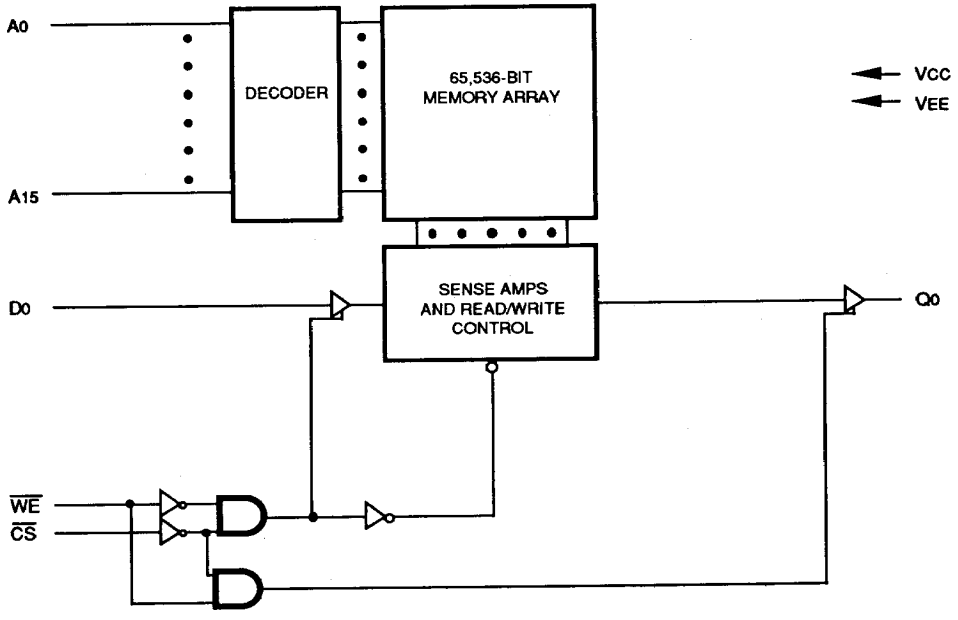
The IDT10490, IDT100490 and IDT101490 are 65,536-bit high-speed BiCEMOS™ ECL static random access memories organized as 64K x 1, with separate data inputs and outputs. All I/Os are fully compatible with ECL levels.

These devices are part of a family of asynchronous one-bit-wide ECL SRAMs. The devices have been configured to follow the standard ECL SRAM JEDEC pinout. Because they are manufactured in BiCEMOS™ technology, however, power dissipation is greatly reduced over equivalent bipolar devices.

The asynchronous SRAMs are the most straightforward to use because no additional clocks or controls are required: $Data_{OUT}$ is available an access time after the last change of address. To write data into the device requires the creation of a Write Pulse, and the write cycle disables the output pins in conventional fashion.

The fast access time and guaranteed Output Hold time allow greater margin for system timing variation. $Data_{IN}$ setup time specified with respect to the trailing edge of Write Pulse eases write timing allowing balanced Read and Write cycle times.

FUNCTIONAL BLOCK DIAGRAM



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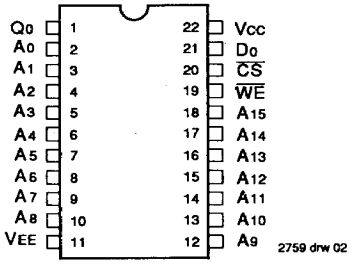
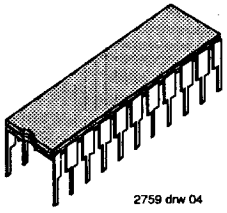
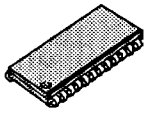
PIN CONFIGURATION



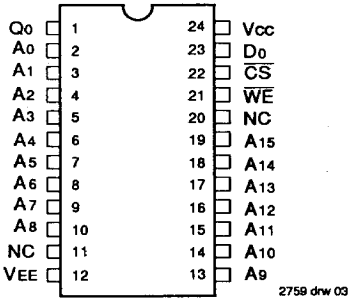
CERDIP
TOP VIEW



300-Mil-Wide
CERDIP PACKAGE
D22

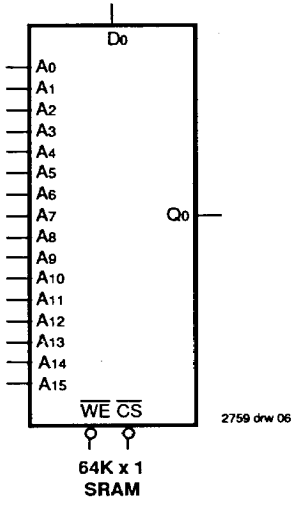


300-Mil-Wide
PLASTIC SOJ PACKAGE
Y24



SOJ
TOP VIEW

LOGIC SYMBOL



64K x 1
SRAM

PIN DESCRIPTIONS

Symbol	Pin Name
A0 through A15	Address Inputs
D0	Data Input
Q0	Data Output
$\overline{WE}$	Write Enable Input
$\overline{CS}$	Chip Select Input (Internal pull down)
VEE	More Negative Supply Voltage
VCC	Less Negative Supply Voltage

2759 tbl 01

CAPACITANCE (TA =+25°C, f=1.0MHz)

Symbol	Parameter	DIP Typ.	DIP Max.	SOJ Typ.	SOJ Max.	Unit
CIN	Input Capacitance	4	–	3	–	pF
COUT	Output Capacitance	6	–	3	–	pF

2759 tbl 03

AC OPERATING RANGES(1)

I/O	VEE	Temperature
10K	-5.2V ±5%	0 TO 75°C, air flow exceeding 2 m/sed
100K	-4.5V ±5%	0 TO 85°C, air flow exceeding 2 m/sed
101K	-4.75V to -5.46V	0 TO 75°C, air flow exceeding 2 m/sed

2759 tbl 02

NOTE:
1. Referenced to Vcc

TRUTH TABLE(1)

$\overline{CS}$	$\overline{WE}$	Data OUT	Function
H	X	L	Deselected
L	H	RAM Data	Read
L	L	L	Write

2759 tbl 04

NOTE:
1. H=High, L=Low, X=Don't Care

ECL-10K ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +75	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
		Plastic	-55 to +125	
P_T	Power Dissipation		1.5	W
I_{OUT}	DC Output Current (Output High)		-50	mA

2759 tbl 05

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-10K DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -5.2V, R_L =50Ω to -2.0V, T_A = 0 to +75°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Conditions		Min. (B)	Typ.[1]	Max. (A)	Unit	T_A
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1000 -960 -900	-885	-840 -810 -720	mV	0°C 25°C 75°C
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1870 -1850 -1830	–	-1665 -1650 -1625	mV	0°C 25°C 75°C
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1020 -980 -920	–	–	mV	0°C 25°C 75°C
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1645 -1630 -1605	mV	0°C 25°C 75°C
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs		-1145 -1105 -1045	–	-840 -810 -720	mV	0°C 25°C 75°C
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs		-1870 -1850 -1830	–	-1490 -1475 -1450	mV	0°C 25°C 75°C
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA	–
			Others	–	–	110	µA	–
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA	–
			Others	-50	–	90	µA	–
I_{EE}	Supply Current	All Inputs and Outputs Open		-170	-80	–	mA	–

2759 tbl 06

NOTES:
1. Typical parameters are specified at V_{EE} = -5.2V, T_A = +25°C and maximum loading.

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ECL-100K ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +85	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
		Plastic	-55 to +125	
P_T	Power Dissipation		1.5	W
I_{OUT}	DC Out mput Current (Output High)		-50	mA

2759 tbl 07

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-100K DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -4.5V, R_L =50Ω to -2.0V, T_A = 0 to +85°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Conditions		Min. (B)	Typ.(1)	Max. (A)	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1025	-955	-880	mV
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1810	-1715	-1620	mV
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1035	–	–	mV
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1610	mV
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs		-1165	–	-880	mV
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs		-1810	–	-1475	mV
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA
			Others	–	–	110	
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA
			Others	-50	–	90	
I_{EE}	Supply Current	All Inputs and Outputs Open		-150	-70	–	mA

2759 tbl 08

NOTE:
1. Typical parameters are specified at V_{EE} = -4.5V, T_A = +25°C and maximum loading.

ECL-101K ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +75	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
		Plastic	-55 to +125	
P_T	Power Dissipation		1.0	W
I_{OUT}	DC Out mput Current (Output High)		-50	mA

2759 tbl 09

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-101K DC ELECTRICAL CHARACTERISTICS

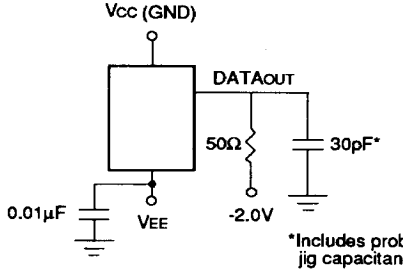
(V_{EE} = -5.2V, R_L=50Ω to -2.0V, T_A = 0 to +75°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Conditions		Min. (B)	Typ.(1)	Max. (A)	Unit
V_{OH}	Output HIGH Voltage	V_{IN} = V_{IHA} or V_{ILB}		-1025	-955	-880	mV
V_{OL}	Output LOW Voltage	V_{IN} = V_{IHA} or V_{ILB}		-1810	-1715	-1620	mV
V_{OHC}	Output Threshold HIGH Voltage	V_{IN} = V_{IHB} or V_{ILA}		-1035	–	–	mV
V_{OLC}	Output Threshold LOW Voltage	V_{IN} = V_{IHB} or V_{ILA}		–	–	-1610	mV
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs		-1165	–	-880	mV
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs		-1810	–	-1475	mV
I_{IH}	Input HIGH Current	V_{IN} = V_{IHA}	$\overline{CS}$	–	–	220	µA
			Others	–	–	110	
I_{IL}	Input LOW Current	V_{IN} = V_{ILB}	$\overline{CS}$	0.5	–	170	µA
			Others	-50	–	90	
I_{EE}	Supply Current	All Inputs and Outputs Open		-170	-80	–	mA

2759 tbl 10

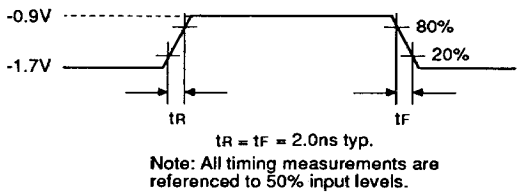
NOTE:
1. Typical parameters are specified at V_{EE} = -5.2V, T_A = +25°C and maximum loading.

AC TEST LOAD CONDITION



2759 drw 07

AC TEST INPUT PULSE



2759 drw 08

RISE/FALL TIME

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
tR	Output Rise Time	–	–	2	–	ns
tF	Output Fall Time	–	–	2	–	ns

2759 tbl 11

FUNCTIONAL DESCRIPTION

The IDT10490, IDT100490 and IDT101490 BiCMOS ECL static RAMs (SRAM) provide high speed with low power dissipation typical of BiCMOS ECL. These devices follow the conventional pinout and functionality for 64Kx1 SRAMs. The ECL -101K meets electrical specifications that combine the ECL-100K temperature and voltage compensated output levels with the high-speed of ECL-10K VEE compatibility (-5.2V).

READ TIMING

The read timing on these asynchronous devices is straightforward. DataOUT is held low until the device is selected by Chip Select ($\overline{CS}$). Then Address (ADDR) settles and data appears on the output after time tAA. Note that DataOUT is held for a short time (tOH) after the address begins to change for the next access, then ambiguous data is on the bus until a new time tAA.

WRITE TIMING

To write data to the device, a Write Pulse need be formed on the Write Enable input ($\overline{WE}$) to control the write to the SRAM array. While $\overline{CS}$ and ADDR must be set-up when $\overline{WE}$ goes low, DataIN can settle after the falling edge of $\overline{WE}$, giving the data path extra margin. Data is written to the memory cell at the end of the Write Pulse, and addresses and Chip Select must be held after the rising edge of the Write Pulse to ensure satisfactory completion of the cycle.

DataOUT is disabled (held low) during the Write Cycle. If $\overline{CS}$ is held low (active) and addresses remain unchanged, the DataOUT pins will output the written data after "Write Recovery Time" (tWR).

Because of the very short Write Pulse requirement, these devices can be cycled as quickly for Writes as for Reads. Balanced cycles mean simpler timing in cache applications.

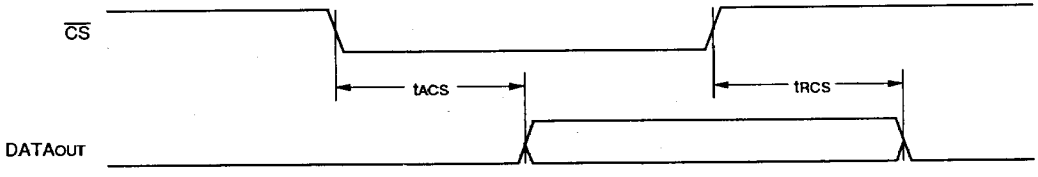
AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter[1]	Test Condition	10490S8 100490S8 101490S8		10490S10 100490S10 101490S10		10490S12 100490S12 101490S12		10490S15 100490S15 101490S15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle											
tACS	Chip Select Access Time	–	–	3	–	5	–	5	–	5	ns
tRCS	Chip Select Recovery Time	–	–	3	–	5	–	5	–	5	ns
tAA	Address Access Time	–	–	8	–	10	–	12	–	15	ns
tOH	Data Hold from Address Change	–	3	–	3.5	–	3.5	–	3.5	–	ns

2759 tbl 12

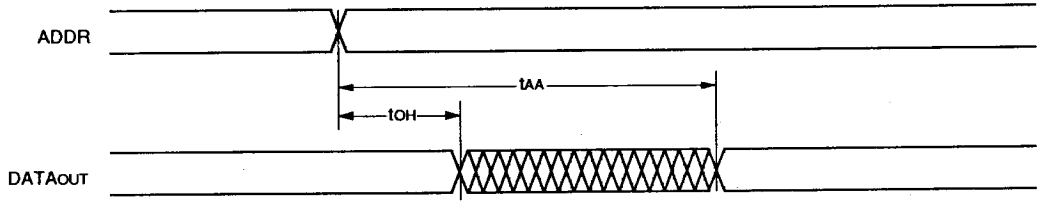
NOTES:
1. Input and Output reference level is 50% point of waveform.

READ CYCLE GATED BY CHIP SELECT



2759 drw 09

READ CYCLE GATED BY ADDRESS



2759 drw 10

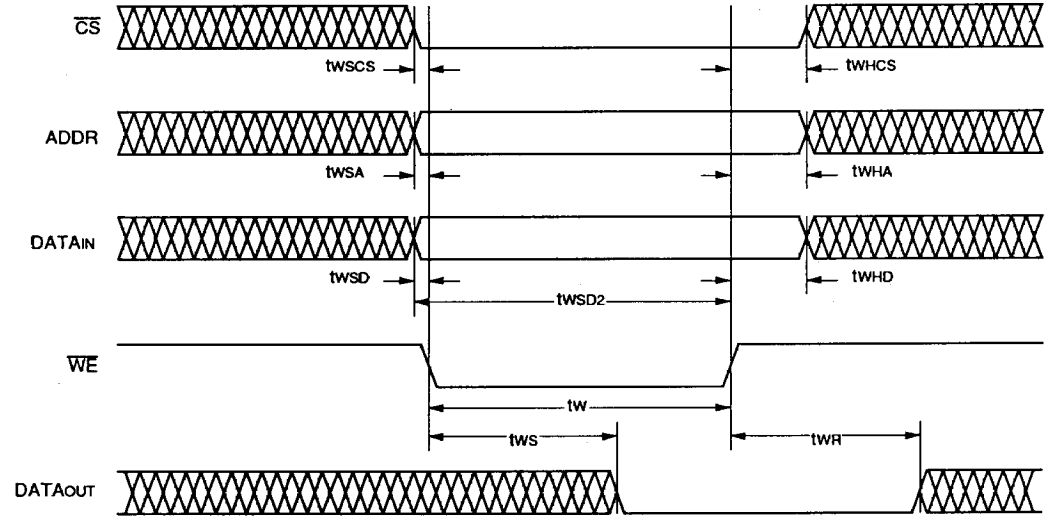
AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter[1]	Test Condition	10490S8 100490S8 101490S8		10490S10 100490S10 101490S10		10490S12 100490S12 101490S12		10490S15 100490S15 101490S15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle											
tW	Write Pulse Width	tWSA = minimum	6	–	8	–	10	–	10	–	ns
tWSD	Data Set-up Time	–	0	–	0	–	0	–	2	–	ns
tWSD2[2]	Data Set-up Time to $\overline{WE}$ High	–	5	–	5	–	5	–	5	–	ns
tWSA	Address Set-up Time	tWSA = minimum	0	–	0	–	0	–	2	–	ns
tWSCS	Chip Select Set-up Time	–	0	–	0	–	0	–	2	–	ns
tWHD	Data Hold Time	–	2	–	2	–	2	–	3	–	ns
tWHA	Address Hold Time	–	2	–	2	–	2	–	3	–	ns
tWHCS	Chip Select Hold Time	–	2	–	2	–	2	–	3	–	ns
tWS	Write Disable Time	–	–	5	–	5	–	5	–	10	ns
tWR[3]	Write Recovery Time	–	–	10	–	12	–	14	–	18	ns

2759 tbl 13

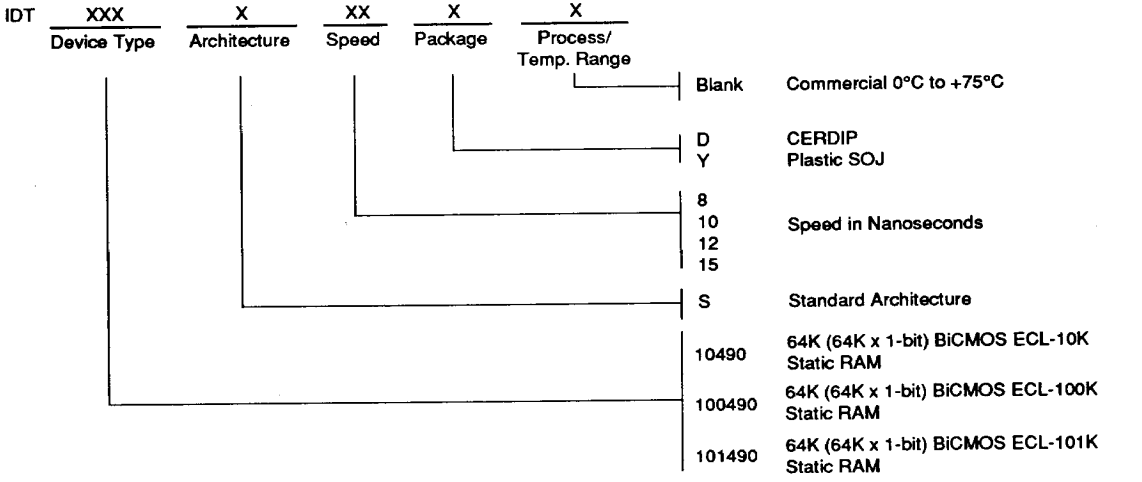
NOTES:
1. Input and Output reference level is 50% point of waveform.
2. tWSD is specified with respect to the falling edge of $\overline{WE}$ for compatibility with bipolar part specifications, but this device actually only requires tWSD2 with respect to rising edge of $\overline{WE}$.
3. tWR=tWHA + tAA and thus can include a full access time if addresses change while Chip Select is still low.

WRITE CYCLE TIMING DIAGRAM



2759 drw 11

ORDERING INFORMATION



2759 drw 12

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