

LH21256/7/8

NMOS 256K (256K × 1) Dynamic RAM

FEATURES

- 262,144 × 1 bit organization
- Access times: 100/120/150 ns (MAX.)
- Cycle times: 200/230/260 ns (MIN.)
- Page mode operation (LH21256)
Nibble mode operation (LH21257)
Byte mode operation (LH21258)
- Power supply: +5 V ± 10%
- Power consumption:
Operating: 440/440/385 mW (MAX.)
Standby: 27.5 mW (MAX.)
- TTL compatible I/O
- Built-in gated $\overline{\text{CAS}}$ function
- Separate I/O allows Early-Write action
- Available for read modify write $\overline{\text{RAS}}$ only refresh, hidden refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh
- 256 refresh cycle (refreshing time 4 ms)
- Built-in high output bias generator circuit
- Packages:
16-pin, 300-mil DIP
16-pin, 325-mil ZIP

DESCRIPTION

The LH21256/7/8 is a 262,144 word × 1 bit dynamic RAM fabricated using N-channel 2-layer polysilicon gate process technology. With multiplexed address inputs and standard 16-pin DIP/ZIP packages, it is easy to comprise memory systems with high speed, low power consumption and large memory capacity. The LH21256/7/8 operates on a single +5 V power supply. The built-in high output substrate bias generator circuit eliminates sensitivity to undershoot on the input signals.

PIN CONNECTIONS

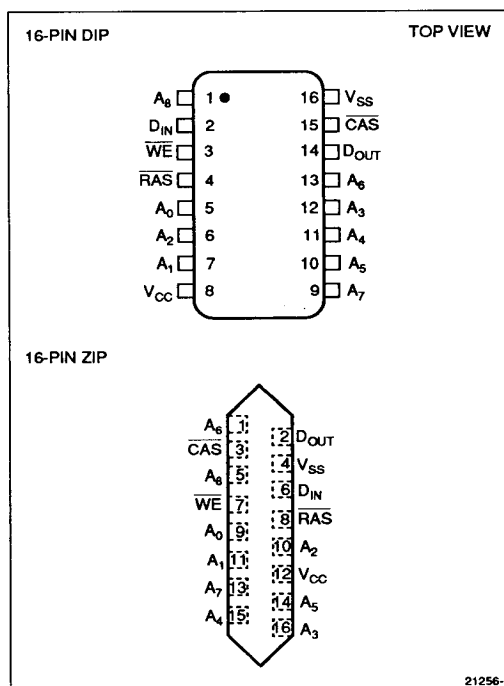


Fig. 1. Pin Connections for DIP & ZIP Packages

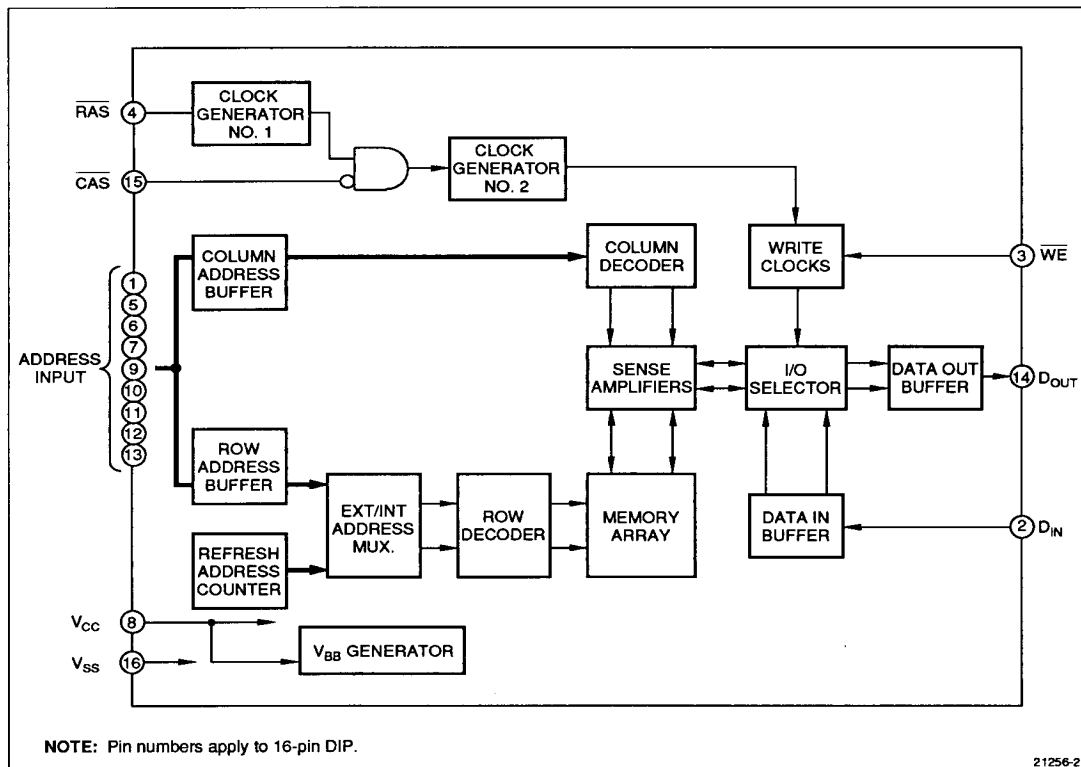


Figure 2. LH21256/7/8 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A ₀ - A ₈	Address input
$\overline{\text{RAS}}$	Row address strobe
$\overline{\text{CAS}}$	Column address strobe
$\overline{\text{WE}}$	Write enable

SIGNAL	PIN NAME
D _{IN}	Data input
D _{OUT}	Data output
V _{CC}	Power supply (+5 V)
V _{SS}	Power supply (0 V)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V _T	-1.0 to 7.0	V	1
Output short-circuit current	I _O	50	mA	
Power consumption	P _D	1.0	W	
Operating temperature	T _{opr}	0 to +70	°C	
Storage temperature	T _{stg}	-55 to +150	°C	

NOTE:

1. Referenced to V_{SS}

RECOMMENDED OPERATING CONDITIONS (TA = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage	VCC	4.5	5.0	5.5	V	1
	VSS	0	0	0		
Input voltage	V _{IH}	2.4		6.5	V	1
	V _{IL}	-1.0		0.8		

NOTE:

1. Referenced to VSS

CAPACITANCE (VCC = 5 V ± 10%, TA = 0 to +70°C, f = 1MHz)

PARAMETER	SYMBOL	MIN.	TYPICAL	MAX.	UNIT
Input capacitance	A ₀ - A ₈ , D _{IN} , WE	C _{IN1}		5	pF
	RAS, CAS	C _{IN2}		7	pF
Output capacitance	D _{OUT}	C _{OUT}		7	pF

DC CHARACTERISTICS (VCC = 5 V ± 10%, TA = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE	
Average supply current in normal operation	LH21256/7/8-10	I _{CC1}	—	80	mA	1, 2
	LH21256/7/8-12		—	80		
	LH21256/7/8-15		—	70		
Average supply current in standby mode		I _{CC2}	—	5.0	mA	1
Average supply current in RAS only refresh time	LH21256/7/8-10	I _{CC3}	—	60	mA	1, 2
	LH21256/7/8-12		—	60		
	LH21256/7/8-15		—	55		
Average supply current in page mode	LH21256-10	I _{CC4}	—	50	mA	1, 2
	LH21256-12		—	45		
	LH21256-15		—	40		
Average supply current in nibble mode	LH21257-15	I _{CC4}	—	65	mA	1, 2
	LH21257-10		—	49		
	LH21257-12		—	49		
Average supply current in byte mode	LH21258-10	I _{CC4}	—	60	mA	1, 2
	LH21258-12		—	55		
	LH21258-15		—	50		
CAS before RAS average supply current in refresh cycle	LH21256/7/8-10	I _{CC5}	—	65	mA	1, 2
	LH21256/7/8-12		—	60		
	LH21256/7/8-15		—	55		
Input leakage current	0 V ≤ V _{IN} ≤ 6.5 V 0 V on all other pins	I _{I(L)}	-10	10	μA	
Output leakage current	0 V ≤ V _{OUT} ≤ 6.5 V Output in high-impedance state	I _{O(L)}	-10	10	μA	
Output "High" voltage	I _{OUT} = -5 mA	V _{OH}	2.4	—	V	
Output "Low" voltage	I _{OUT} = 4.2 mA	V _{OL}	—	0.4	V	

NOTES:

1. The output pins are in high-impedance state.
2. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on the cycle time.

AC CHARACTERISTICS^{1, 2, 3} ($V_{CC} = 5\text{ V} \pm 10\%$, $T_A = 0\text{ to }70^\circ\text{C}$)

PARAMETER	SYMBOL	LH21256/7/8-10		LH21256/7/8-12		LH21256/7/8-15		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Random read/write cycle time	t _{RC}	200	—	230	—	260	—	ns	
Read write cycle time	t _{RWC}	240	—	275	—	310	—	ns	
Access time from $\overline{\text{RAS}}$	t _{RAC}	—	100	—	120	—	150	ns	4, 6
Access time from $\overline{\text{CAS}}$	t _{CAC}	—	50	—	60	—	75	ns	5, 6
Output turn-off delay time	t _{OFF}	0	30	0	35	0	40	ns	
Rise and fall time	t _r	3	35	3	35	3	35	ns	3
$\overline{\text{RAS}}$ precharge time	t _{RP}	85	—	100	—	100	—	ns	
$\overline{\text{RAS}}$ pulse width	t _{RAS}	100	10,000	120	10,000	150	10,000	ns	
$\overline{\text{RAS}}$ hold time	t _{RSH}	50	—	60	—	75	—	ns	
$\overline{\text{CAS}}$ precharge time	t _{CPN}	25	—	30	—	35	—	ns	
$\overline{\text{CAS}}$ pulse width	t _{CAS}	50	10,000	60	10,000	75	10,000	ns	
$\overline{\text{CAS}}$ hold time	t _{CSH}	100	—	120	—	150	—	ns	
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$)	t _{FCH}	100	—	120	—	150	—	ns	
$\overline{\text{CAS}}$ set up time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$)	t _{FCS}	10	—	10	—	30	—	ns	
$\overline{\text{RAS}}$ / $\overline{\text{CAS}}$ delay time	t _{RCD}	20	50	25	60	30	75	ns	7, 8
$\overline{\text{CAS}}$ / $\overline{\text{RAS}}$ precharge time	t _{CRP}	10	—	10	—	30	—	ns	
Row address setup time	t _{ASR}	0	—	0	—	0	—	ns	
Row address hold time	t _{RAH}	10	—	15	—	20	—	ns	
Column address setup time	t _{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t _{CAH}	25	—	25	—	45	—	ns	
Column address hold time from $\overline{\text{RAS}}$	t _{LAR}	75	—	90	—	120	—	ns	
Read command setup time	t _{RCS}	0	—	0	—	0	—	ns	
Read command hold time	t _{RCH}	0	—	0	—	0	—	ns	11
Read command hold time from $\overline{\text{RAS}}$	t _{RRH}	10	—	10	—	20	—	ns	11
Write command setup time	t _{WCS}	0	—	0	—	0	—	ns	10
Write command hold time	t _{WCH}	35	—	40	—	45	—	ns	
Write command hold time from $\overline{\text{RAS}}$	t _{WCR}	85	—	100	—	120	—	ns	
Write command pulse width	t _{WP}	35	—	40	—	45	—	ns	
Write command $\overline{\text{RAS}}$ read time	t _{RWL}	35	—	40	—	45	—	ns	
Write command $\overline{\text{CAS}}$ read time	t _{CWL}	35	—	40	—	45	—	ns	
$\overline{\text{RAS}}$ write command delay time	t _{RWD}	95	—	120	—	150	—	ns	
$\overline{\text{CAS}}$ write command delay time	t _{CWD}	45	—	60	—	75	—	ns	
Data input setup time	t _{DS}	0	—	0	—	0	—	ns	9
Data input hold time	t _{DH}	30	—	30	—	35	—	ns	9
Data input hold time from $\overline{\text{RAS}}$	t _{DHR}	80	—	90	—	110	—	ns	
Refresh time	t _{REF}	—	4	—	4	—	4	ms	
$\overline{\text{RAS}}$ precharge $\overline{\text{CAS}}$ hold time	t _{RPC}	0	—	0	—	0	—	ns	

NOTES:

- For proper operation, at least 500 μs of pause time after power-on followed by several initialization cycles (usually 8 ordinary refresh cycles) should be given.
- AC characteristics assume $t_r = 5\text{ ns}$. (t_r refers to the transition time between V_{IH} and V_{IL} .)
- Timing measurements are referenced to V_{IH} (MIN.) and V_{IL} (MAX.).
- Only when $t_{RCD} \leq t_{RCD}(\text{MAX.})$. If $t_{RCD} > t_{RCD}(\text{MAX.})$, t_{RAC} will increase by $(t_{RCD} - t_{RCD}(\text{MAX.}))$
- When $t_{RCD} \geq t_{RCD}(\text{MAX.})$.
- Load condition for 2TTL + 100 pF.
- $t_{RCD}(\text{MAX.})$ is the maximum point for t_{RCD} where $t_{RAC}(\text{MAX.})$ is ensured, and does not represent a limit of operation. If $t_{RCD}(\text{MAX.}) \leq t_{RCD}$, the access time is controlled by t_{CAC} .
- $t_{RCD}(\text{MIN.}) = t_{RAH}(\text{MIN.}) + 2t_r + t_{ASC}(\text{MIN.})$.
- t_{DS} and t_{DH} are given with respect to the fall of $\overline{\text{CAS}}$ in the Early-Write cycle and fall of $\overline{\text{WE}}$ in the read/write cycle and the Read-Modify-Write cycle.
- t_{WCS} , t_{CWD} and t_{RWD} are the specified points of the operating mode, and do not represent a limit of operation. When $t_{WCS} \geq t_{WCS}(\text{MIN.})$, it comes into early write cycle with $\overline{\text{Dout}}$ pin coming into high-impedance state. When $t_{CWD} \geq t_{CWD}(\text{MIN.})$ and $t_{RWD} \geq t_{RWD}(\text{MIN.})$, it comes into the read/write cycle with the output data becoming the information for the selection cell. Timing other than the above-mentions will give undefined value of output.
- The operation is ensured when either t_{RCH} or t_{RRH} is satisfied.

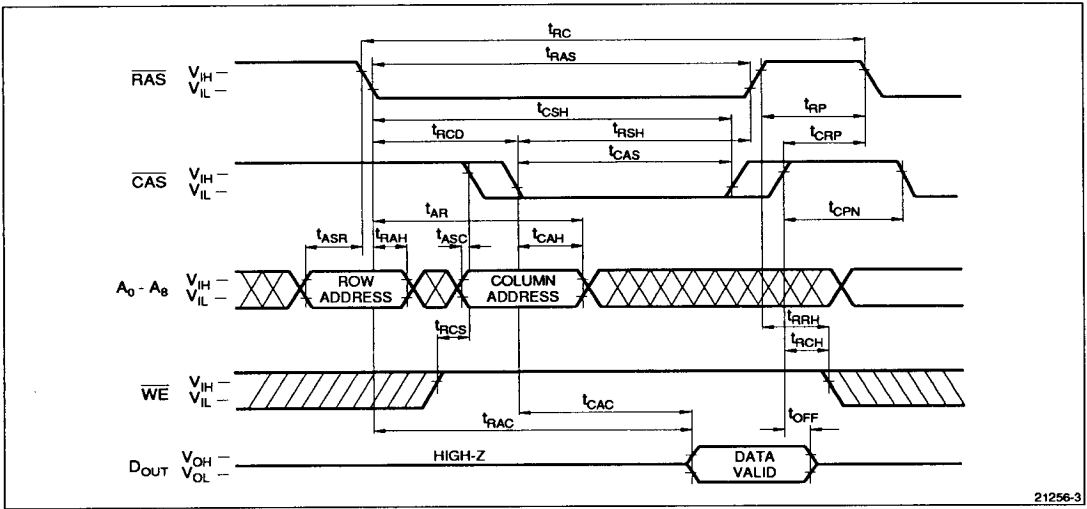


Figure 3. Read Cycle

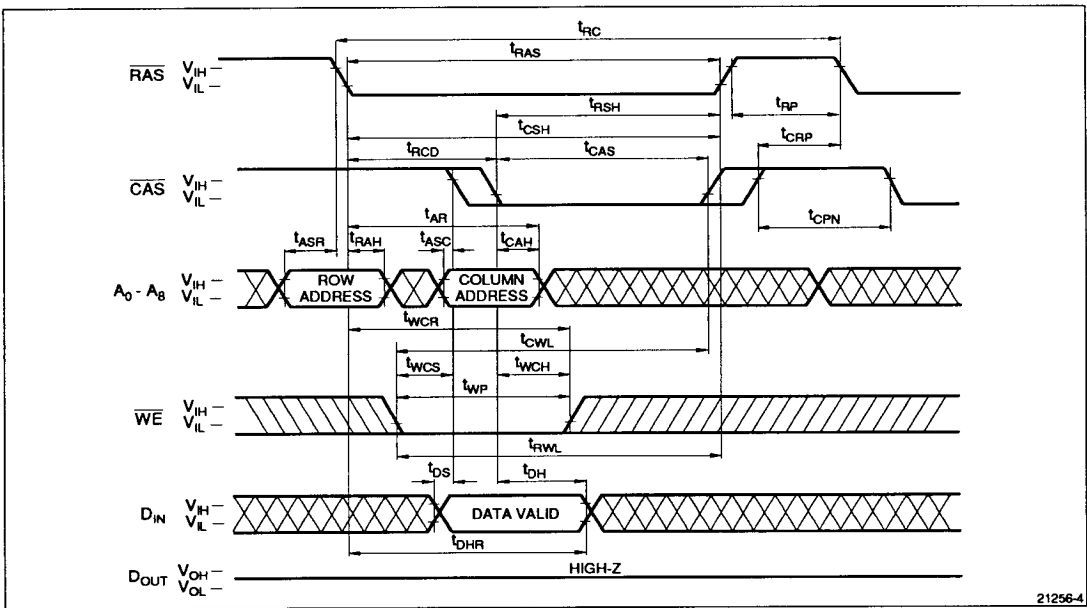
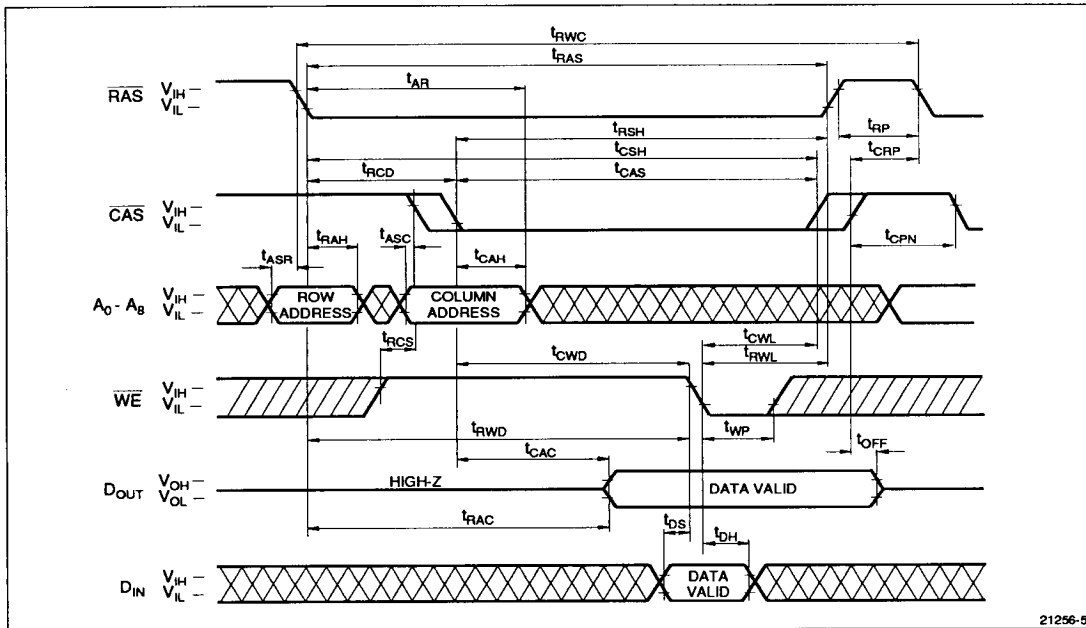
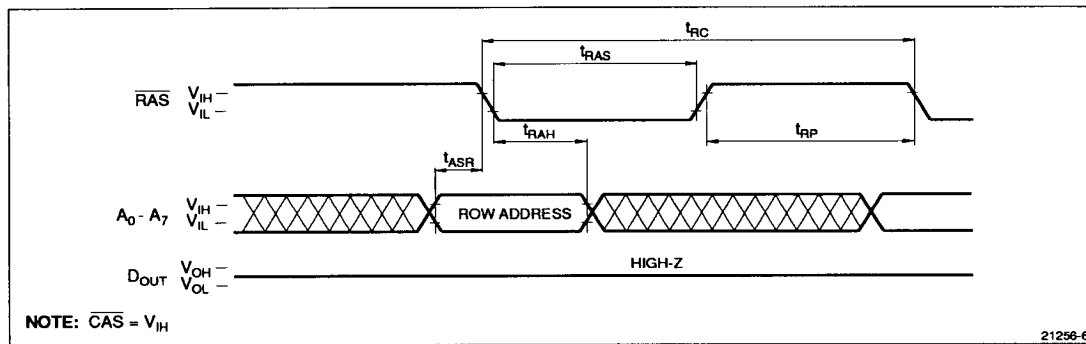


Figure 4. Write Cycle (Early Write)



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Figure 5. Read-Write/Read-Modify-Write Cycle



NOTE: $\overline{CAS} = V_{IH}$

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Figure 6. RAS Only Refresh Cycle

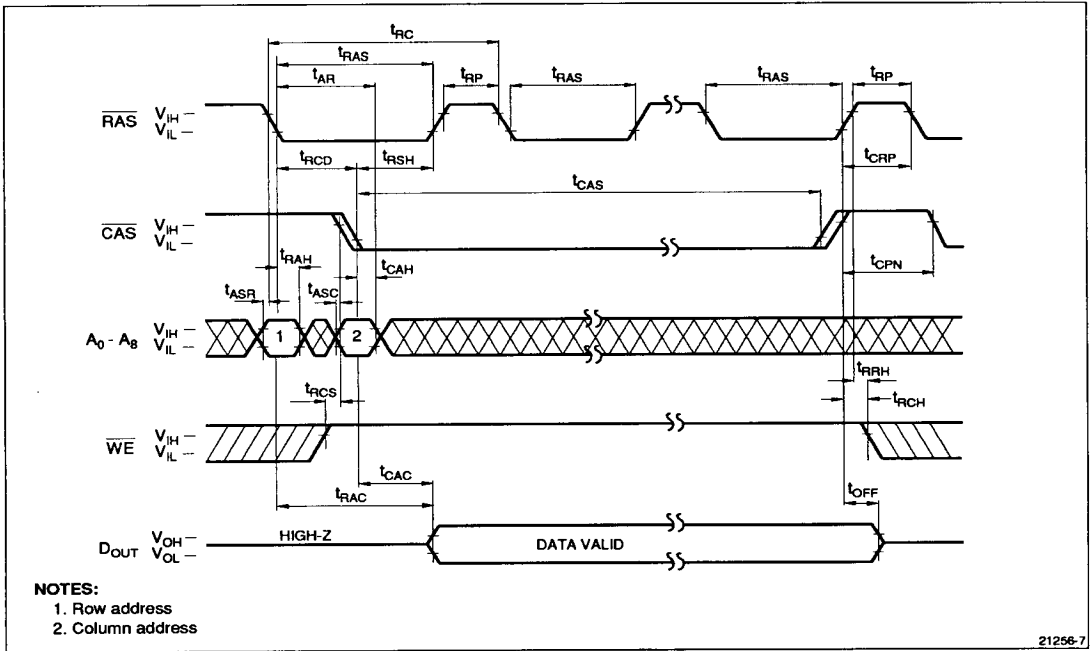


Figure 7. Hidden Refresh Cycle

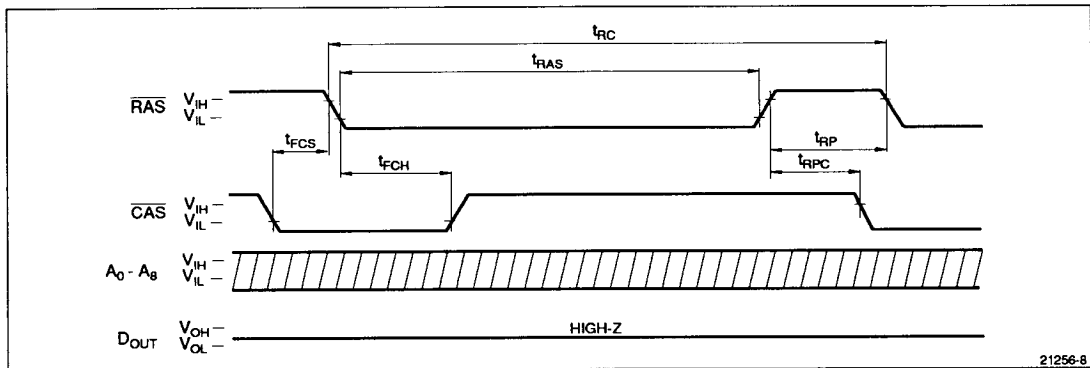
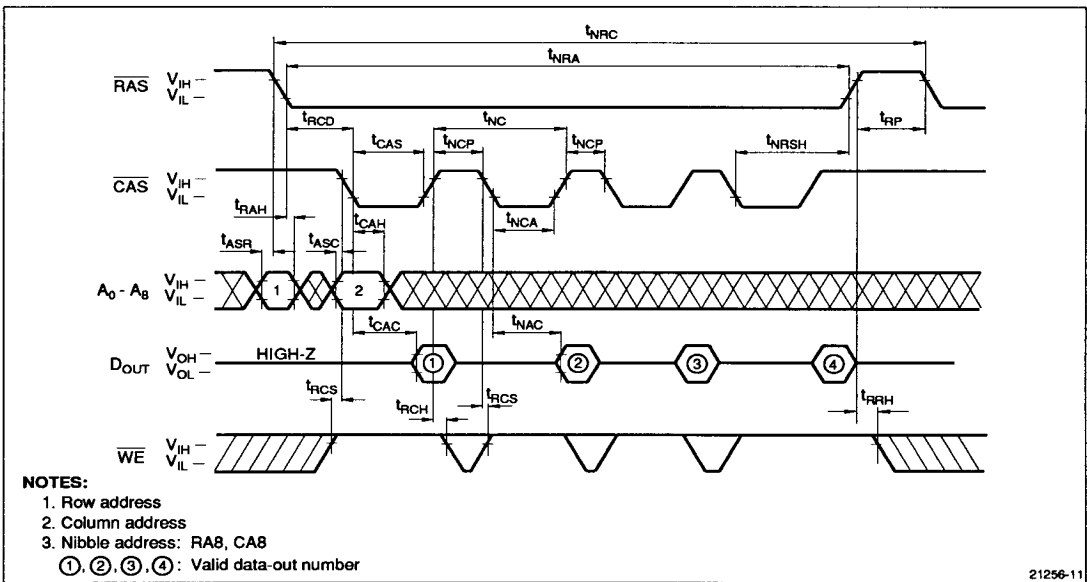


Figure 8. $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle

NIBBLE MODE CHARACTERISTICS ($V_{CC} = 5 V \pm 10\%$, $T_A = 0$ to $+70^\circ C$)

PARAMETER	SYMBOL	LH21257-10		LH21257-12		LH21257-15		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Nibble mode access time	t_{NAC}	—	25	—	30	—	35	ns	
Nibble mode \overline{RAS} cycle time	t_{NRC}	400	—	460	—	520	—	ns	
Nibble mode \overline{RAS} pulse width	t_{NRA}	300	—	350	—	410	—	ns	
Nibble mode cycle time	t_{NC}	60	—	65	—	80	—	ns	
Nibble mode \overline{CAS} precharge time	t_{NCP}	25	—	25	—	35	—	ns	
Nibble mode \overline{CAS} pulse width	t_{NCA}	25	—	30	—	35	—	ns	
Nibble mode \overline{RAS} hold time	t_{NRSH}	45	—	50	—	55	—	ns	
Nibble mode $\overline{CAS}/\overline{WE}$ delay	t_{NCWD}	15	—	20	—	25	—	ns	
Nibble mode write command \overline{CAS} lead time	t_{NCWL}	20	—	25	—	25	—	ns	
Nibble mode write command \overline{RAS} lead time	t_{NRWL}	40	—	45	—	55	—	ns	
Nibble mode write command pulse width	t_{NWP}	20	—	25	—	35	—	ns	



21256-11

Figure 11. Nibble Mode Read Cycle

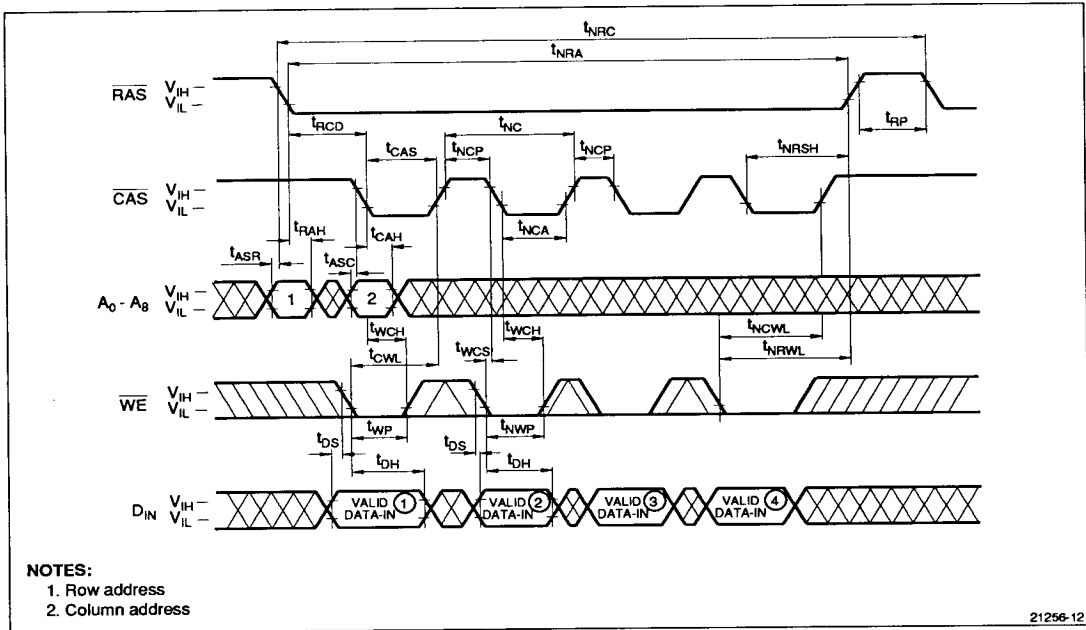


Figure 12. Nibble Mode Write Cycle

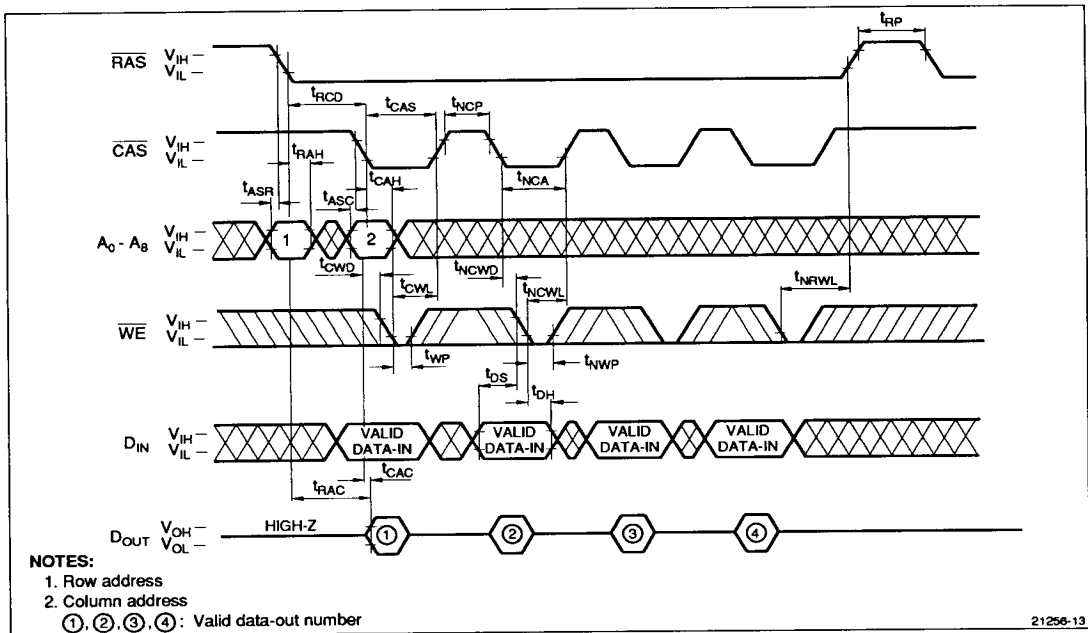


Figure 13. Nibble Mode Read-Modify-Write Cycle

BYTE MODE CHARACTERISTICS ($V_{CC} = 5\text{ V} \pm 10\%$, $T_A = 0\text{ to }+70^\circ\text{C}$)

PARAMETER	SYMBOL	LH21258-10		LH21258-12		LH21258-15		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Byte mode access time	t_{BAC}	—	25	—	30	—	35	ns	
Byte mode $\overline{\text{RAS}}$ cycle time	t_{BRC}	640	—	740	—	840	—	ns	
Byte mode $\overline{\text{RAS}}$ pulse width	t_{BRA}	540	—	630	—	730	—	ns	
Byte mode cycle time	t_{BC}	60	—	70	—	80	—	ns	
Byte mode $\overline{\text{CAS}}$ precharge time	t_{BCP}	25	—	30	—	35	—	ns	
Byte mode $\overline{\text{CAS}}$ pulse width	t_{BCA}	25	—	30	—	35	—	ns	
Byte mode $\overline{\text{RAS}}$ hold time	t_{BRSH}	45	—	50	—	55	—	ns	
Byte mode $\overline{\text{CAS}}$, $\overline{\text{WE}}$ delay	t_{BCWD}	15	—	20	—	25	—	ns	
Byte mode write command $\overline{\text{CAS}}$ lead time	t_{BCWL}	20	—	25	—	25	—	ns	
Byte mode write command $\overline{\text{RAS}}$ lead time	t_{BRWL}	40	—	45	—	55	—	ns	
Byte mode write command pulse width	t_{BWP}	20	—	25	—	35	—	ns	

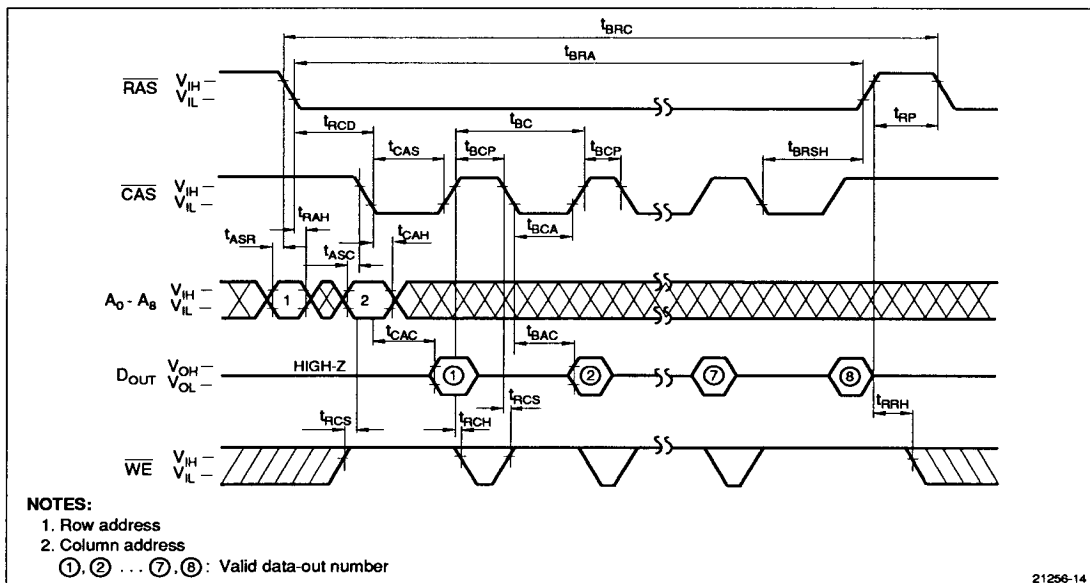


Figure 14. Byte Mode Read Cycle

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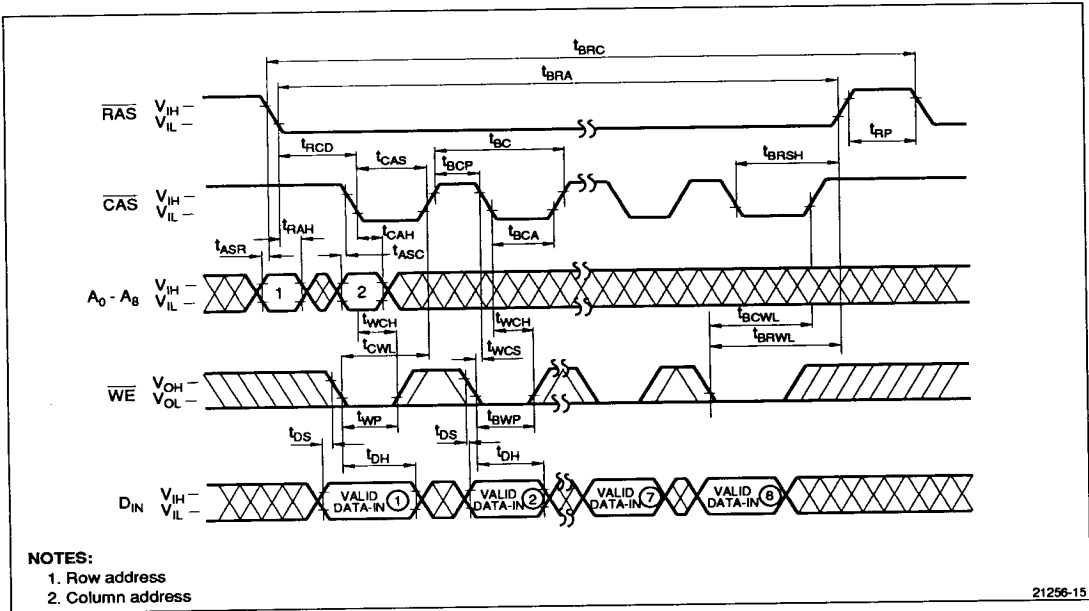


Figure 15. Byte Mode Write Cycle

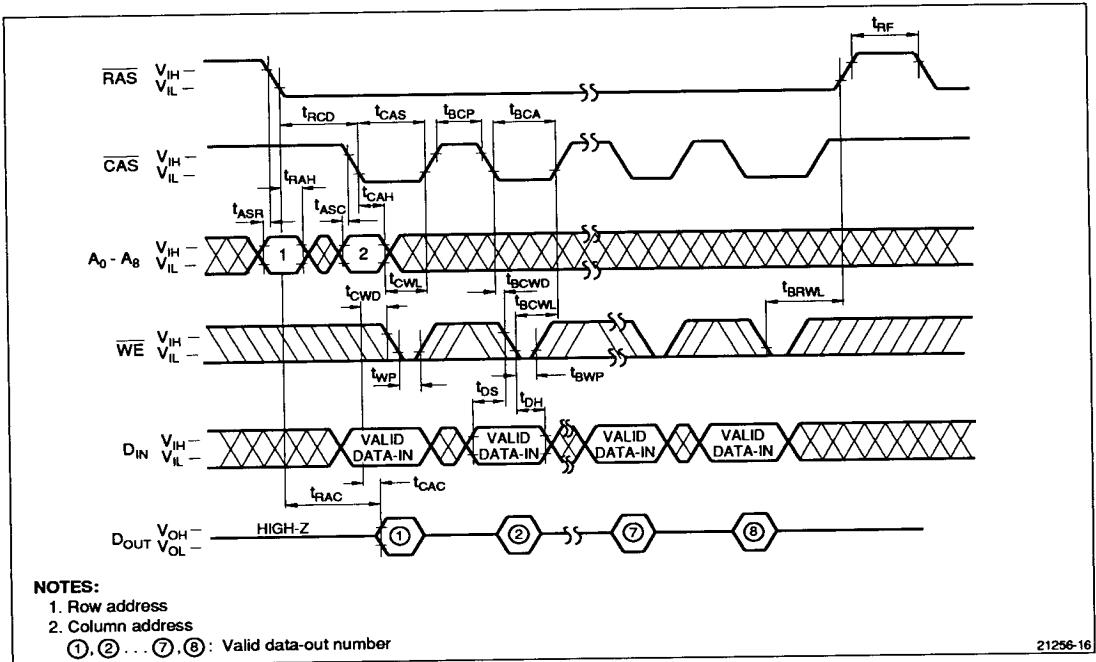


Figure 16. Byte Mode Read-Modify-Write Cycle

ORDERING INFORMATION

