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# SSI 32M7010
## Hall-Sensorless Motor Speed Control
## Preliminary Data

February 1992

## DESCRIPTION

The (Spindle) Motor Speed Control in conjunction with several external components, provides starting, accelerating, and precise rotational speed regulation functions. Different circuit versions are provided to control 4-, 8-, or 12-pole brushless DC motors without the need for Hall sensors. Control is accomplished via five pins and operation is monitored via two pins. The complete speed regulation control loop is contained in the circuit and the companion microprocessor is only required during start and to monitor status.

Motor speed control is accomplished by measuring the period of each revolution with a 500 kHz clock signal (SYSCLK divided by four). Period resolution is therefore 2 microseconds with the desired period being 8333 counts (16.66 milliseconds, or 3600.144 RPM).

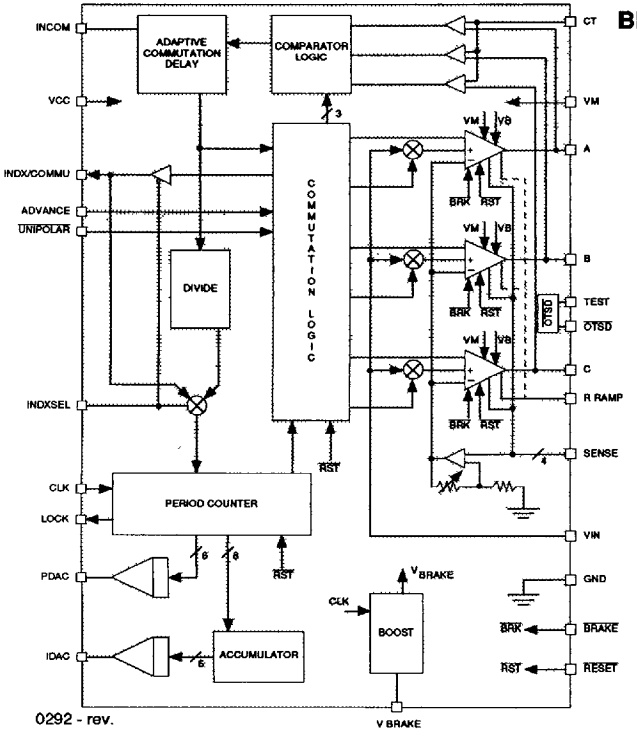
Motor armature position is determined by monitoring the coil voltage of the winding that is not presently being driven by the drivers. The back-emf at the coil in conjunction with the state of the output drivers, indicates armature position. The back emf is compared to a reference (CT) and initiates commutation when the

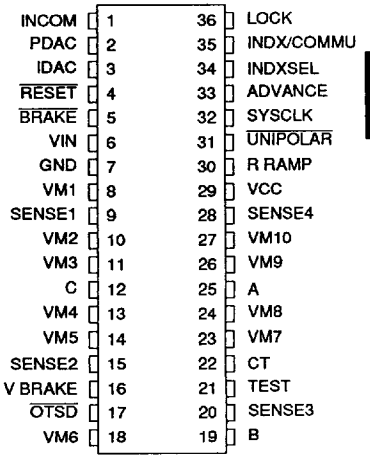
(continued)

## FEATURES

- **Precise speed control**
- **1 amp peak drivers**
- **No blocking diode**
- **Adaptive commutation delay**
- **Commutation transient suppression**
- **Convenient Retract / Brake Control**

## BLOCK DIAGRAM




**36-Pin SOM**
**PIN DIAGRAM**

CAUTION: Use handling procedures necessary for a static sensitive component.

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**TABLE 1: Output Driver States**

| STATE | COMMU | PULL DOWNS A | B | C | PULL UP UPA | UPB | UPC |
|---|---|---|---|---|---|---|---|
| 0, (Reset State) | 1 | off | on, (off) | off | on | off | off |
| 1 | 0 | off | off | on | on | off | off |
| 2 | 1 | off | off | on | off | on | off |
| 3 | 0 | on | off | off | off | on | off |
| 4 | 1 | on | off | off | off | off | on |
| 5 | 0 | off | on | off | off | off | on |

## DESCRIPTION (Continued)

appropriate comparison is made. Because the back-emf comparison event occurs prior to the time when optimum commutation should occur, commutation is delayed by a predetermined time after the comparison. The commutation delay is provided by a circuit which measures the interval between comparison events and delays commutation by a time equal to 0.43 of the prior interval. (The delay is set at 0.43 not 0.50 in order to compensate for commutation delays and motor current build-up time.) The circuit is adaptive and will provide the optimum delay for a wide range of motor speeds. Since the commutation of motor coils typically causes transients, the circuit also provides a noise blanking function which prevents response to back-emf comparison events for a period of time equal to 5/7 of the interval (between events) after the comparison event. The commutation delay can be externally modified by ±15% with the INCOM pin. The commutation states are shown in Table 1.

The period counter is loaded with a count of 8333 initially, and the period measurement results in residual counts (ideally zero) in the period counter as it counts down during the index to index time. The residual count is fed to the proportional DAC (5 bits plus sign). When there is no period error the PDAC will output 1/2 full scale (2.25/2 volts) from PDAC, too short a period will output a lower voltage, and too long a period will output a higher voltage, each depending on the amount of period error. When the residual count is within ± 15 counts of zero, the motor status is indicated as "in lock." The lower eight bits of the period counter are fed to an accumulator which adds the present period residue to the previous accumulation thus accomplishing an integrating effect which forces the speed error to zero over time. The upper six bits of the accumulator are fed to the integral DAC whose output is IDAC. Gross period errors will cause PDAC and IDAC to saturate at the appropriate extremes to achieve the maximum corrective control voltage.

The outputs PDAC and IDAC are connected to VIN with an external resistor network. The resistor values are selected to set the required loop response based on motor and system requirements. Input pin VIN is the non-inverting input of a linear transconductance amplifier which uses the lower driver transistor that is presently active per the commutation state as the power driver element. An external resistor is used to sense the current in the drive transistor source (and hence the motor coil current). The voltage across the sense resistor is amplified by a gain stage (Av=8) and fed to the inverting input of the transconductance output stage.

When the speed error is more than 3% slow, 2.25 volts is selected as the control voltage in lieu of VIN. Maximum motor current is limited to a value such that Imotor ≤ 2.25V/ (4 • $R_{SENSE}$).

Four operating conditions are selected via $\overline{BRAKE}$ and $\overline{RESET}$. With $\overline{BRAKE}$ and $\overline{RESET}$ asserted (low), outputs A, B, and C are low impedance to ground, (without current limiting function) and analog circuits are de-biased. This is the "sleep" condition. It also provides dynamic braking to the motor. With $\overline{BRAKE}$ asserted, and $\overline{RESET}$ de-asserted, drivers are low impedance to ground (without current limit function) and the analog circuitry is biased. For $\overline{RESET}$ asserted, $\overline{BRAKE}$ de-asserted, the output drivers are in a high impedance state. This will allow the user to take energy from the back-emf of a spinning motor for retracting heads. Normal operation is given for $\overline{BRAKE}$ and $\overline{RESET}$ de-asserted.

## DESCRIPTION (Continued)

**TABLE 2: Rout Low to SENSE**

| $\overline{\text{BRAKE}}$ | $\overline{\text{RESET}}$ | CONDITION | ANALOG | COUNTERS | A, B, C |
|---|---|---|---|---|---|
| 0 | 0 | SLEEP/BRAKE | OFF | RESET | Rout low to SENSE |
| 0 | 1 | BRAKE | ON | ACTIVE | Rout low to SENSE |
| 1 | 0 | RETRACT | ON | ACTIVE | FLOAT |
| 1 | 1 | RUN | ON | ACTIVE | ACTIVE |

Motor starting is accomplished with a companion microprocessor utilizing ADVANCE, $\overline{\text{RESET}}$ and COMMU. The microprocessor can assert $\overline{\text{RESET}}$ to initialize the commutation counter and then increment the counter with ADVANCE. ADVANCE at logic high excludes internal commutations. COMMU provides feedback to the microprocessor on motor activity.

## PIN DESCRIPTION

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| $\overline{\text{RESET}}$ | I | When asserted low, internal counters and registers are cleared. Refer to Table 2. |
| $\overline{\text{BRAKE}}$ | I | $\overline{\text{BRAKE}}$ is used to provide a delay between the initiation of Fault-induced head retract and motor braking. A capacitor to ground and a resistor to $\overline{\text{RESET}}$ are selected such that 1.2•R•C is equal to the maximum time required for retract. |
| SYSCLK | I | Reference frequency for motor speed measurement. A 2.000 MHz SYSCLK will result in 3600 RPM motor speed for 8-pole motors. SYSCLK can be set to other frequencies to obtain a different rotational speed or operate with motors other than 8-pole configurations (use of an external index signal is only valid for 8-pole motors). |
| INDX/COMMU | I/O | When selected with INDXSEL set high, this pin is used to provide a once-per-revolution indication of rotational position and speed to the circuit. With INDXSEL low, COMMU (the LSB of the commutation counter) is presented as an output. |
| INDXSEL | I | See above. |
| LOCK | O | When the motor period is within ±15 counts of nominal, the motor is indicated as "in lock" with LOCK high. |
| ADVANCE | I | ADVANCE is used to increment the commutation counter. The rising edge of ADVANCE will increment the counter. ADVANCE held high will inhibit internal incrementing of the counter, ADVANCE held low permits the normal operation of commutation from back-emf events. |
| VM 1 - 10 | - | Motor Power Supply. |

**PIN DESCRIPTION** (continued)

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| INCOM | I | Adaptive commutator delay test point. |
| PDAC | O | Proportional DAC output pin. The proportional channel output is the lowest 5 bits plus sign of the period measuring counter. The LSB signifies a 2 microsecond period variation for SYSCLK = 2.00 MHz. |
| IDAC | O | Integral DAC output pin. The integral channel output comes from the upper six bits of an eight bit accumulator. The accumulator adds the lower eight bits of the period measurement to the previous value obtained from prior period measurements and accumulations. |
| VIN | I | Control Voltage input pin. The internal driver transistors and internal predriver circuits form a transconductance amplifier which will set motor current in relation to VIN. In conjunction with the SENSE input and the gain of the sense amplifier, transconductance (Gm) will be: Gm = Im/VIN = 1/ (Rs • 8). |
| SENSE1<br>SENSE2<br>SENSE3<br>SENSE4 | I | Current monitoring sense amplifier (high side) input pin. The lower driver transistor current (hence motor current) is sent through a current sensing resistor to monitor motor current. The circuit will control the voltage across this resistor (multiplied by the gain of 8 in the sense amplifier) to match either VIN (during normal operation) or internal 2.25V (during low-speed operation with Av = 4). |
| A, B, C | O | Motor Drive Outputs. These pins provide drive to the motor coils. |
| CT | I | Back-EMF input from motor coil center tap. Input connected to the center tap for sensing generated back-emf voltages. The circuit uses the back-emf voltages to determie rotor position and effect commutation. |
| VCC | - | 5V power pin. |
| V BRAKE | O | External capacitor to store charge for driver circuitry. The stored charge is used by the lower drivers in fault conditions to achieve dynamic braking. |
| GND | - | Ground connection. GND is the low side input to the current SENSE amplifier and care should be taken to see that GND and the low side of the sense resistor are at the same potential. |
| $\overline{\text{OTSD}}$ | O | Indicates over temperature condition. |
| R RAMP | I | External resistor. Sets DV/DT for lower driver turn-off. DV/DT is approximately 4E 10 • R RAMP. |
| $\overline{\text{UNIPOLAR}}$ | I | Select line for Unipolar or Bipolar mode. |

## ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

(Exposure to conditions in excess of the conditions given below may result in permanent damage or affect device reliability.)

| PARAMETER | | RATING |
|---|---|---|
| Supply Voltage | VCC | -0.3 to 7V |
| | VM | -0.3 to 15V |
| Digital Inputs/Outputs | SYSCLK, ADVANCE INDXSEL, INDX/COMMU, LOCK | -0.3 to VCC +0.3V |
| Analog I/O | PDAC, IDAC, VIN | -0.3 to VCC +0.3V |
| Motor Interface Voltage | CT, A, B, C, $\overline{\text{BRAKE}}$, SENSE, $\overline{\text{RESET}}$ | -0.3 to 20V |
| Motor Interface Current | A, B, C, VM, SENSE | -1.0 to +1.0A |
| Storage Temperature, Tstg | | -65 to 150°C |
| Lead Temperature, Tlead | | 300°C |

### RECOMMENDED OPERATING CONDITIONS

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Supply Voltage | VCC | | 4.75 | | 5.25 | V |
| | VM | | 4.75 | | 5.25 | V |
| Supply Current | ICC | | 1.0 | | 10.0 | mA |
| | ICC, Sleep Mode | | 0.05 | | 1.0 | mA |
| | IVM | | 0 | | 0.75 | A |
| | IVM, Sleep Mode | | 0.1 | | 1.5 | mA |
| Ambient Temperature | Ta | | 0 | | 70 | °C |
| Capacitive Load Digital I/O | Cl | | 0 | | 100 | pF |
| Resistive Load PROP, INTEGRAL | Rla | | 5000 | | | Ω |
| Capacitive Load PROP, INTEGRAL | Cla | | 0 | | 40 | pF |

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## ELECTRICAL SPECIFICATIONS (Continued)

### DIGITAL INPUTS

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Fmax, SYSCLK | | | | 4.5 | MHz |
| Twh, Twl, SYSCLK width high or low | | 40 | | | ns |
| External Index, INDX/COMMU (as input) Pulse Width | | 200 | | | ns |
| Input Leakage, INDX/COMMU | | | | 10 | µA |
| Input Leakage, others | | | | 1 | µA |
| Vil (EXTINDX, SYSCLK, ADVANCE, INDXSEL) | | | | 0.8 | V |
| Vih (inputs above) | | 2.0 | | | V |
| Vil ($\overline{\text{RESET}}$, $\overline{\text{BRAKE}}$) | VBRAKE ≥ 4.5V | | | 0.8 | V |
| Vih ($\overline{\text{RESET}}$, $\overline{\text{BRAKE}}$) | VBRAKE ≥ 4.5V | 2.0 | | | V |

### PROPORTIONAL (PDAC), INTEGRAL (IDAC) OUTPUTS

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Output Voltage | Iout ≤ 0.1 mA<br>VCC = 5.0 V | 0 | | 2.25V ±5% | V |
| DAC Step Size | VCC = 5.0V | 0.32 | | 0.39 | V |
| Output Impedance | 0.5V ≤V out <2.0V<br>Iout = 0.10 mA | | | 200 | Ω |
| Kp, Porportional Gain | | 0.70 | | 0.85 | V/rad/s |
| Ki, Integral Gain | | 10.48 | | 12.75 | V/rad |

### DIGITAL OUTPUTS, LOCK, INDX/COMMU

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Voh | Iout = -100 µA | 2.4 | | | V |
| Vol | Iout = 2.0 mA | | | 0.4 | V |
| Tdts, Time delay to tri-state output | INDXSEL high to high impedance on INDX/COMMU | 10 | | 100 | ns |
| Tdoe, Time delay to enable as output pin | INDXSEL low to drive state | 10 | | 100 | ns |

## ELECTRICAL SPECIFICATIONS (Continued)

**VIN**

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Input Voltage | | 0 | | 2.25 | V |
| Input Current | 0 ≤ Vin < 2.5V | -1 | | +1 | µA |

**OUTPUTS A, B, C**

| | | | | | |
|---|---|---|---|---|---|
| Routup | Output in high state VM = 4.75V | 0.05 | | 1.0 | Ω |
| Routlow | Output driving low, VM = 4.75V | 0.05 | | 1.0 | Ω |

**SENSE**

| | | | | | |
|---|---|---|---|---|---|
| Vin, SENSE | Normal operation | 0.0 | | 0.4 | V |
| | Low speed operation | 0.0 | | 0.8 | V |
| Iin, SENSE | 0.0 ≤ Vin < 1.0V | -10 | | +10 | µA |
| Cin | | | | 20 | pF |
| Transconductance gain from VIN to motor current (steady-state) will be given by: G = Imotor/VIN = 1/Rsense • 8, for rotational speeds greater than 3490 RPM. | | | | | |

**CT**

| | | | | | |
|---|---|---|---|---|---|
| Rin | -0.3V ≤Vin < 15V | 30K | | | Ω |
| Cin | | | | 10 | pF |

**V BRAKE**

| | | | | | |
|---|---|---|---|---|---|
| Ibst (run) | VCC = 4.75V | | | 100 | µA |
| Ibst (float) | VCC ≤ 0.5V | | | 10 | µA |
| Ibst (brake) | VCC ≤ 0.5V | | | 10 | µA |

**OPERATING REQUIREMENTS**

| | | | | | |
|---|---|---|---|---|---|
| LOCK Indication Range | SYSCLK = 2.000 MHz, 8-pole | 3593.5 | | 3606.5 | RPM |
| Speed Resolution | | -.012 | | +0.012 | % |

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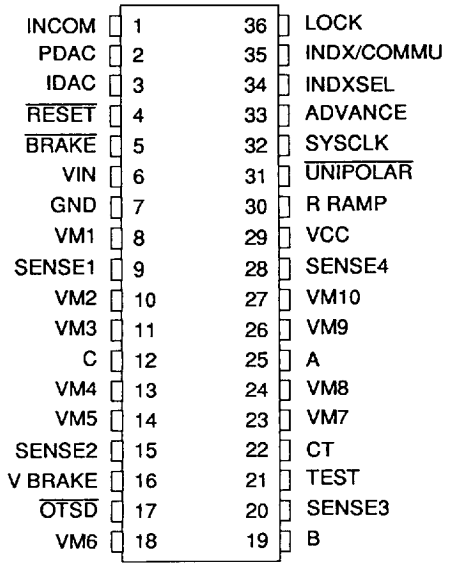
## PACKAGE PIN DESIGNATIONS

(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.




**36-Pin SOM**

## ORDERING INFORMATION

| PART DESCRIPTION | ORDER NO. | PKG. MARK |
|---|---|---|
| SSI 32M7010, Hall-Sensorless Motor Speed Control | | |
| 36-Pin SOM | 32M7010-CM | 32M7010 |

**Preliminary Data:** Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed Small quantities are available, and Silicon Systems should be consulted for current information.



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