



TSWC01622 SONET/SDH/PDH/ATM Clock Synthesizer and Protection Switch

Features

- Fully-integrated clock synthesis
- Clock or sync protection switching
- Fast, autonomous switching with software-override capability
- Supports a wide choice of SONET/SDH/ATM output clock frequencies:

| | | |
|------------|------------|------------|
| 622.08 MHz | 155.52 MHz | 77.76 MHz |
| 51.84 MHz | 44.736 MHz | 38.88 MHz |
| 34.368 MHz | 32.768 MHz | 24.704 MHz |
| 19.44 MHz | 16.384 MHz | 8.192 MHz |
| 4.096 MHz | 2.43 MHz | 2.048 MHz |
| 1.544 MHz | | |
- Supports multiple input clock frequencies:

| | | |
|-----------|-----------|-----------|
| 51.84 MHz | 38.88 MHz | 19.44 MHz |
| 8.192 MHz | 6.48 MHz | 2.048 MHz |
| 1.544 MHz | 8 kHz | |
- Generates sync outputs at 8 kHz aligned to an 8 kHz input clock/sync
- Locks to backup reference clock if both working and protection reference clocks are lost
- Compatible with Lucent Technologies TTRN012G5 2.5 Gbits/s MUX/Synthesizer, TDAT042G5/TADM042G5 SONET/ATM/POS devices, TSOT0410G, and TMXF28155 Super Mapper
- Single 3.3 V supply
- Supports multiple output levels: CMOS, LVPECL, or LVDS

Applications

- SONET/SDH and PDH add/drop multiplexers
- SONET/SDH and PDH cross connects
- ATM and packet over SONET switches and routers
- SONET/SDH and PDH test equipment
- Remote access servers

Description

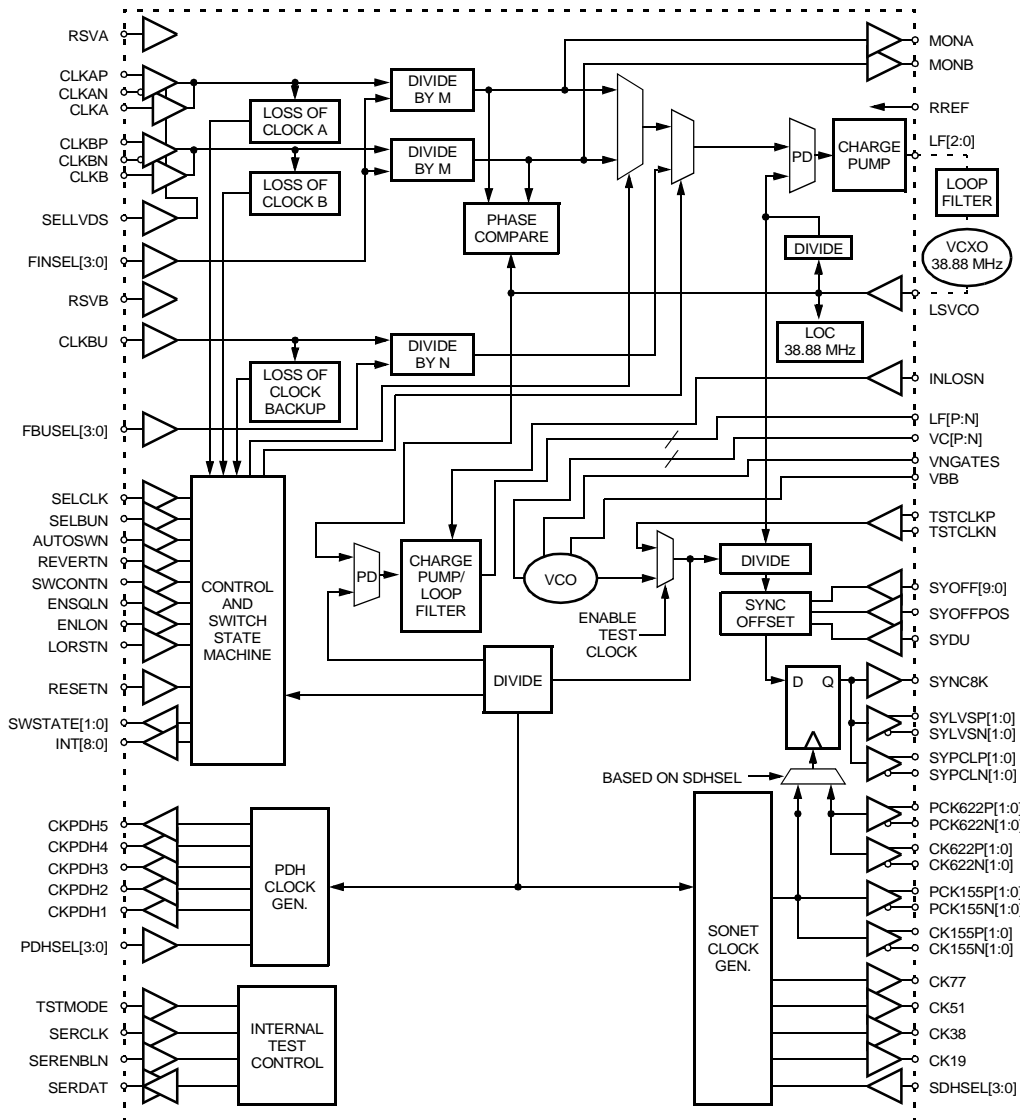
The Lucent Technologies Microelectronics Group TSWC01622 is designed for a wide variety of synchronous timing applications. It serves as a clock synthesizer and low-skew clock fanout device generating clocks at frequencies up to 622.08 MHz that are synchronized to the system reference clock. It also serves as an intelligent clock protection switch with fast, autonomous selection based on the presence of the two input clocks. Alternatively, clock switching can be controlled entirely through a software interface.

The TSWC01622 also delivers an output sync signal that is aligned to the input clock. If 8 kHz system sync signals are applied as the clock A and clock B inputs, the TSWC01622 will generate an output sync signal that is phase-aligned to the selected input sync. A programmable phase offset is provided to allow the user to offset the output sync relative to the input sync. The output sync can be used for global alignment of cells or frames in SONET/SDH/PDH cross connects or ATM switch applications. The device allows flexible choices of LVDS, LVPECL, or CMOS input and output levels.

The TSWC01622 is intended for clock distribution and protection switching on a line card, a switch card, or a shelf timing card. Along with the wide variety of input and output frequencies, a unique feature of the device is a guaranteed correct number of output clock cycles between output sync pulses before, during, and after a clock selection switching event. The number of clock cycles between sync pulses remains correct even during a switch between working and protection clock sources that have an arbitrary phase relationship between them. The TSWC01622 also solves the skew problem associated with timing distribution over cable or backplane traces of different lengths.

The block diagram is shown on the next page. Note that the diagram is representative of device functionality and conceptual signal flow. Internal implementation details may be different than shown.

Description (continued)



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Figure 1. Functional Block Diagram of TSWC01622

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