VTC Incorporated

VM118/VM118R

6-CHANNEL, CENTER-TAPPED THIN-FILM HEAD, READ/WRITE PREAMPLIFIER

April, 1990

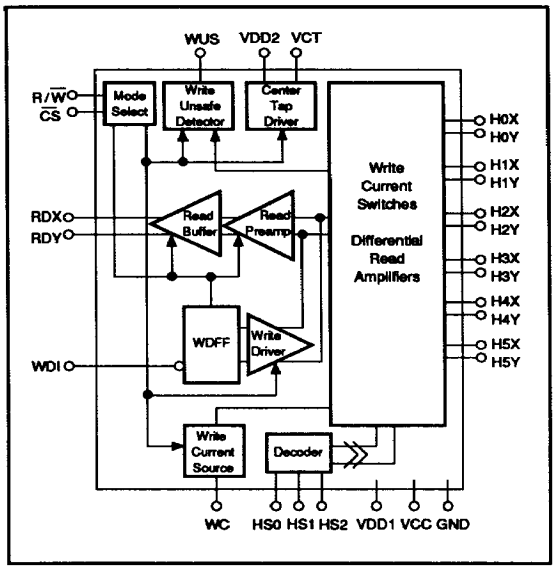
FEATURES

- Operates on +5V and +12V Power Supplies
- Programmable Write-Current Source
- TTL-Compatible Control Lines
- Write-Unsafe Detection Circuitry
- Low Input Noise
- For Use With Center-Tapped Thin-Film Heads
- Power-Up/Power-Down Write Protection
- Optional Internal Head Damping Resistors
- Available in 2, 4 and 6 Channels

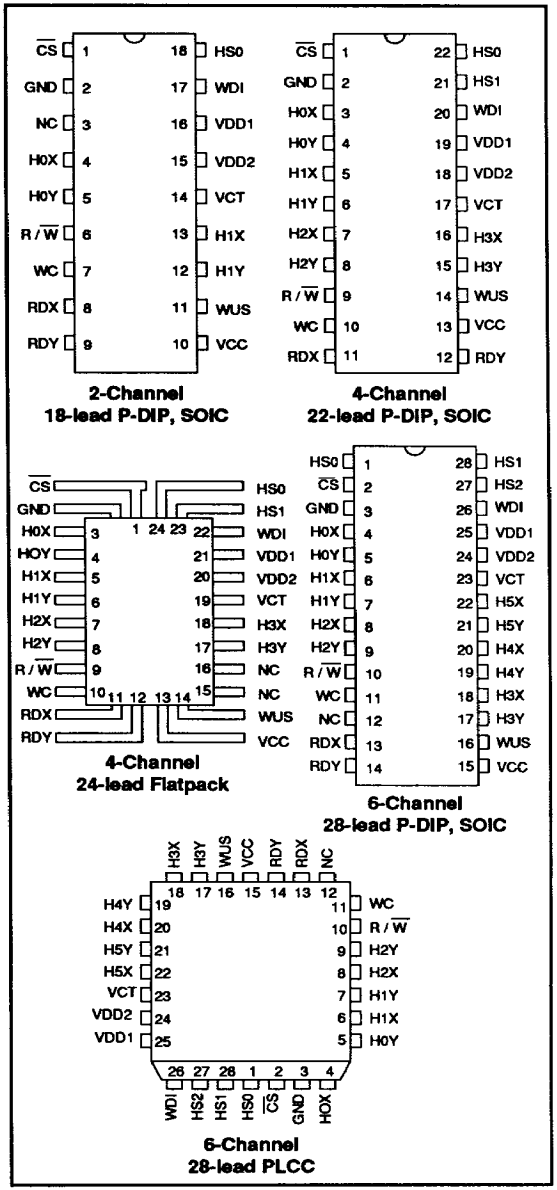
DESCRIPTION

The VM118/VM118R is a bipolar, monolithic read/write preamp circuit designed for use with center-tapped thin-film recording heads. The circuit provides a low-noise read data path for signals from the disk in the read mode and provides write-current control for data written on the disk in the write mode.

BLOCK DIAGRAM



CONNECTION DIAGRAMS



ABSOLUTE MAXIMUM RATINGS

Power Supply Voltages:
- V_{DD1} ..... -0.3 to 14V
- V_{DD2} ..... -0.3V to 14V
- V_{CC} ..... -0.3V to 6V

Pin Voltages:
- Head Select (HS) ..... -0.3V to V_{CC} + 0.3V
- Write Unsafe (WUS) ..... -0.3V to V_{CC} + 0.3V
- Write Data Input (WDI) ..... -0.3V to V_{CC} + 0.3V
- Read/Write Select (R/W) ..... -0.3V to V_{CC} + 0.3V

Output Current:
- Write Current (I_W) 60mA
- Read Data (RDX, RDY) 10mA
- Center Tap Current (I_{CT}) 60mA
- Write Unsafe (WUS) 12mA

Storage Temperature Range ..... -65 to 150°C
Lead Temperature (Soldering 60 Seconds) ..... 300°C
Junction Temperature ..... 150°C
Thermal Characteristics, Θ_{JA}:
- 18-lead P-DIP ..... 140°C/W
- 18-lead SOIC ..... 140°C/W
- 22-lead P-DIP ..... 65°C/W
- 22-lead SOIC ..... 80°C/W
- 24-lead Flatpack ..... 110°C/W
- 28-lead P-DIP ..... 55°C/W
- 28-lead SOIC ..... 70°C/W
- 28-lead PLCC ..... 65°C/W

RECOMMENDED OPERATING CONDITIONS

DC Power Supply Voltage:
- V_{DD1} ..... 12V ± 10%
- V_{DD2} ..... 7.0V to VDD1
- V_{CC} ..... 5V ± 10%

Head Inductance (L_H) ..... 1.2µH Typ.
Damping Resistance (R_D) (*Note 1*) 750Ω
R_{CT} Resistor at I_W = 50mA (*Note 2*) ..... 68Ω ± 5%
RDX,RDY Output Current (Read Mode) ..... 0 to 100µA
Write Current ..... 10 to 50mA
Operating Temperature Range ..... 0 to 70°C
Junction Temperature ..... 25° to +125°

Note 1: VM118R has head damping resistors placed on the chip; the standard value is 750Ω ± 20%.

Note 2: Resistor (R_{CT}) used to limit power dissipation. $R_{CT}(\Omega) \leq 3.4/I_W$ (A)

CIRCUIT OPERATION

The VM118/VM118R operates as a write-current switch in the write mode and as a low-noise differential amplifier in the read mode. Channel selection is controlled by HS0, HS1 and HS2 lines, and mode select is controlled by the CS and R/W select lines. Both CS and R/W have internal pull-up resistors to prevent accidental write conditions. Unsafe write conditions are indicated by the WUS line.

Write Mode

In the write mode, the VM118/VM118R operates as a write-current switch. Write current is supplied by an internal current source. The magnitude of the write current is determined by an external resistor connected between WC and ground. The head current is switched between the X and Y side of a selected head by falling transitions on WDI (write data input). When switching to the write mode from the read mode, the write data flip-flop is initialized to pass head current through the X side of the head.

The write unsafe (WUS), open collector output, will give a high level for any of the following unsafe conditions:
- Open Head
- No Write Current
- Read Mode
- Idle Mode
- Write Data Frequency Too Low
- Head Center-Tapped Open

After the fault condition is corrected, it takes two negative transitions on WDI to clear the WUS line.

Read Mode

In the read mode, the circuit operates as a low-noise differential amplifier. The write current source is turned off and the write data flip-flop is set. The selected head provides a differential input. The RDX and RDY pins provide differential emitter follower outputs which are in phase with the X and Y inputs.

Write current is deactivated for both the read and the idle mode so that external gating is not required.

Head Select

One of the six or eight heads may be selected in both the read and write modes. The selected head is determined by the voltage level of the head select inputs as shown below:

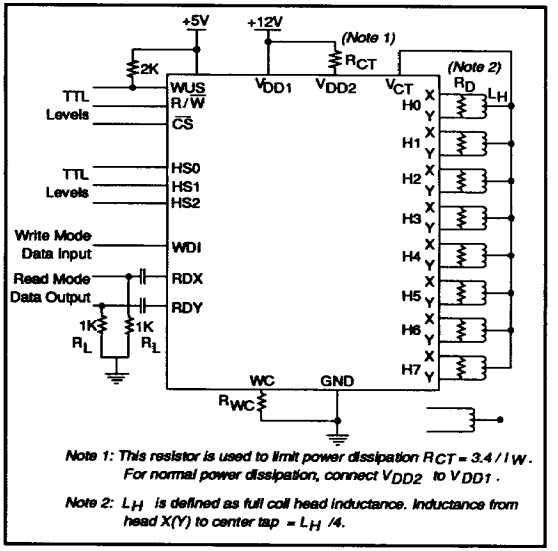
HS0	*HS1*	*HS2*	*HEAD*
L	L	L	0
H	L	L	1
L	H	L	2
H	H	L	3
L	L	H	4
H	L	H	5
X	H	H	None

Mode Select

This circuit has three modes of operation: read, write and idle. The state of the chip select ($\overline{CS}$) and the Read/Write select ($R/\overline{W}$) inputs determine the mode of operation as shown below:

$\overline{CS}$	$R/\overline{W}$	MODE
L	L	Write
L	H	Read
H	X	Idle

TYPICAL APPLICATION



Note 1: This resistor is used to limit power dissipation $R_{CT} = 3.4 / I_W$. For normal power dissipation, connect V_{DD2} to V_{DD1}.

Note 2: L_H is defined as full coil head inductance. Inductance from head X(Y) to center tap = L_H /4.

DC CHARACTERISTICS Unless otherwise specified, $V_{DD1} = V_{DD2} = 12V \pm 10\%$, $V_{CC} = 5V \pm 10\%$, $T_A = 25°C$.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Positive Supply Current	I_{DD}	Read Mode			40	mA
		Write Mode			26 + I_W	
		Idle Mode			25	
	I_{CC}	Idle/Read Mode			15	mA
		Write Mode			18	
Power Supply Dissipation	P_D	Read Mode		325	610	mW
		Idle Mode		200	412	
		Write Mode I_W = 50mA, R_{CT} = 75Ω		675	850	
		Write Mode I_W = 50mA, R_{CT} = 0Ω		850	1100	
DIGITAL TTL INPUTS: $\overline{CS}$, $R/\overline{W}$, HS, WD1						
Input High Voltage	VIH		2		V_{CC} + 0.3	V
Input Low Voltage	VIL		-0.3		0.8	V
Input High Current	IIH	V_{IH} = 2.0V V_{CC} = 5.5V	-400		100	µA
Input Low Current	IIL	V_{IL} = 0.4V V_{CC} = 5.5V	-0.4			mA
WUS OUTPUT						
Low Voltage	V_{OL}	I_{OL} = 8mA (Safe)			0.5	V
High Current	I_{OH}	V_{OH} = 5V (Unsafe)			100	µA
HEAD CENTER TAP VOLTAGES						
Read Mode	V_{CT}	Read Mode		4.2		V
Write Mode	V_{CT}	Write Mode		6.6		V

READ CHARACTERISTICS Unless otherwise specified, $V_{DD1} = V_{DD2} = 12V \pm 10\%$, $V_{CC} = 5V \pm 10\%$, $T_A = 25°C$.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Differential Voltage Gain	A_V	V_{IN} = 1mVrms, f = 500KHz R_L (RDX,RDY) = 1KΩ	80		120	V/V
Dynamic Range	DR	DC input Voltage where AC Gain Falls 10%, $V_{IN} = V_{DC} + 0.5mVp\text{-}p$ f = 500KHz	-2		2	mV
Bandwidth (-3dB)	BW	V_{IN} = 1mVrms, $Z_S < 5Ω$	30			MHz
Input Noise Voltage	e_{in}	$L_H = 0$, $R_H = 0$, BW = 15MHz		0.8	1.1	$nV/\sqrt{Hz}$
Differential Input Capacitance	C_{IN}	f = 5MHz			35	pF
Differential Input Resistance	R_{IN}	VM118	1.5			KΩ
		VM118R		750		Ω
Input Current	I_{IN}				45	μA
Common Mode Rejection Ratio	CMRR	$V_{CM} = V_{CT}$ + 100mVp-p, f = 5MHz	50			dB
Power Supply Rejection Ratio	PSRR	V_{DD} or V_{CC} = 100mVp-p, f = 5MHz	45			dB
Channel Separation	CS	V_{IN} = 100mVp-p, f = 5MHz Three Channel Driven, Selected Channel Measured	45			dB
Output Offset Voltage	V_{OS}		-400		400	mV
Common Mode Output Voltage	V_{OCM}		5		7	V
Head Center Tap Voltage	V_{CT}			4.2		V
Single-Ended Output Resistance	R_{SEO}				30	Ω

WRITE CHARACTERISTICS Unless otherwise specified, $V_{DD1} = V_{DD2} = 12V \pm 10\%$, $V_{CC} = 5V \pm 10\%$, $T_A = 25°C$, $I_W = 45mA$, $L_H = 0.72μH$, $R_H = 20Ω$, $R_D = 750Ω$, $f_{DATA} = 5MHz$. Note: The peak differential head voltage must be limited to 6V maximum i.e. at $I_W = 50mA$, $L_{MAX} = 1.2μH$. L_{MAX} varies inversely with I_{MAX}.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Write-Current Range	I_W	(see table and note on next page)	10		50	mA
Differential Head Voltage	V_{DH}			3.5		Vpk
Unselected Head Current	I_{UH}				2	mA p-p
Current Gain	A_I			20		mA/mA
Head-Center Tap Voltage	V_{CT}			6.5		V
Head-Current Propagation Delay	t_{PD}	$L_H = 0μH$, $R_H = 0Ω$, 50% WDI to 50% I_W			30	ns
Rise/Fall Time	t_r, t_f	$L_H = 0μH$, $R_H = 0Ω$, 10% to 90%		5	20	ns
Symmetry	S	$(t_r - t_f)/2$		0.3	2	ns
Write Current Tolerance	ΔI_W	$R_{WC} = 3111Ω$	42.75	45	47.25	mA
Differential Output Resistance	R_{OUT}	VM118	10			KΩ
		VM118R			750	Ω
Differential Output Capacitance	C_{OUT}	f = 5MHz			15	pF

EXTERNAL RESISTOR vs WRITE CURRENT

I_W into the selected Head terminal X or Y with VCT shorted only to the respective X or Y terminal.	
External Resistor R_{WC} (KΩ)	Write Current I_W (mA)
14.810	10
7.205	20
4.753	30
3.517	40
3.111	45
2.786	50

Note: The effective current I_{FLUX} generated in the magnetic head is related to I_W by the following expression:

$$I_{FLUX} = I_W \left(\frac{R_D}{R_H + R_D} \right)$$

Where R_H equals the full coil resistance of a center tapped ferrite head and R_D is the damping resistor connected internally or externally between the X and Y terminals.

SWITCHING CHARACTERISTICS Unless otherwise specified, $V_{DD1} = V_{DD2} = 12V \pm 10\%$, $V_{CC} = 5V \pm 10\%$, $T_A = 25°C$, $I_W = 45mA$, $L_H = 0.72\mu H$, $R_H = 20\Omega$, $R_D = 750\Omega$, $f_{DATA} = 5MHz$.

PARAMETER	*SYM*	*CONDITIONS*	*MIN*	*TYP*	*MAX*	*UNITS*
Read-to-Write Switching Delay	t_{RW}	50% of R/$\overline{W}$ to 90% of Write Output Envelope			1	µs
Write-to-Read Switching Delay	t_{WR}	50% of R/$\overline{W}$ to 90% of 100mVp-p RDX, RDY Envelope			1	µs
Idle-to-Write Switching Delay	t_{IW}	50% of $\overline{CS}$ to 90% of Write Output Envelope			1	µs
Idle-to-Read Switching Delay	t_{IR}	50% of $\overline{CS}$ to 90% of 100mVp-p RDX, RDY Envelope			1	µs
Write-to-Idle Switching Delay	t_{WI}	50% of $\overline{CS}$ to 10% of Write Output Envelope			1	µs
Read-to-Idle Switching Delay	t_{RI}	50% of $\overline{CS}$ to 10% of RDX, RDY Envelope			1	µs
Head Select Switching Delay	t_{HS}	50% of HS Transition to 90% of 100mVp-p RDX, RDY Envelope from Selected Head			1	µs
Write Unsafe Delay Safe-to-Unsafe	t_{D1}	Gate WDI. Measure from 50% of Last Data Pulse to 50% WUS	1.6		8	µs
Write Unsafe Delay Unsafe-to-Safe	t_{D2}	Gate WDI. Measure from 50% of Falling Edge of First Data Pulse to 50% WUS			1	µs