GigaBit Logic

10G101

T-45-07

Carry Lookahead Generator
675 ps Propagation Delay / 1.4 GHz
10G PicoLogic™ Family

FEATURES

- Typical input to carry output delay of 525 ps
- 150 ps output rise and fall times
- ECL and 10G PicoLogic™ compatible I/O
- Temperature and voltage compensated using VBB threshold reference input
- $\overline{P}$ input provided for compatibility with ECL adders
- On chip threshold reference voltage supply (VBBS)
- Available in 40 pin C-leaded or leadless chip carrier and die form
- Packages contain internal decoupling capacitors for optimum high frequency performance

APPLICATIONS

- Fast carry expander for 10G100 Adder and 10G181 ALU
- Replacement of ECL carry look ahead generators for higher speed performance

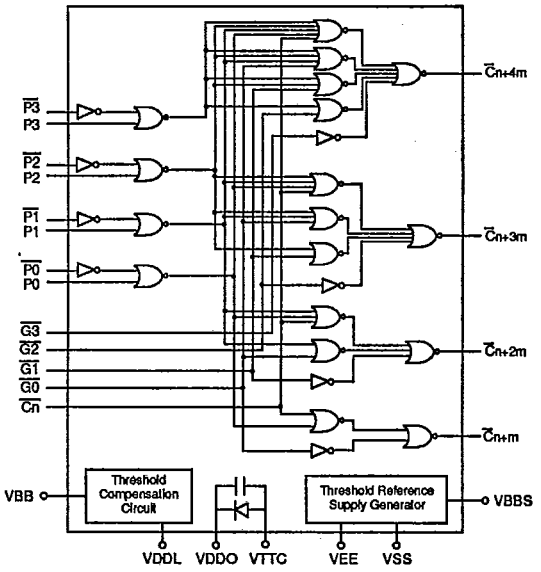
FUNCTIONAL DESCRIPTION

The 10G101 is an ultra-fast carry look ahead generator capable of generating carry outputs in 525 ps (typical delay), four times faster that equivalent ECL carry look ahead generators. The time reduction is even greater for word sizes longer than 16 bits. At room temperature, each additional 10G101 adds only 425 ps to the input to carry output delay. Both polarities of the carry propagate inputs are provided. The P input is used for higher speed with GigaBit's 10G100 adder. The $\overline{P}$ input is included for direct interface with ECL adders. Speed can be improved by over 30% by replacing 100K ECL carry lookahead generators with the 10G101 in existing ECL adder designs. The 10G101 can process input signals from DC to 1.4 GHz.

For compatibility with other high speed logic families, the 10G101 features the PicoLogic™ family standard VBB input. This input allows the 10G101's threshold voltage to be controlled by the driving logic family. Therefore, mismatches in threshold level due to temperature and power supply variations can be compensated, providing high system noise immunity. An on-chip threshold voltage output (VBBS) is also provided.

The 10G101 is a member of the 10G PicoLogic™ family of GaAs integrated circuits and is fabricated using GigaBit Logic's high volume GaAs MESFET process technology.

LOGIC DIAGRAM



10G101 ORDERING INFORMATION

PACKAGE TYPE	SPEED (Min 0° to 85° C)
	1.4 GHz
40 pin C-Leaded CC	10G101-2C
40 pin Leadless CC	10G101-2L
Die	10G101-2X

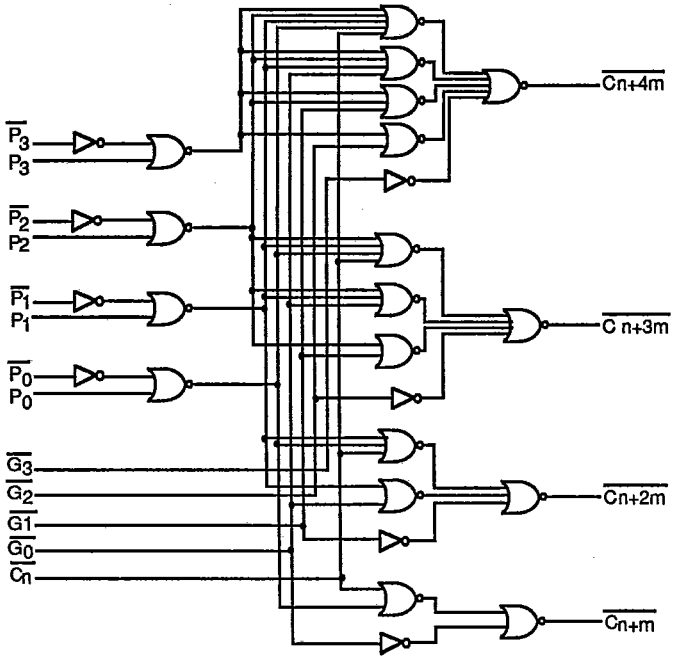
GigaBit Logic

10G101

T-45-07

1

10G101 OPERATION



m: number of bits per Adder or ALU

PIN DESCRIPTIONS

$\overline{G0}$...$\overline{G3}$	Active low carry generate inputs
P0...P3	Active high carry propagate inputs Unused P should be tied up to VTT.
$\overline{P0}$...$\overline{P3}$	Active low carry propagate inputs Unused $\overline{P}$ should be tied up to VDD.
$\overline{Cn}$	Active low carry input
$\overline{Cn+m}$,...$\overline{Cn+4m}$	Active low carry outputs; m is the number of bits per Adder or ALU. For example for the Picologic 10G100, m is equal to 4.
VDDO	Output driver ground pin (0V)
VDDL	Internal logic ground connection (0V)
VSS	-3.4 V power supply
VEE	-5.2 V power supply
VTTC	The AC return pin for the package internal VDDO decoupling capacitor. VTTC is not brought onto the 10G101 circuit, and is typically tied to VTT (nominally -2.0V).
VDCH	Output driver high level clamp voltage. When not in used, VDCH should be connected to VDDO. When driving ECL, VDCH may be used to limit VOH. Consult Application Note 4 for detail.
VBB	Reference input to the 10G101's input threshold tracking circuit. Connect to the VBB supplied from ECL when driving the 10G101 from ECL. Must be strapped to the VBBS pin when the 10G101 is driven from PicoLogic. This pin may not be left unconnected.
VBBS	PicoLogic threshold reference output voltage. Connect to VBB when driving from PicoLogic.

GigaBit Logic

10G101

T-45-07

10G101 Truth Table and Operations

• $\overline{Cn+4m}$ Output

$$\overline{Cn+4m} = \overline{G3 + P3 \cdot G2 + P3 \cdot P2 \cdot G1 + P3 \cdot P2 \cdot P1 \cdot G0 + P3 \cdot P2 \cdot P1 \cdot P0 \cdot C0}$$

Inputs								Output	Operation
$\overline{Cn}$	$\overline{G0}$	$\overline{P0}$	$\overline{G1}$	$\overline{P1}$	$\overline{G2}$	$\overline{P2}$	$\overline{G3}$ $\overline{P3}$	$\overline{Cn+4m}$	
X	X	X	X	X	X	X	L X	L	Carry generated by the 4th adder.
X	X	X	X	X	L	X	X L	L	Carry generated by the 3rd adder and propagated by the 4th adder.
X	X	X	L	X	X	L	X L	L	Carry generated by the 2nd adder and propagated by the 3rd and 4th adder.
X	L	X	X	L	X	L	X L	L	Carry generated by the 1st adder and propagated by the 2nd, the 3rd and the 4th adder.
L	X	L	X	L	X	L	X L	L	Carry supplied to the 1st adder and propagated by the 1st, the 2nd, the 3rd and the 4th adder.
All other combinations								H	No input carry, no generated carry or no propagated carry.

• $\overline{Cn+3m}$ Output

$$\overline{Cn+3m} = \overline{G2 + P2 \cdot G1 + P2 \cdot P1 \cdot G0 + P2 \cdot P1 \cdot P0 \cdot C0}$$

Inputs							Output
$\overline{Cn}$	$\overline{G0}$	$\overline{P0}$	$\overline{G1}$	$\overline{P1}$	$\overline{G2}$	$\overline{P2}$	$\overline{Cn+3m}$
X	X	X	X	X	L	X	L
X	X	X	L	X	X	L	L
X	L	X	X	L	X	L	L
L	X	L	X	L	X	L	L
All other combinations							H

• $\overline{Cn+2m}$ Output

$$\overline{Cn+2m} = \overline{G1 + P1 \cdot G0 + P1 \cdot P0 \cdot C0}$$

Inputs					Output
$\overline{Cn}$	$\overline{G0}$	$\overline{P0}$	$\overline{G1}$	$\overline{P1}$	$\overline{Cn+2m}$
X	X	X	L	X	L
X	L	X	X	L	L
L	X	L	X	L	L
All other combinations					H

• $\overline{Cn+m}$ Output

$$\overline{Cn+m} = \overline{G0 + P0 \cdot C0}$$

Inputs			Output
$\overline{Cn}$	$\overline{G0}$	$\overline{P0}$	$\overline{Cn+m}$
X	L	X	L
L	X	L	L
All other combinations			H

Notes :

- H: High voltage level
  L: Low voltage level
  X: don't care
  m: number of bits per adder or ALU
  n: input carry bit number
- $\overline{P}$ is used in the truth tables for compatibility with ECL adders. Truth tables for P (used with 10G100 Adders) can be derived by changing L to H in the P columns.
- Unused P inputs should be tied up to VTT. Unused $\overline{P}$ inputs should be tied up to VDD.

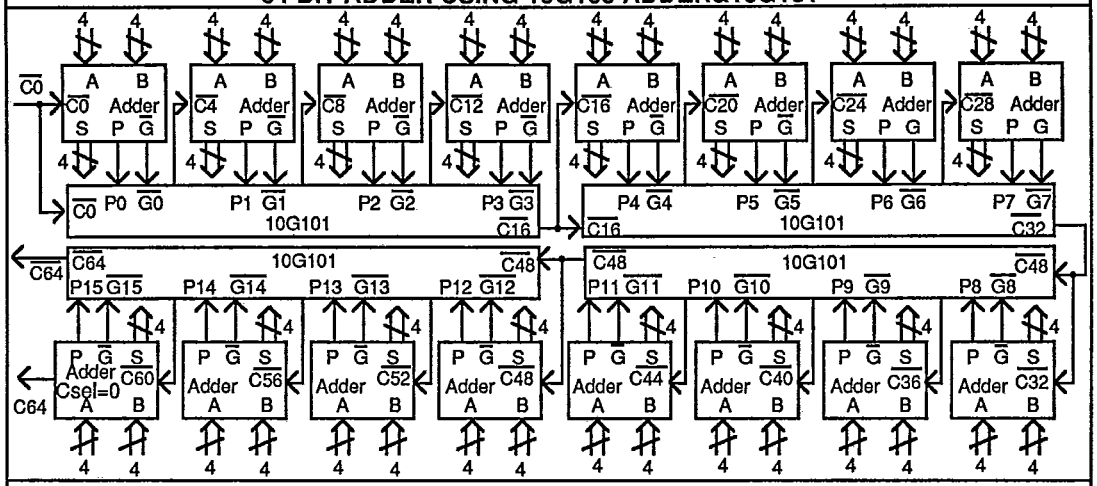
GigaBit Logic

10G101

T-45-07

1

64 BIT ADDER USING 10G100 ADDER&10G101



TYPICAL PROPAGATION DELAYS

	Operation	Typical Propagation Delay
a) •	Input signals ready : A, B, $\overline{C0}$ signals to 10G100/10G101	N/A
b) •	Input to Carry Propagate and Carry Generate outputs : A, B, $\overline{C0}$ to P, $\overline{G}$ (10G100)	700ps
c) •	Input to carry output : P, $\overline{G}$ to $\overline{C16}$ (10G101)	525ps
d) •	Carry inputs to carry outputs : $\overline{C16}$ to $\overline{C32}$, $\overline{C32}$ to $\overline{C48}$ and $\overline{C48}$ to $\overline{C64}$ (respectively 2nd, 3rd and 4th 10G101)	3 X 425 = 1275 ps
e) •	Carry input to sum output : $\overline{C48}$ to S (4 most significant 10G100 adders)	850ps
	Total Propagation Delay	3.35ns

64 BIT ADDER DESCRIPTION

a) The carry input $\overline{C0}$ is supplied to the first adder and carry lookahead generator. At the same time the A and B inputs are supplied to all adders.

b) All adders generate the Carry Propagate (P/$\overline{P}$) and the Carry Generate ($\overline{G}$) signals. P is the limiting factor since it takes 700ps to output P compared to 650ps to output $\overline{G}$.

c) The Carry Propagate (P) and Carry Generate ($\overline{G}$) signals are supplied to the 1st 10G101. It takes 525ps for the 10G101 to generate $\overline{C4}$, $\overline{C8}$, $\overline{C12}$ and $\overline{C16}$.

d) $\overline{C16}$ is supplied to the 2nd 10G101 and the 5th adder. Since all the P and G signals have been generated at stage (b) it takes 425ps for the 10G101 to output $\overline{C20}$, $\overline{C24}$, $\overline{C28}$ and $\overline{C32}$. The second group of 4 adders (Adders 5 to 8) then generates the sum outputs. The sum outputs propagation delay is always less than the remaining time to complete the 64 bit addition and, therefore, does not have to be accounted.

Step C is repeated for the third and fourth groups of adders respectively, adders 9 to 12 and adders 13 to 16.

e) After $\overline{C52}$, $\overline{C56}$, $\overline{C60}$, and $\overline{C64}$ have been generated, the sum output of the 4 most significant adders is calculated. The most significant adder should have $\overline{Csel}$ low to select the active high carry output (C64) for the M.S.B.

GigaBit Logic

10G101

T-45-07

DC CHARACTERISTICS

Tc = 0°C to 85°C, VSS = -3.5 V TO -3.3 V, VEE = -5.5 TO -5.1 V, VDDL = VDDO = Gnd., unless otherwise indicated

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
VBBS	Threshold Reference Voltage		-1.2		V
ISS	Power Supply Current		240	380	mA
IEE	Power Supply Current		18	32	mA
PD	Power Dissipation		910	1460	mW

NOTE:

The remaining DC Characteristics are specified in the 10G PicoLogic™ Family Electrical Characteristics Table at the beginning of this section. This table notes parameter deviations to Family Characteristics and provides specific supplementary characteristics only.

AC CHARACTERISTICS (Note 1)

10G101-2

VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

SYMBOL	PARAMETER	Tc = 0°C		Tc = +25°C			Tc=+85°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
1/T1	Input frequency	1.4		1.4	1.5		1.4		GHz	
Td1	Carry input ($\overline{Cn}$) or carry generate ($\overline{G}$) to carry outputs	325	575	325	425	575	325	575	ps	
Td2	Active high carry propagate (P) to carry outputs	350	675	350	525	675	350	675	ps	
Td3	Active low carry propagate ($\overline{P}$) to carry outputs	375	700	375	550	700	375	700	ps	
Tr,f	Output rise or fall time		200		150	200		225	ps	2

Notes: 1. Test conditions (unless otherwise indicated) :

VBB = -1.2V
VTT = -2.0V
VTTC = VTT
RLOAD = 50Ω to VTT
Input signal rise and fall time ≤ 150 ps

VIH = -0.7V
VIL = -1.7V
VOH ≥ -0.7V
VOL ≤ -1.7V

VDCH = VDDO

2. Rise and fall times are measured at the 20% and 80% points of the transition from VOL max to VOH min.

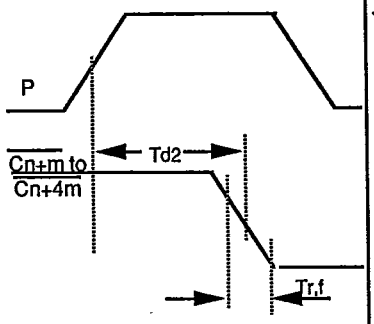
GigaBit Logic

10G101

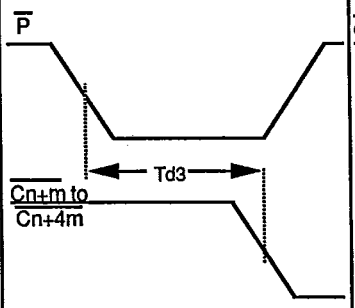
T-45-07

SWITCHING WAVEFORMS

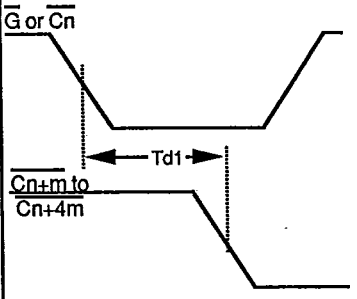
Active high carry propagate to carry outputs.



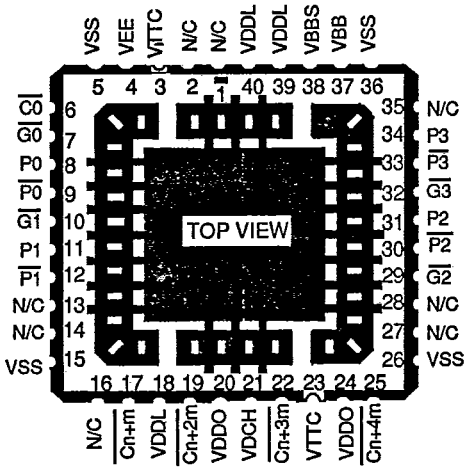
Active low carry propagate ($\overline{P}$) to carry outputs.



Active low carry generate ($\overline{G}$) or carry input ($\overline{Cn}$) to carry outputs.



Pin Functions - TYPE "L" and "C" Packages



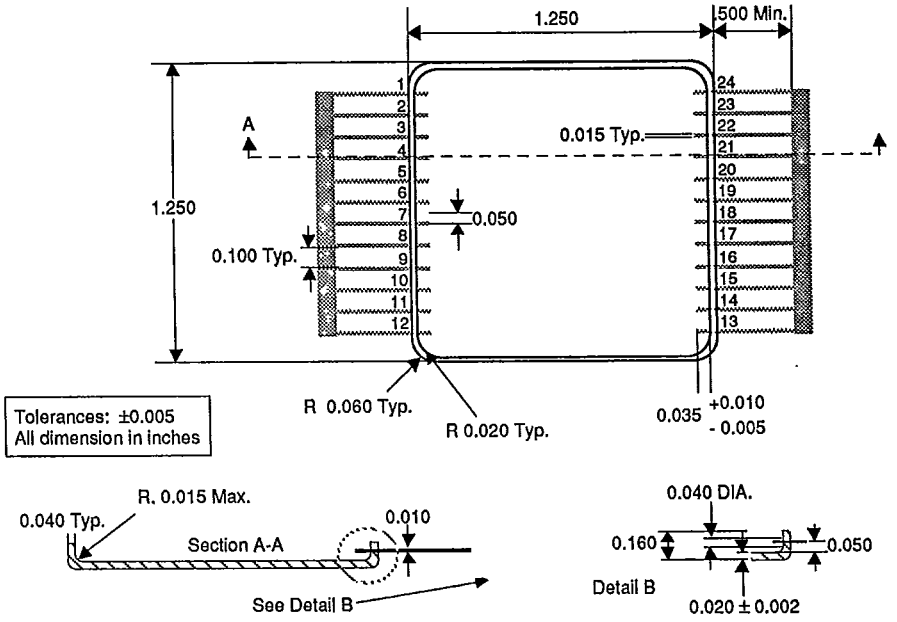
GigaBit Logic

24 PIN HYBRID 18 PIN PACKAGE

T-90-20

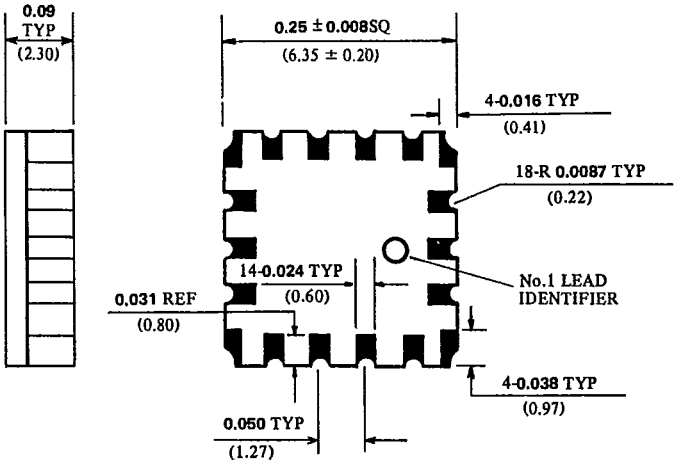
24 PIN HYBRID PACKAGE

Type H



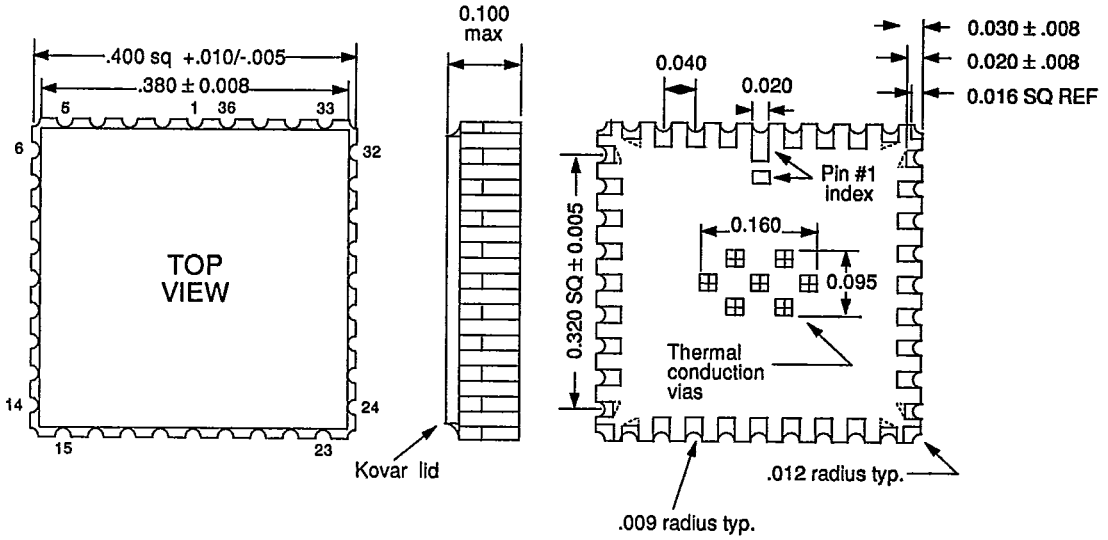
18 PIN LEADLESS CHIP CARRIER

TYPE L1



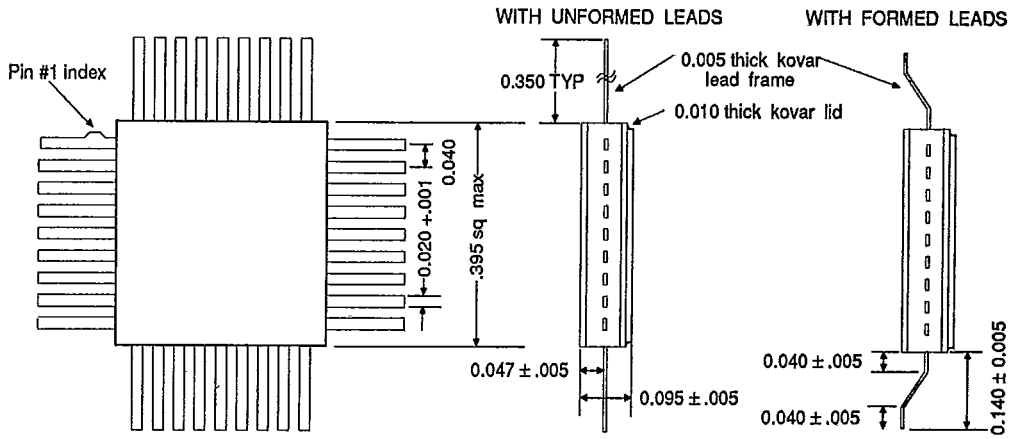
All dimensions shown in **inches** and (millimeters)

36 PIN LEADLESS CHIP CARRIER
TYPE L36



NOTES:
1) The package bottom thermal vias, top lid surface and 4 metallized corner castellations (when present) are all at Vss potential.
2) All dimensions in inches.
3) Pin #1 identifier may be an elongated pad or small, square gray marker.

36 I/O LEAD FLATPACK
TYPE F



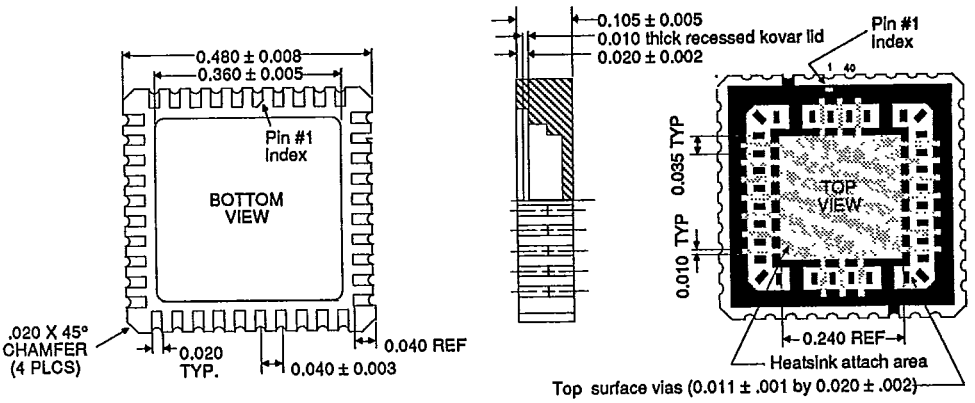
11

T-90-20

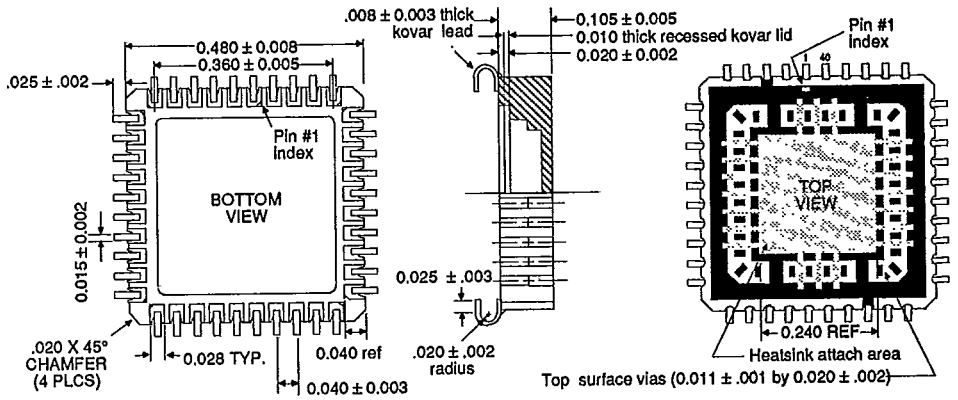
GigaBit Logic

40 PIN PACKAGES

40 PIN LEADLESS CHIP CARRIER
TYPE L



40 PIN LEADED CHIP CARRIER
TYPE C

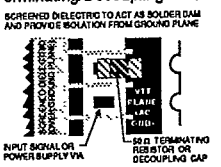


NOTES:

(1) Footprint is JEDEC standard outline.
(2) Top surface vias (for terminating resistors and decoupling capacitors) are not available on pins 3,4,17, 18, 23,24,37 and 38.
(3) Top surface metal (not including vias) and pins 3 and 23 are fixed at VTT potential.
(4) Recommended top surface chip resistors are0.040 long by 0.020 wide by 0.010 thick typ, 100 mw min. nominal power rating (Mini-Systems MSR-21 or equivalent.)
(5) Recommended top surface chip capacitors are 0.040 long by 0.030 wide by 0.020 thick typ, 25V VDCW, 1000 pf, min. (Johanson R09 case or equivalent).
(6) Recommended heatsinks are GBL P/Ns 90GHS-40-A and 90GHS-40-B.
(7) Thermally conductive, electrically non-conductive epoxy is recommended for heatsink attachment (Ablestick 789-4 or 561K, or Thermalloy Thermalbond™ or equivalent.)
(8) L40 and C40 packages are dimensionally identical except for contact finger width.

TOP SURFACE LEGEND:
Metalized Ceramic.....
Screened Dielectric.....
Bare Ceramic.....

Top Surface Terminating/Decoupling Detail

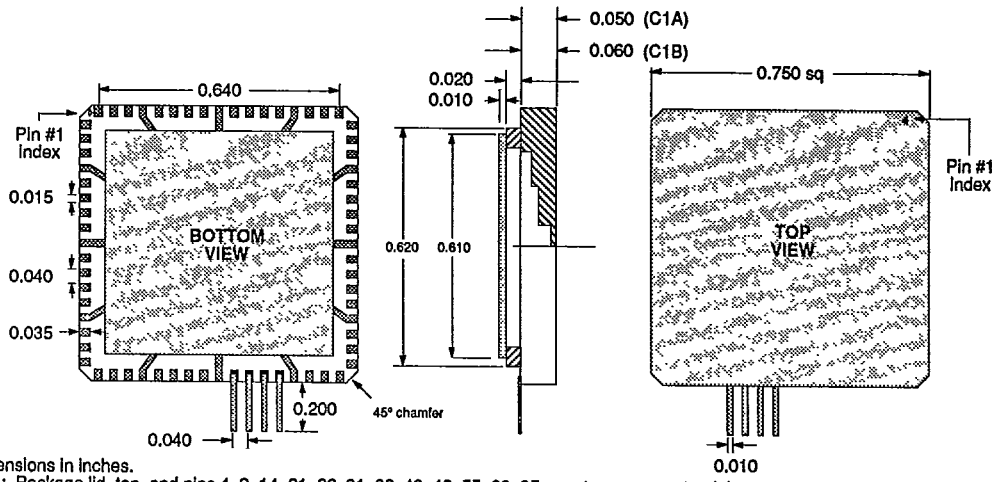


GigaBit Logic

68 & 132 PIN PACKAGES

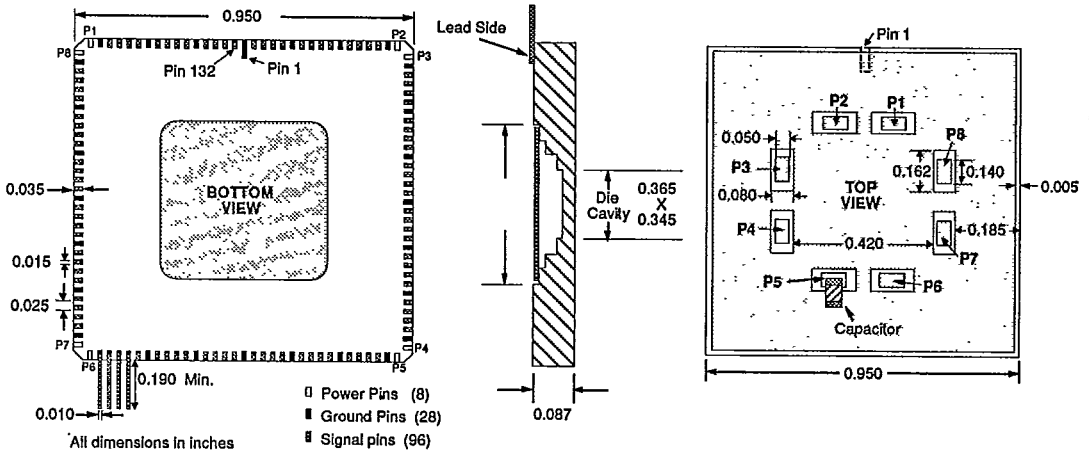
T-90-20

68 PIN LEADED CHIP CARRIER
TYPE C1



(1) All dimensions in inches.
(2) a. C1A: Package lid, top, and pins 4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65 are at common potential (system ground).
b. C1B: Package lid and pins 4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65 are at common potential (system ground).

132 PIN LEADED CHIP CARRIER
TYPE C3



11