8M x 32 SO DIMM Module

Features

- 72-Pin Small Outline Dual-In-Line Memory Module
- Performance:

		-60
t_{RAC}	$\overline{RAS}$ Access Time	60ns
t_{CAC}	$\overline{CAS}$ Access Time	15ns
t_{AA}	Access Time From Address	30ns
t_{RC}	Cycle Time	110ns
t_{HPC}	EDO Mode Cycle Time	25ns

- High Performance CMOS process
- Single 3.3V ± 0.3V Power Supply
- Low active current consumption
- All inputs & outputs are LVTTL(3.3V) compatible
- Extended Data Out (EDO) access cycle
- Refresh Modes: $\overline{RAS}$-Only, CBR, Hidden and Self Refresh
- 4096 refresh cycles distributed across 256ms
- 12/11 Addressing (Row/Column)
- Optimized for use in byte-write non-parity applications.
- Au contacts

Description

The IBM11S8325HP is a 32MB industry standard 72-pin 4-byte small outline dual in-line memory module (SO DIMM). The module is organized as a 8Mx32 high speed memory array that is intended for use in 16, 32 and 64 bit applications. It is manufactured with four 8Mx8 TSOP devices, each in a 500mil package.

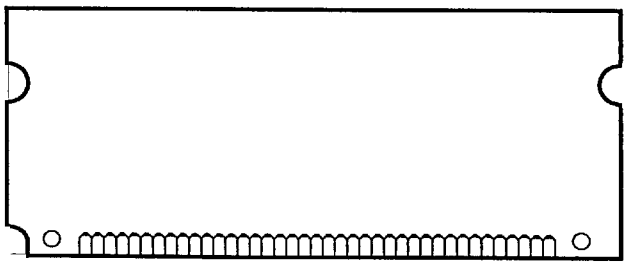
The use of EDO DRAMs allows for a reduction in Page Mode cycletime from 40ns (Fast Page) to 25ns.

The use of TSOP packages allows tight DIMM spacing (.3" on center).

This assembly is intended for use in space constrained and/or low power applications.

The IBM 72-Pin SO DIMMs provide a high performance, flexible 4-byte interface in a 2.35" long footprint.

Card Outline



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Pin Description

RAS0, RAS2	Row Address Strobe
CAS0 - CAS3	Column Address Strobe
WE	Read/write Input
A0 - A11	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
V_{CC}	Power (+3.3V)
V_{SS}	Ground
NC	No Connect
PD1 - PD7	Presence Detects

Pinout

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	V_{SS}	13	A1	25	DQ13	37	DQ18	49	DQ20	61	V_{CC}
2	DQ0	14	A2	26	DQ14	38	DQ19	50	DQ21	62	DQ32
3	DQ1	15	A3	27	DQ15	39	V_{SS}	51	DQ22	63	DQ33
4	DQ2	16	A4	28	A7	40	CAS0	52	DQ23	64	DQ34
5	DQ3	17	A5	29	A11	41	CAS2	53	DQ24	65	NC
6	DQ4	18	A6	30	V_{CC}	42	CAS3	54	DQ25	66	PD2
7	DQ5	19	A10	31	A8	43	CAS1	55	NC	67	PD3
8	DQ6	20	NC	32	A9	44	RAS0	56	DQ27	68	PD4
9	DQ7	21	DQ9	33	NC	45	NC	57	DQ28	69	PD5
10	V_{CC}	22	DQ10	34	RAS2	46	NC	58	DQ29	70	PD6
11	PD1	23	DQ11	35	DQ16	47	WE	59	DQ31	71	PD7
12	A0	24	DQ12	36	NC	48	NC	60	DQ30	72	V_{SS}

Ordering Information

Part Number	Organization	Speed	Dimensions	Power
IBM11S8325HP-60	8M x 32	60ns	2.35" x 1" x .1496"	3.3V

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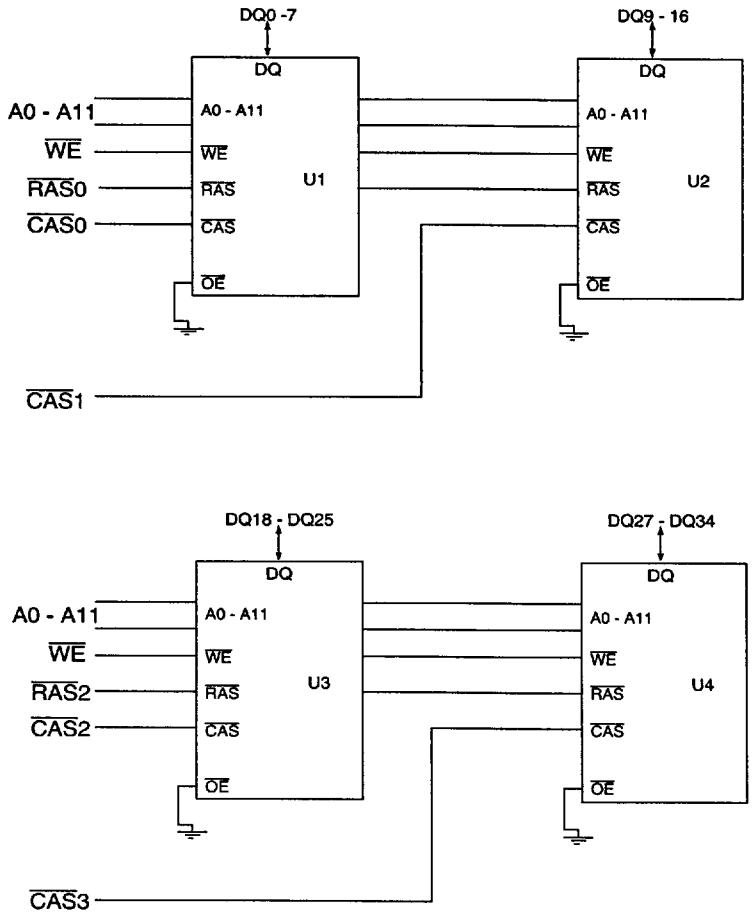
Block Diagram



Truth Table

Function		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	All DQ bits
Standby		H	H→X	X	X	X	High Impedance
Read		L	L	H	Row	Col	Valid Data Out
Early-Write		L	L	L	Row	Col	Valid Data In
EDO Mode - Read: 1st Cycle		L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles		L	H→L	H	N/A	Col	Valid Data Out
EDO Mode - Write: 1st Cycle		L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles		L	H→L	H→L	N/A	Col	Valid Data In
$\overline{RAS}$-Only Refresh		L	H	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh		H→L	L	H	X	N/A	High Impedance
Hidden Refresh	Read	L→H→L	L	H	Row	Col	Data Out
	Write	L→H→L	L	H	Row	Col	Data In
Self Refresh		H→L	L	H	X	X	High Impedance

Presence Detect

Pin	-70
PD1	V_{SS}
PD2	V_{SS}
PD3	NC
PD4	NC
PD5	NC
PD6	NC
PD7	V_{SS}

1. NC= OPEN, V_{SS} = GND

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
		3.3 Volt		
V_{CC}	Power Supply Voltage	-0.5 to + 4.6	V	1
V_{IN}	Input Voltage	-0.5 to min (V_{CC} + 0.5, 4.6)	V	1
V_{OUT}	Output Voltage	-0.5 to min (V_{CC} + 0.5, 4.6)	V	1
T_{OPR}	Operating Temperature	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +150	°C	1
P_D	Power Dissipation	1.9	W	1, 2
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Maximum power occurs when all banks are active.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	3.3 Volt				
		Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	3.0	3.3	3.6	V	1
V_{IH}	Input High Voltage	2.0	—	V_{CC} + 0.5	V	1, 2
V_{IL}	Input Low Voltage	-0.5	—	0.8	V	1, 2

1. All voltages referenced to V_{SS}.
2. V_{IH} may overshoot to V_{CC} + 2.0V for pulse widths of ≤ 4.0ns . V_{IL} may undershoot to -2.0V for pulse widths ≤ 4.0ns . Pulse widths measured at 50% points with amplitude measured peak to DC reference.

Capacitance (T_A = 0 to +70°C, V_{CC} = 3.3V ± 0.3V)

Symbol	Parameter	Max	Units
C_{I1}	Input Capacitance (A0-A11)	36	pF
C_{I2}	Input Capacitance ($\overline{RAS}$)	20	pF
C_{I3}	Input Capacitance ($\overline{CAS}$)	15	pF
C_{I4}	Input Capacitance ($\overline{WE}$)	40	pF
$C_{I/O}$	Output Capacitance (DQ0-DQ34)	12	pF

DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 3.3 0.3V)

Symbol	Parameter		3.3 Volt Min	3.3 Volt Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current $\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-60	—	520	mA	1, 2, 3
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥V_{IH})		—	8	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥V_{IH}; t_{RC} = t_{RC} min)	-60	—	440	mA	1, 3
I_{CC4}	EDO Mode Current Average Power Supply Current, EDO Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{HPC} = t_{HPC} min)	-60	—	320	mA	1, 2, 3
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	800	µA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60	—	480	mA	1, 3
I_{CC7}	Self Refresh Current Average Power Supply Current during Self Refresh CBR cycle with $\overline{RAS}$ ≥ t_{RASS} (min); $\overline{CAS}$ held low; $\overline{WE}$ = V_{CC} - 0.2V; Addresses and D_{IN} = V_{CC} - 0.2V or 0.2V.	-60	—	1600	µA	
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} + 0.3v)) All Other Pins Not Under Test = 0V	$\overline{RAS}$	-20	+20	µA	
		$\overline{CAS}$	-10	+10		
		WE, ADD	-40	+40		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-10	+10	µA	
V_{OH}	Output High Level(LVTTL) Output "H" Level Voltage (I_{OUT} = -2mA)		2.4	—	V	
V_{OH}	Output Low Level(LVTTL) Output "L" Level Voltage (I_{OUT} = +2mA)		—	0.4	V	
V_{OL}	Output High Level(LVCMOS) Output "H" Level Voltage (I_{OUT} = -2mA)		V_{CC}-0.2	—	V	4
V_{OL}	Output Low Level(LVCMOS) Output "L" Level Voltage (I_{OUT} = +2mA)		—	0.2	V	4

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
4. V_{OL} (LVCMOS) and V_{OH} (LVCMOS) levels are not intended for use as timing reference levels. LVCMOS levels are the quiescent state of a low impedance output driver, under the specified load condition.

AC Characteristics

(T_A = 0 to +70°C, V_{CC} = 3.3V 0.3V)

1. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using the internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
2. AC measurements assume t_T=2ns.
3. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. When both $\overline{CAS0}$ & $\overline{CAS1}$ or $\overline{CAS2}$ & $\overline{CAS3}$ go low at the same time, all 16 bits of data are read/written into the device. $\overline{CAS0}$ & $\overline{CAS1}$ or $\overline{CAS2}$ & $\overline{CAS3}$ (CAS's to the same DRAM) cannot be staggered within the same read/write cycle.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		Units	Notes
		Min	Max		
t_{RC}	Random Read or Write Cycle Time	104	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	100K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	10	100K	ns	
t_{ASR}	Row Address Setup Time	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	ns	
t_{ASC}	Column Address Setup Time	0	—	ns	
t_{CAH}	Column Address Hold Time	10	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	14	45	ns	1
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	12	30	ns	2
t_{RSH}	$\overline{RAS}$ Hold Time	10	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	50	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	—	ns	
t_T	Transition Time (Rise and Fall)	1	50	ns	

1. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
2. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.

Write Cycle

Symbol	Parameter	-60		Units	Notes
		Min	Max		
t_{WCS}	Write Command Set Up Time	0	—	ns	1
t_{WCH}	Write Command Hold Time	10	—	ns	
t_{WP}	Write Command Pulse Width	10	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	10	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	10	—	ns	
t_{DS}	D_{IN} Setup Time	0	—	ns	
t_{DH}	D_{IN} Hold Time	10	—	ns	

1. t_{WCS}, is not a restrictive operating parameters. It is included in the data sheet as an electrical characteristic only. If $t_{WCS} \geq t_{WCS}$(min.), the cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle. If the above condition is not satisfied, the condition of the data out (at access time) is indeterminate.

Read Cycle

Symbol	Parameter	-60		Units	Notes
		Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	ns	1, 2, 3, 4
t_{CAC}	Access Time from $\overline{CAS}$	—	15	ns	1, 3, 4
t_{AA}	Access Time from Address	—	30	ns	1, 3, 4
t_{RCS}	Read Command Setup Time	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	ns	5
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	—	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	ns	
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	ns	3
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	15	—	ns	5
t_{OFF}	Output Buffer Turn-off Delay	0	15	ns	6

1. Operation within the t_{RCD}(max.) limit ensures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
2. Operation within the t_{RAD}(max.) limit ensures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.
3. Measured with the specified current load and 100pF.
4. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
5. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Extended Data Out Cycle

Symbol	Parameter	-60		Units	Notes
		Min.	Max.		
t_{HCAS}	$\overline{CAS}$ Pulse Width (Hyper Page Mode)	10	10K	ns	
t_{HPC}	Hyper Page Mode Cycle Time (Read/Write)	25	—	ns	
t_{HPRWC}	Hyper Page Mode Read Modify Write Cycle Time	66	—	ns	
t_{DOH}	Data-out Hold Time from $\overline{CAS}$	5	—	ns	
t_{WHZ}	Output buffer Turn-Off Delay from $\overline{WE}$	0	10	ns	
t_{WPZ}	$\overline{WE}$ Pulse Width to Output Disable at $\overline{CAS}$ High	10	—	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	35	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	35	ns	1, 2
t_{RASP}	Hyper Page Mode $\overline{RAS}$ Pulse Width	60	200K		
t_{OEP}	$\overline{OE}$ High Pulse Width	10	—		
t_{OEHC}	$\overline{OE}$ High Hold Time from $\overline{CAS}$ High	10	—		

1. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
2. Measured with the specified current load and 100pF at V_{OL} = 0.8V and V_{OH} = 2.0V.

Refresh Cycle

Symbol	Parameter	-60		Units	Notes
		Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	5	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	0	—	ns	
t_{REF}	Refresh Period	—	256	ms	1

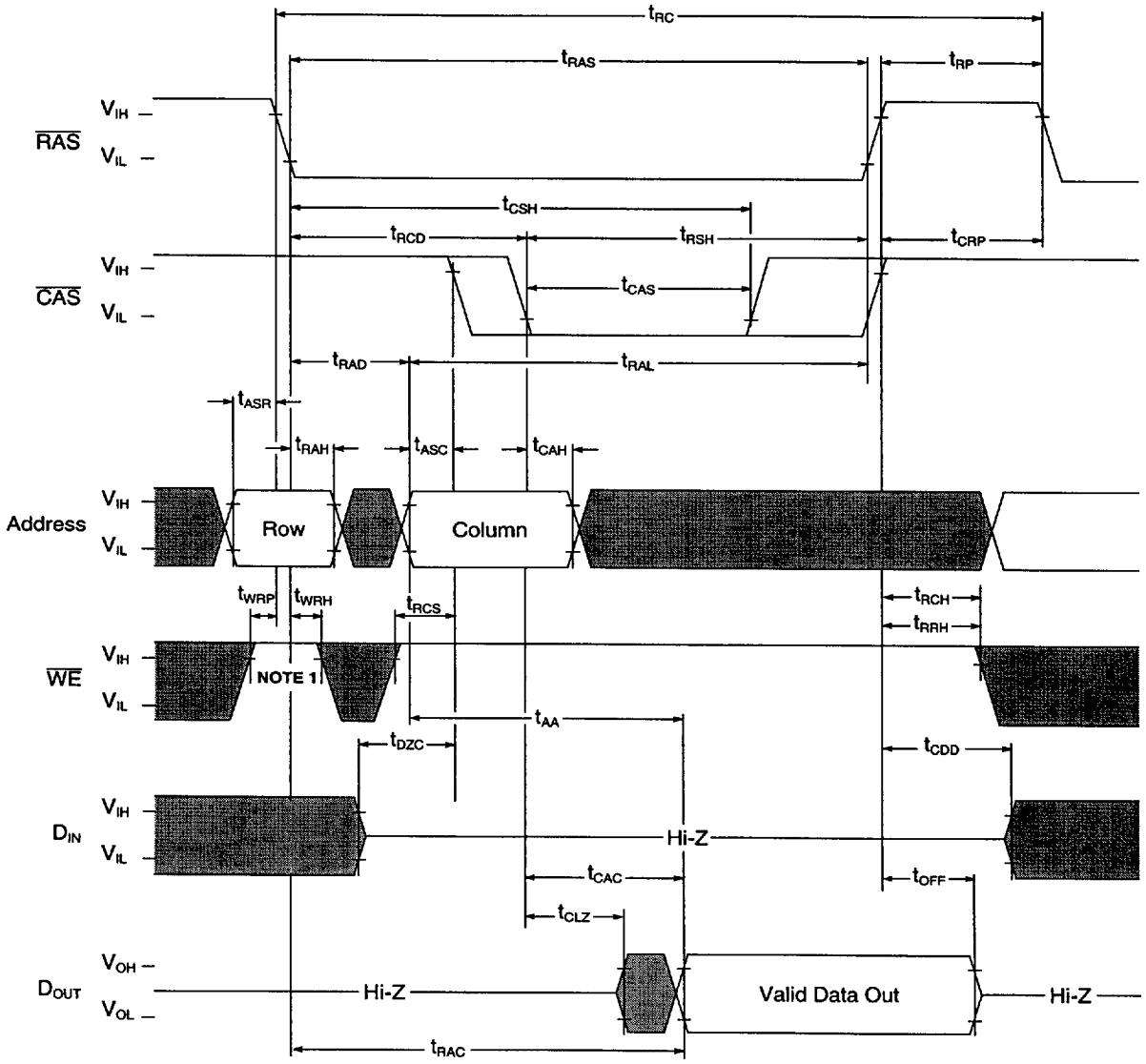
1. 4096 refreshes are required every 256ms.

Self Refresh Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min.	Max.	Min.	Max.		
t_{RASS}	$\overline{RAS}$ Pulse Width During Self Refresh Cycle	100	—	100	—	µs	1
t_{RPS}	$\overline{RAS}$ Precharge Time During Self Refresh Cycle	104	—	124	—	ns	1
t_{CHS}	$\overline{CAS}$ Hold Time During Self Refresh Cycle	-50	—	-50	—	ns	1

1. When using Self Refresh mode, the following refresh operations must be performed to ensure proper DRAM operation: If row addresses are being refreshed in a EVENLY DISTRIBUTED manner over the refresh interval using CBR refresh cycles, then only one CBR cycle must be performed immediately after exit from Self Refresh. If row addresses are being refreshed in any other manner (ROR - Distributed/Burst; or CBR-Burst) over the refresh interval, then a full set of row refreshes must be performed immediately before entry to and immediately after exit from Self Refresh.

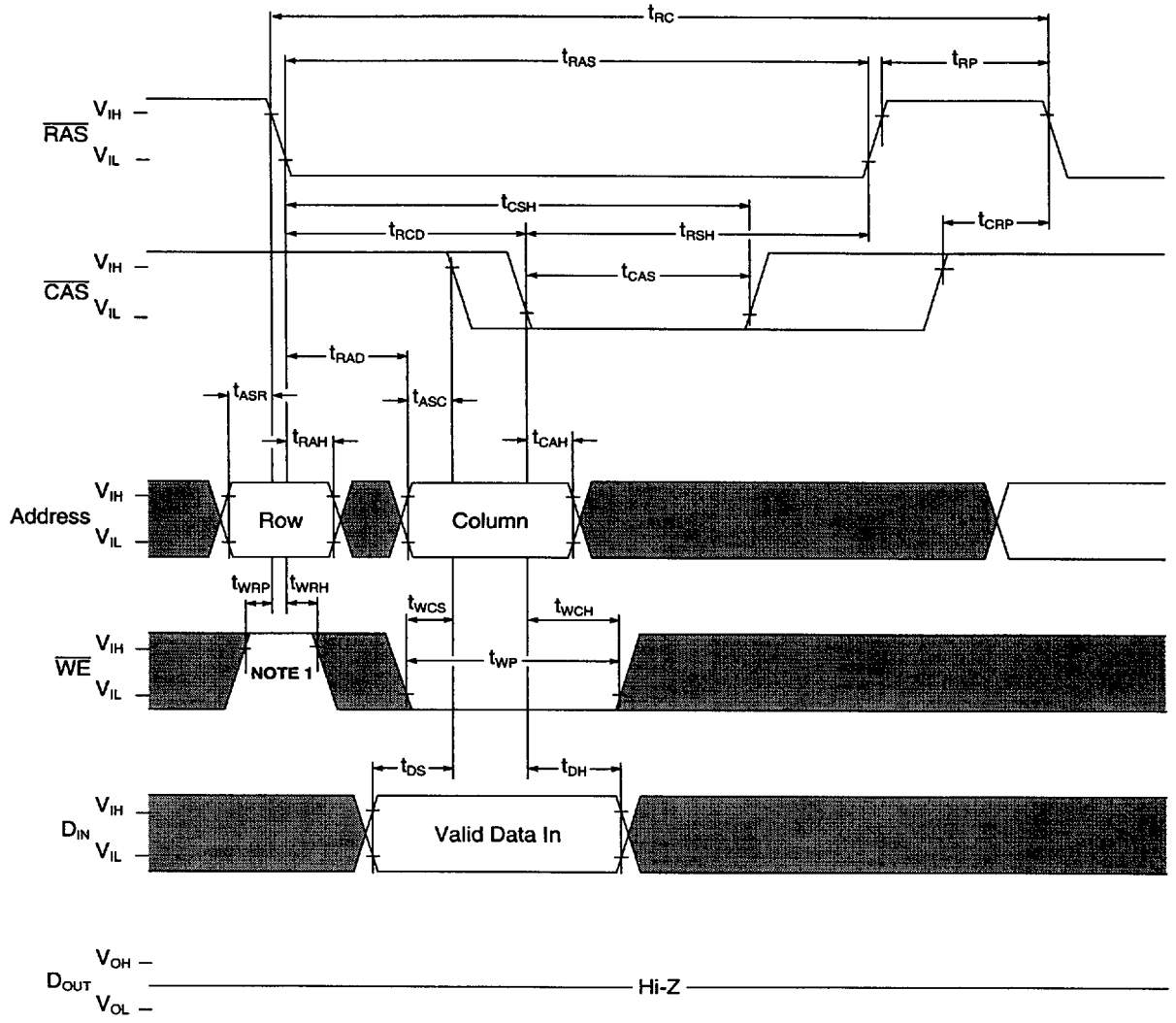
Read Cycle



: "H": or "L"

NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future HPM DRAMs.

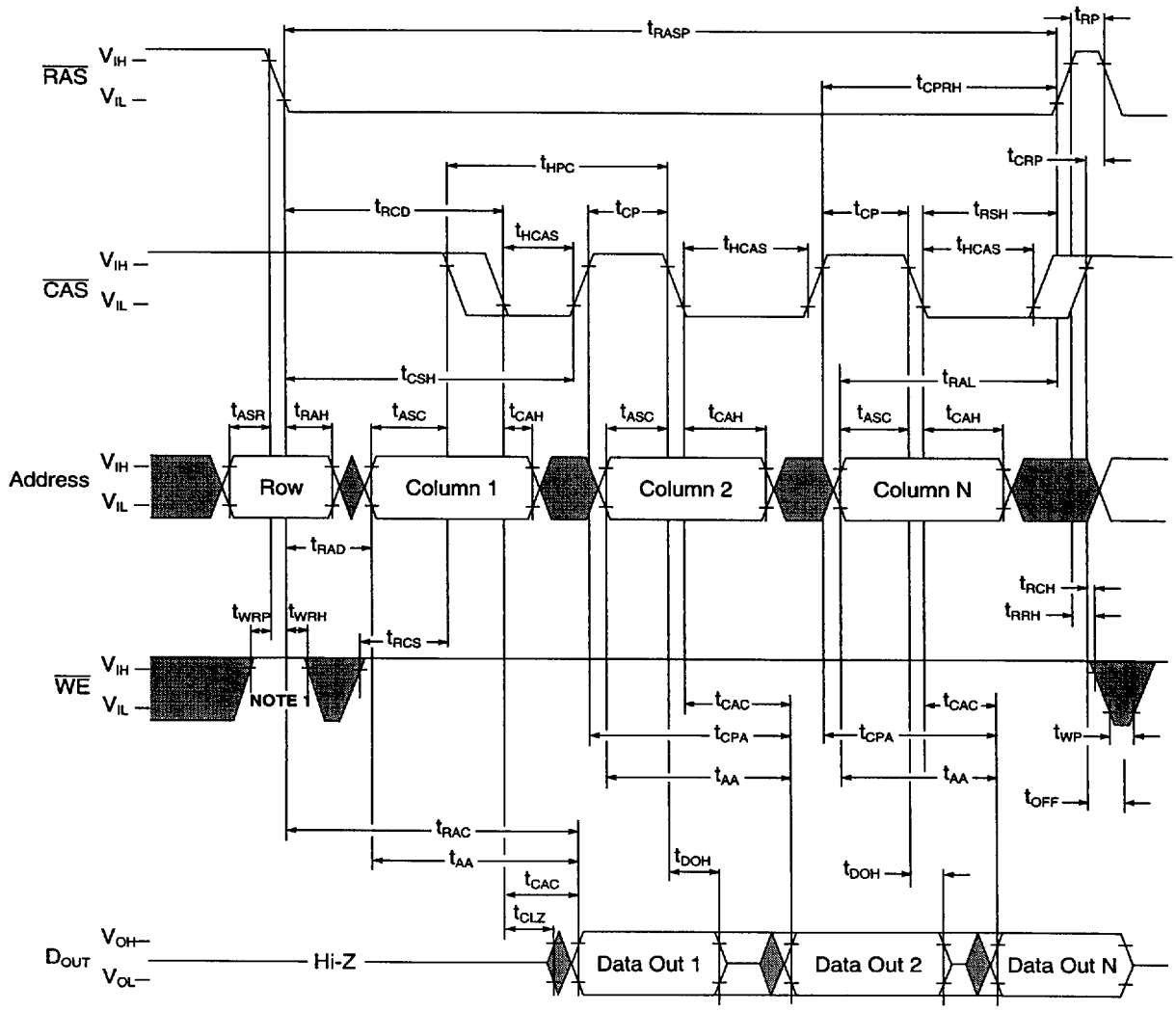
Write Cycle (Early Write)



: "H" or "L"

NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future HPM DRAMs.

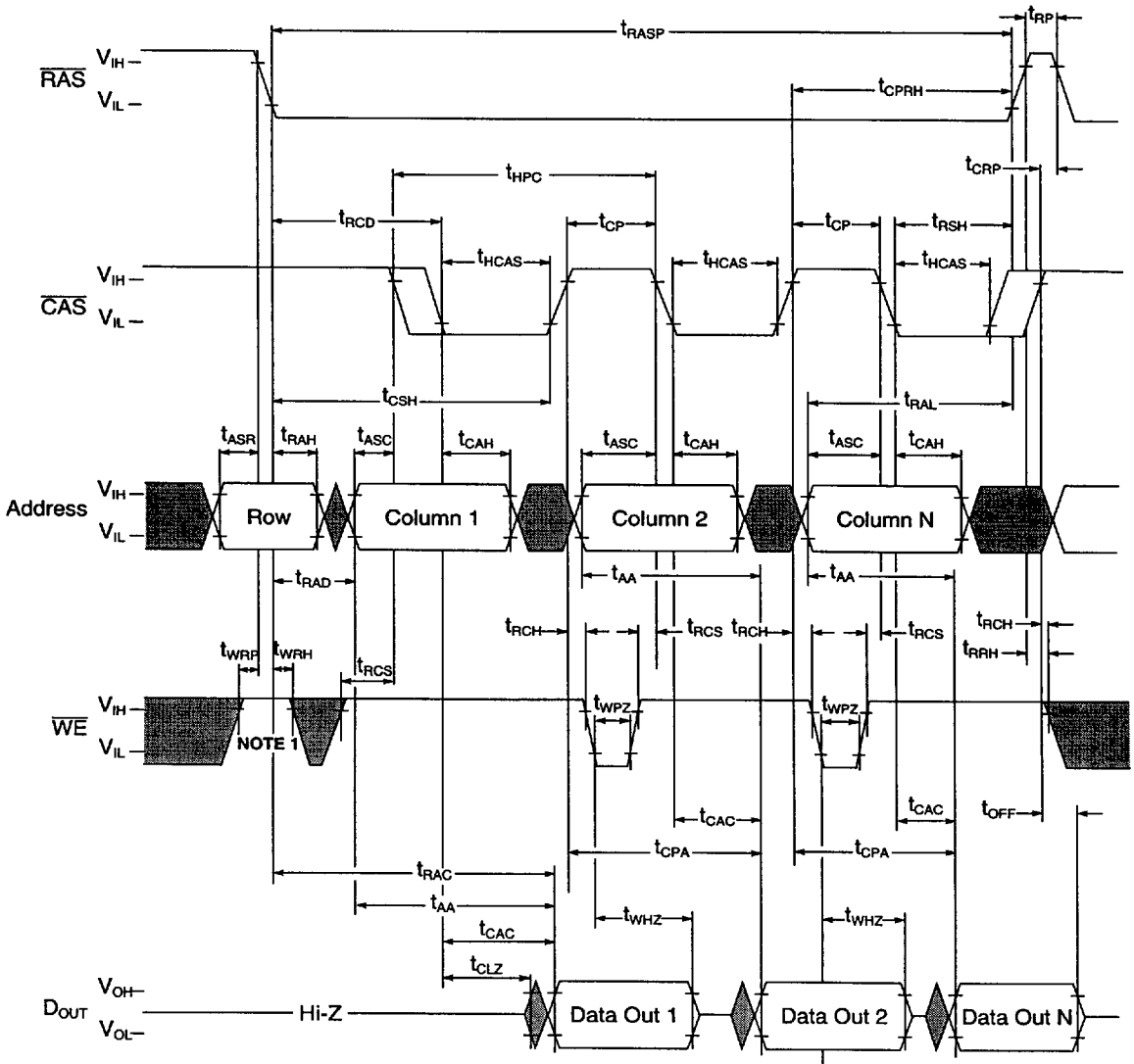
Extended Data Out Mode Read Cycle



: "H" or "L"

NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future HPM DRAMs.

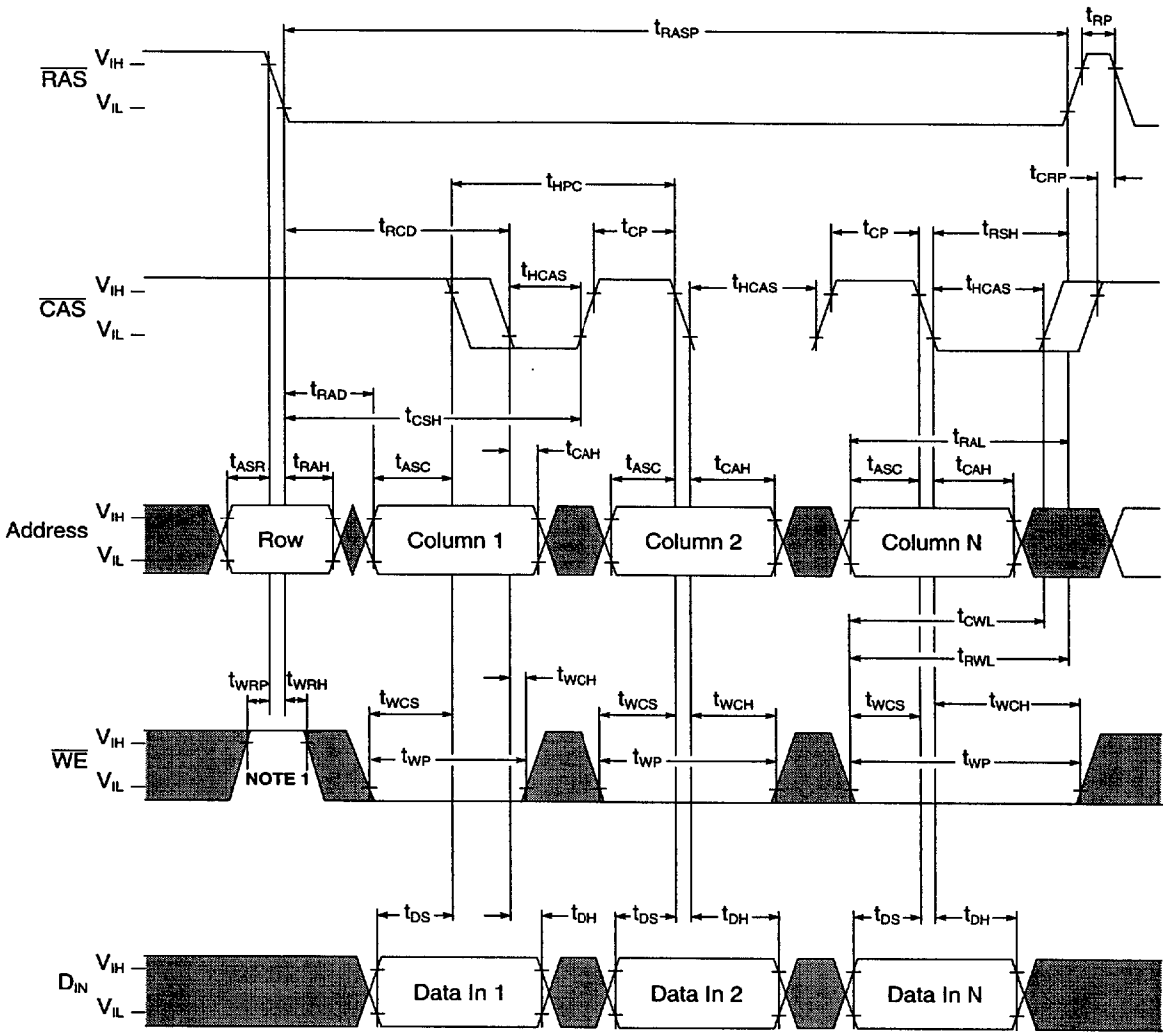
Extended Data Out Mode Read Cycle ($\overline{WE}$ Control)



: "H" or "L"

NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future HPM DRAMs.

Extended Data Out Mode Write Cycle

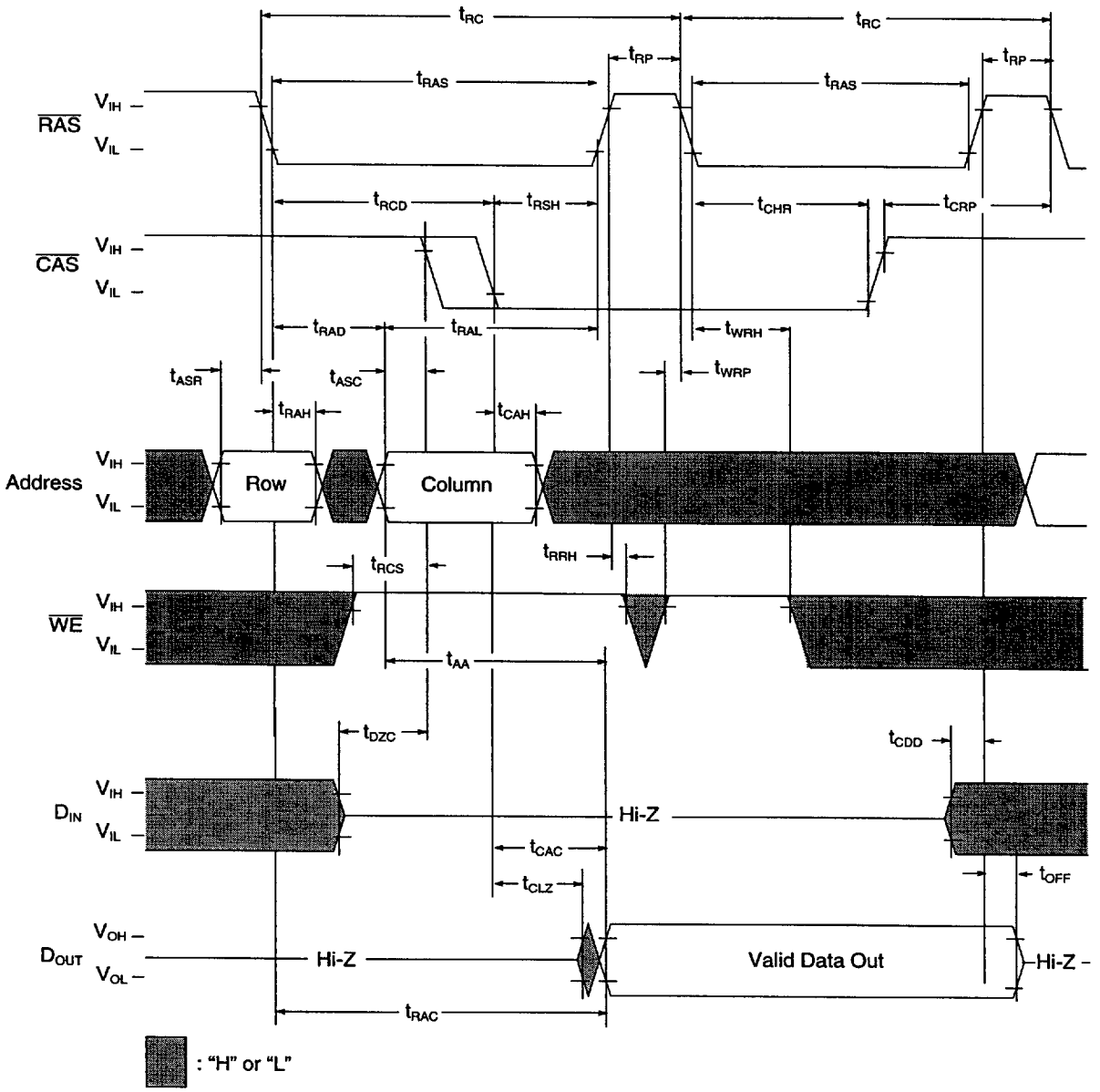


: "H" or "L"

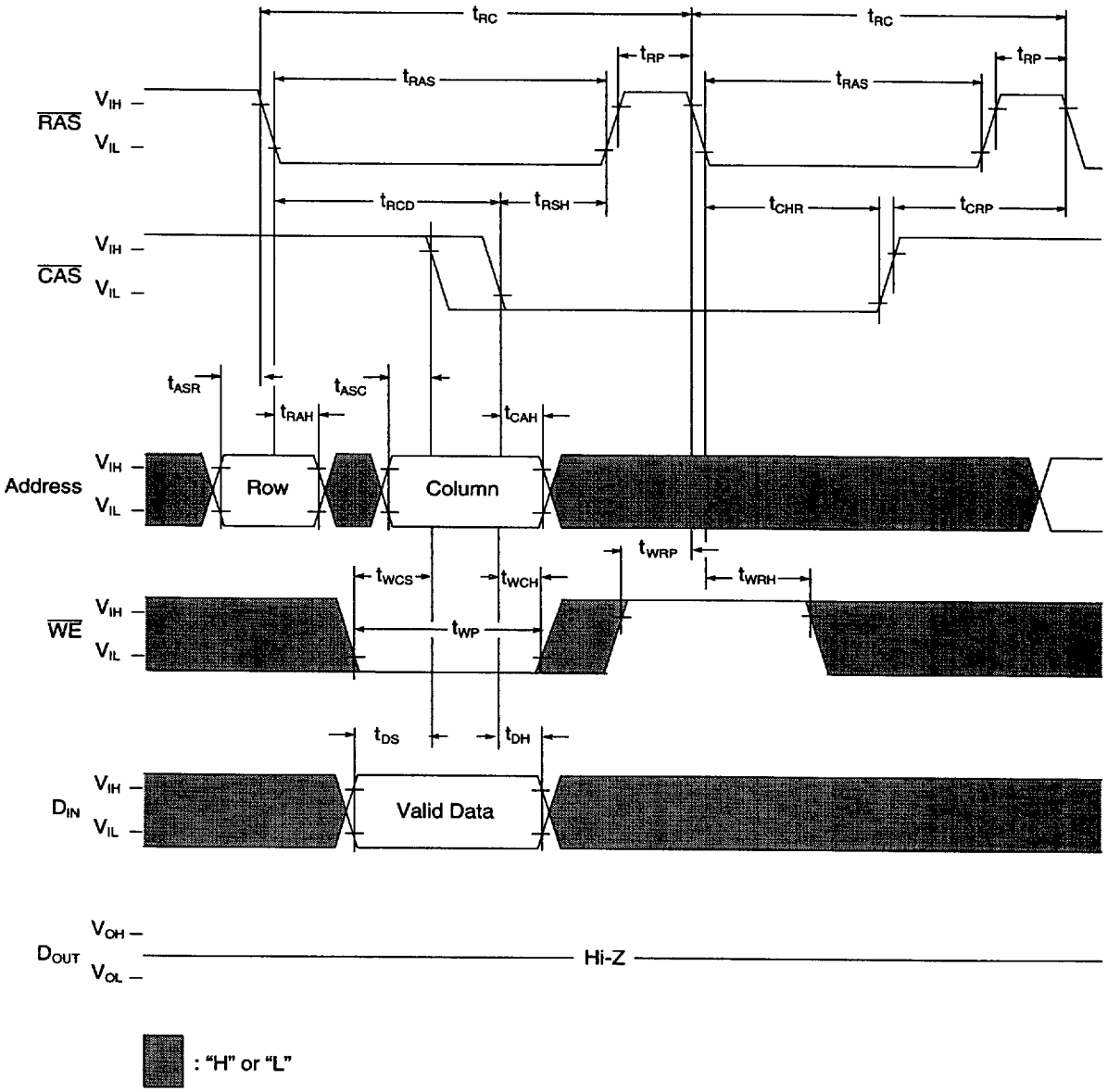
NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future HPM DRAMs.

$\overline{OE}$ = Don't care

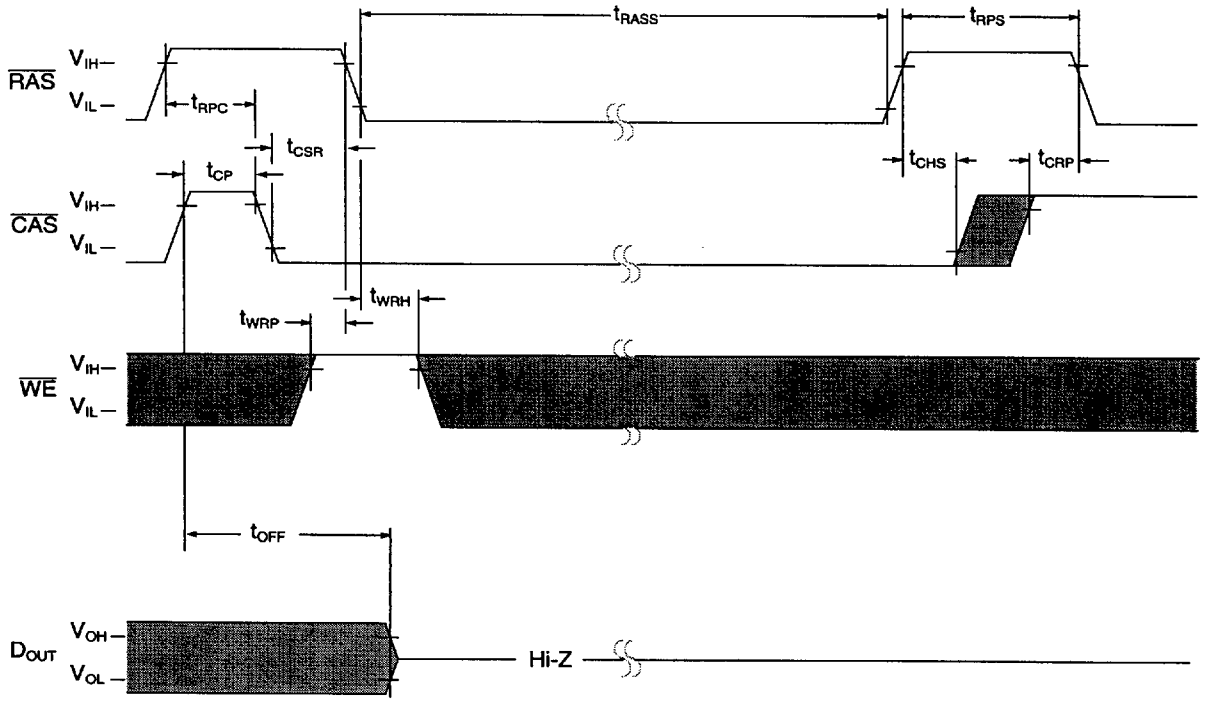
Hidden Refresh Cycle (Read)



Hidden Refresh Cycle (Write)



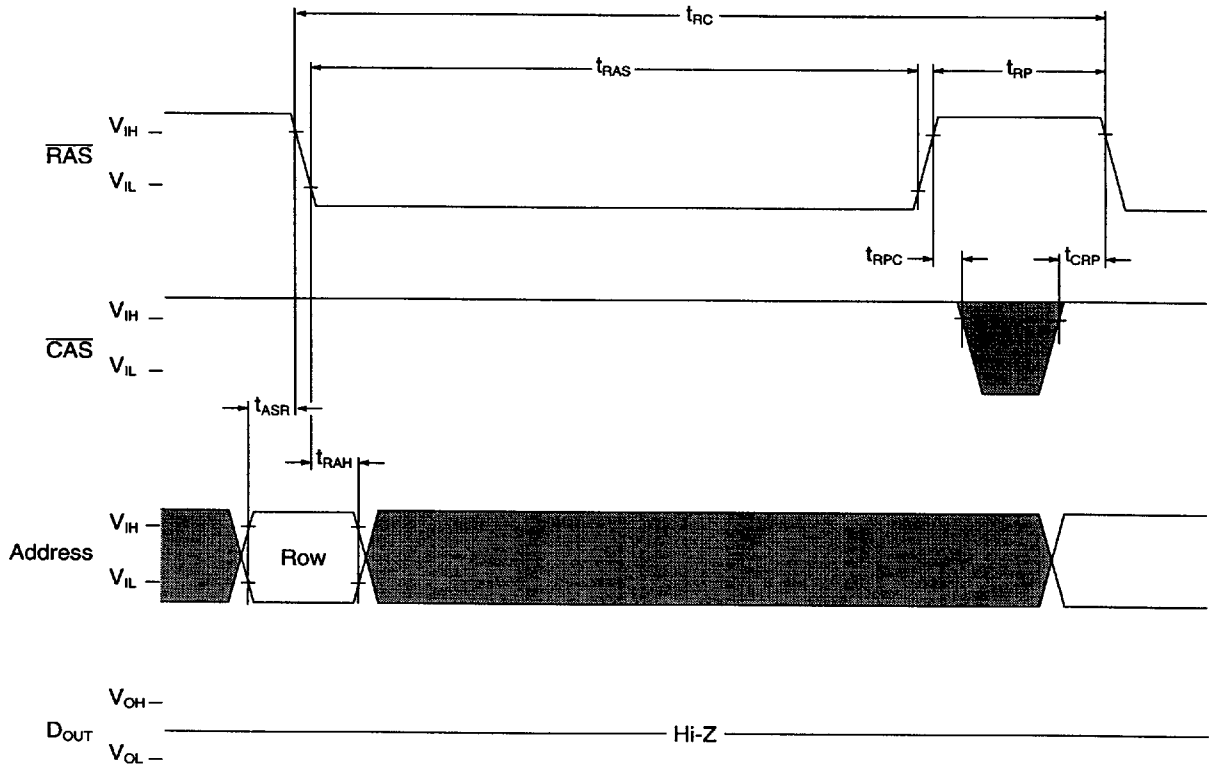
Self Refresh Cycle (Sleep Mode)



: "H" or "L"

NOTE: Address is "H" or "L"
Once t_{RASS} (min) is provided and RAS remains low, the DRAM will be in Self Refresh, commonly known as "Sleep Mode."

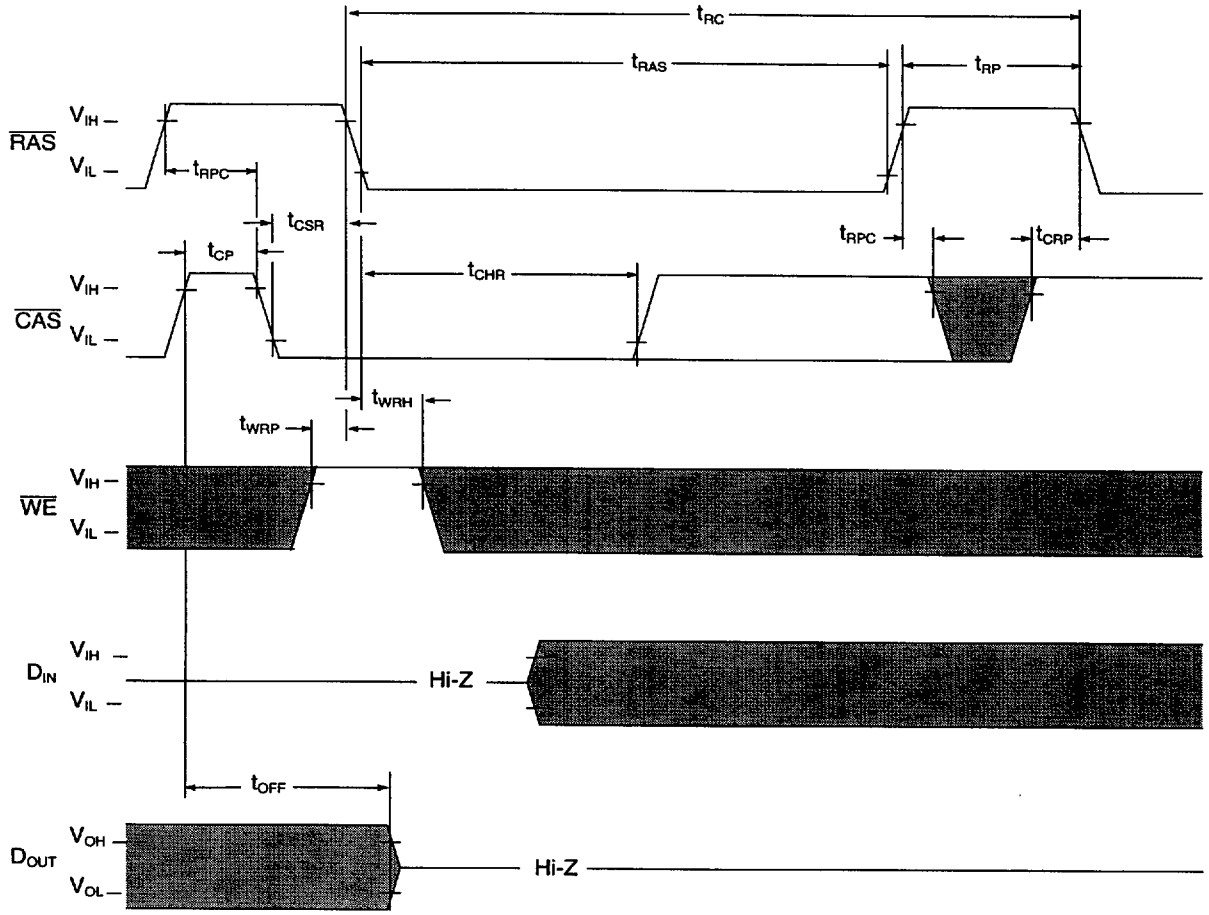
$\overline{RAS}$ Only Refresh Cycle



: "H" or "L"

NOTE: $\overline{WE}$ and D_{IN} are "H" or "L"

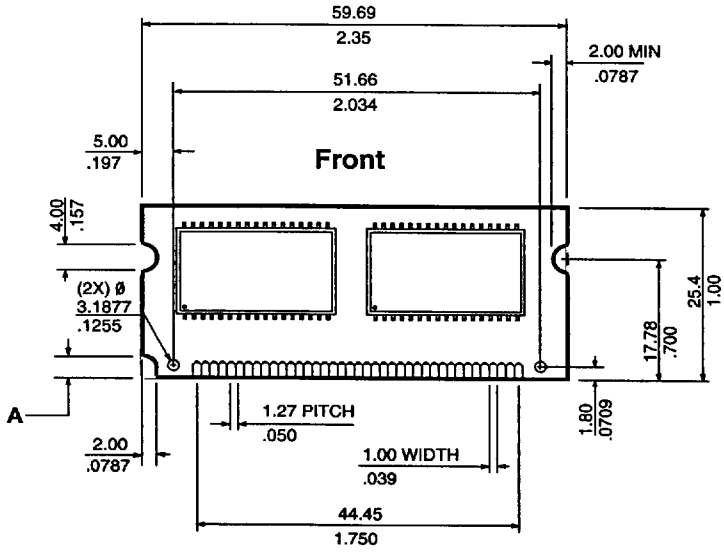
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



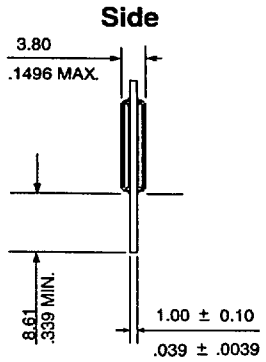
: "H" or "L"

NOTE: Address is "H" or "L"

Layout Drawing



A = $\frac{3.175}{.125}$



Note: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

Revision Log

Rev	Contents of Modification
4/96	Initial release of 8Mx32 EDO specification using 8Mx8 with 11/11 Addressed DRAMs.