KAI - 2093M

1920 (H) x 1080 (V) Pixel

Megapixel Interline CCD Image Sensor

Performance Specification

Eastman Kodak Company

Image Sensor Solutions

Rochester, New York 14650-2010

Revision 2

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TABLE OF CONTENTS

FIGURES

Eastman Kodak Company – Image Sensor Solutions
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1.1 Image Sensor Features

- **2 million pixels, 1920 (H) by 1080 (V)**
- **7.4 µm square pixels**
- **Progressive scan (non-interlaced)**
- **HCCD and output amplifier capable of 40 MHz operation**
- **5 V HCCD clocking**
- **Single or dual video output operation**
- **Each output has 28 light shielded reference columns**
- **9 Frames per second using single output at 20 MHz pixel rate**
- **15 Frames per second using single output at 35 MHz pixel rate**
- **17 Frames per second using dual outputs at 20 MHz pixel rate**
- **30 Frames per second using dual outputs at 37 MHz pixel rate**
- **Only 2 vertical CCD clocks and 2 horizontal CCD clocks**
- **14.2 mm x 8.0 mm imaging area**
- **Electronic shutter**
- **Low Dark Current**
- **Antiblooming protection**

1.2 Description

The KAI-2093M is a high-performance, interline charge-coupled device (CCD) designed for a wide range of medical imaging and machine vision applications. The device is built using an advanced two-phase, double-polysilicon, NMOS CCD technology. The p+npn- photodiodes eliminate image lag while providing antiblooming protection and electronic shutter capability. The 7.4 µm square pixels with microlenses provide high sensitivity and large dynamic range. The two output, split horizontal register enables a 9 to 30 frame per second (fps) video rate with this two megapixel progressive scan imager.

1.3 Image Sensor Layout

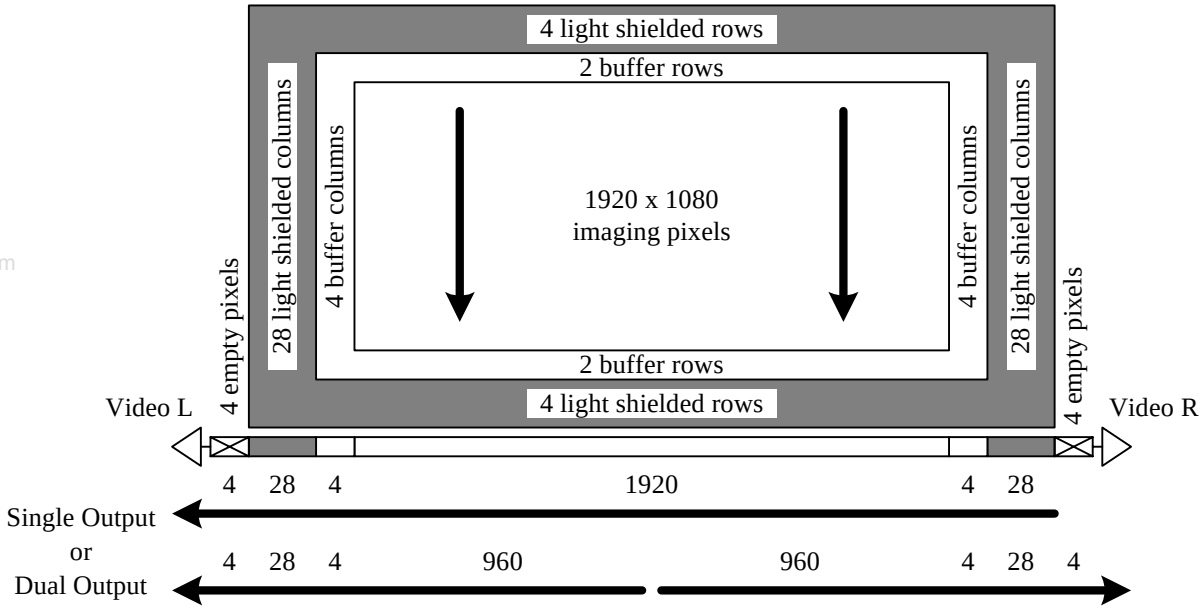


Figure 1 - Sensor Architecture

There are 4 light shielded rows followed by 1084 photoactive rows and finally 4 more light shielded rows. The first and last 2 photoactive rows are buffer rows giving a total of 1080 lines of image data.

In the single output mode all pixels are clocked out of the Video L output in the lower left corner of the sensor. The first four empty pixels of each line do not receive charge from the vertical shift register. The next 28 pixels receive charge from the left light shielded edge followed by 1928 photoactive pixels and finally 28 more light shielded pixels from the right edge of the sensor. The first and last 4 photoactive pixels are buffer pixels giving a total of 1920 pixels of image data.

In the dual output mode the clocking of the right half of the horizontal CCD is reversed. The left half of the image is clocked out Video L and the right half of the image is clocked out Video R. Each row consists of 4 empty pixels followed by 28 light shielded pixels followed by 964 photoactive pixels. When reconstructing the image, data from Video R will have to be reversed in a line buffer and appended to the Video L data.

2.1 Package Drawing

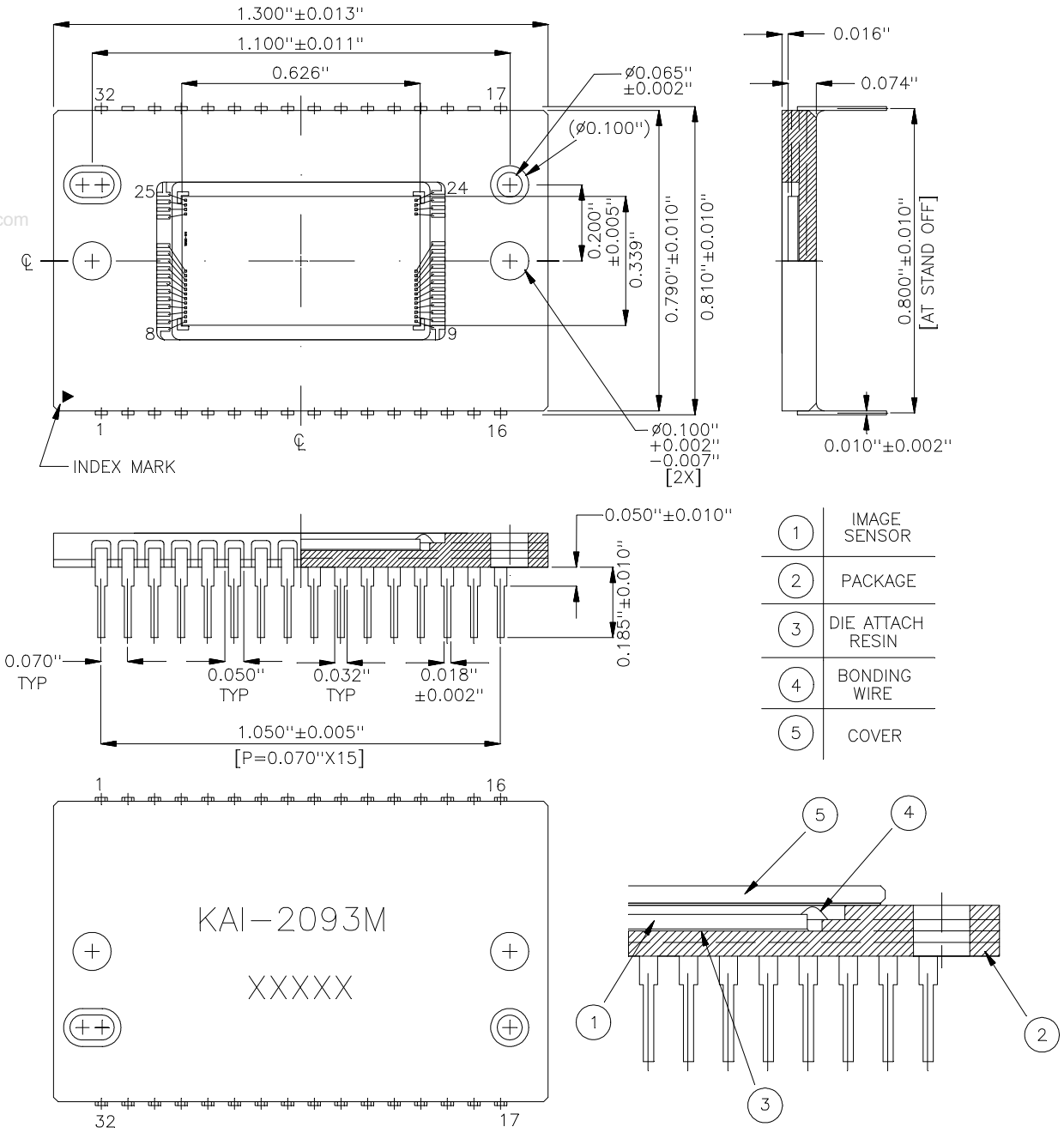


Figure 2 - Package Drawing

2.2 Pin Description

Pin	Label
1	ϕR
2	ϕH2BL
3	ϕH1BL
4	ϕH1SL
5	ϕH2SL
6	GND
7	OG
8	RD
9	RD
10	OG
11	GND
12	ϕH2SR
13	ϕH1SR
14	ϕH1BR
15	ϕH2BR
16	ϕR

Pin	Label
17	VSS
18	VOUTR
19	GND
20	ϕV2O
21	ϕV1
22	VSUB
23	GND
24	VDDR
25	VDDL
26	GND
27	VSUB
28	ϕV1
29	ϕV2E
30	ESD
31	VOUTL
32	VSS

The horizontal shift register is on the side of the sensor parallel to the row of pins 1 through 16. In single output mode the pixel closest to pin 1 will be read out first through Video L, the pixel closest to pin 17 will be read out last. In dual output mode the pixel closest to pin 16 will be read out first through Video R.

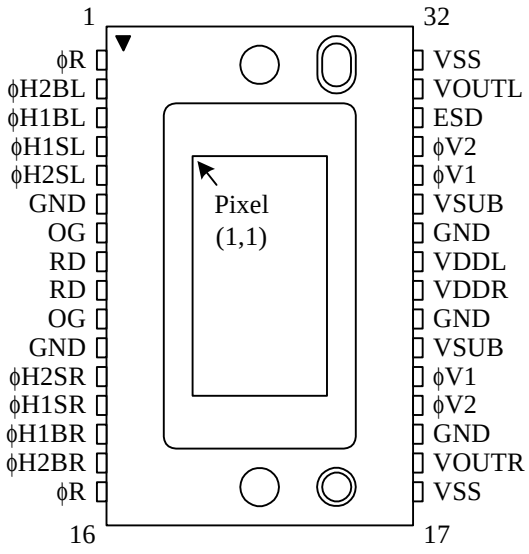


Figure 3 - Package Pin Designations - Top View

3.1 Absolute Maximum Ratings

		Min.	Max.	Units	Notes
Temperature	Operation without damage	-50	70	C	
	Storage	-55	70	C	
Voltage between pins	VSUB to GND	8	20	V	1
	VDD, OG to GND	0	17	V	
	VRD to GND	0	14	V	
	ϕV1 to ϕV2	-20	20	V	
	ϕH1 to ϕH2	-15	15	V	
	ϕR to GND	-15	15	V	
	ϕH1, ϕH2 to OG	-15	15	V	
	ϕH1, ϕH2 to ϕV1, ϕV2	-15	15	V	
Current	Video Output Bias Current	0	10	mA	2

1. For electronic shuttering VSUB may be pulsed to 50 V for up to 10 µs.
2. Total for both outputs. Current is 5 mA for each output. Note that the current bias effects the amplifier bandwidth.

Caution: This device contains limited protection against Electrostatic Discharge (ESD). Devices should be handled in accordance to strict ESD procedures for class 0 devices (HBM). Also, see the ISS Application Note "Electrostatic Discharge Control" MTD/PS-0224.

Caution: Improper cleaning of the cover glass may damage this device. Refer to the ISS Application Note "Cover Glass Cleaning Procedure for Image Sensors" DS 00-009.

3.2 DC Operating Conditions

Symbol	Description	Min.	Nom.	Max.	Units	Notes
OG	Output Gate	-3.0	-2.5	-2.0	V	
VRD	Reset Drain	10.0	10.5	11.0	V	
VSS	Output Amplifier Return	0.0	0.7	1.0	V	
VDD	Output Amplifier Supply	14.5	15.0	15.5	V	
GND	Ground, P-well		0.0		V	
VSUB	Substrate	8.0	TBD	17.0	V	
VESD	ESD Protection	-8.0	-7.0	-6.0	V	1

1. VESD must be at least 1 V more negative than ϕH1L and ϕH2L during sensor operation *AND* during camera power turn on.

3.3 AC Clock Level Conditions

Symbol	Description	Min.	Nom.	Max.	Units	Notes
ϕV2H	Vertical CCD Clock High	7.5	8.0	8.5	V	
ϕV1M, ϕV2M	Vertical CCD Clocks Midlevel	-1.6	-1.5	-1.4	V	
ϕV1L, ϕV2L	Vertical CCD Clocks Low	-9.5	-9.0	-8.5	V	
ϕH1H, ϕH2H	Horizontal CCD Clocks High	0.5	1.0	2.0	V	
ϕH1L, ϕH2L	Horizontal CCD Clocks Low	-5.0	-4.0	-3.8	V	
ϕR	Reset Clock Amplitude		5.0		V	
ϕRL	Reset Clock Low	-4.0	-3.5	-3.0	V	
VShutter	Electronic Shutter Voltage	44	48	52	V	

3.4 Clock Capacitance

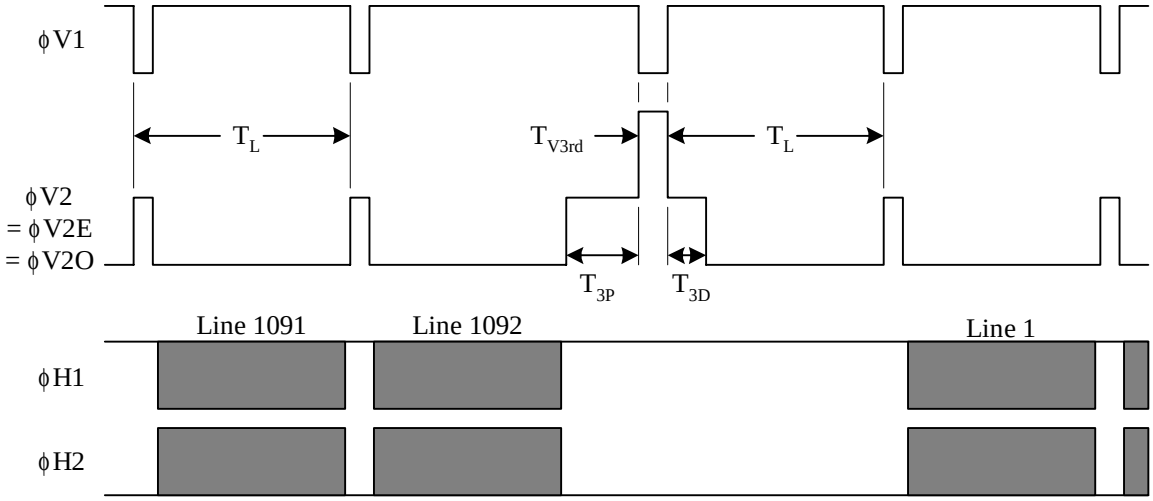
Clocks	Capacitance	Units	Notes
ϕV1 to GND	25	nF	1
ϕV2 to GND	25	nF	1
ϕV1 to ϕV2	5	nF	
ϕH1S to GND	45	pF	2
ϕH2S to GND	38	pF	2
ϕH1B to GND	21	pF	2
ϕH2B to GND	20	pF	2
ϕH2B to ϕH1S	10	pF	2
ϕH1B to ϕH1S	10	pF	2
ϕH2B to ϕH2S	10	pF	2
ϕH1B to ϕH2S	10	pF	2
ϕR to GND	10	pF	

1. Gate capacitance to GND is voltage dependent. Value is for nominal VCCD clock voltages.
2. For nominal HCCD clock voltages, total capacitance for one half (H1SR only or H1SL only).

3.5 AC Timing Conditions

Symbol	Description	Min.	Nom.	Max.	Units	Notes
T_{HD}	HCCD Delay	1.3	1.5	10.0	µs	
T_{VCCD}	VCCD Transfer time	1.3	1.5		µs	
T_{V3rd}	Photodiode Transfer time	8.0	12.0	15.0	µs	
T_{3P}	VCCD Pedestal time	20.0	25.0	50.0	µs	
T_{3D}	VCCD Delay	15.0	20.0	100.0	µs	
T_{R}	Reset Pulse time	5.0	10.0		ns	
T_{S}	Shutter Pulse time	3.0	5.0	10.0	µs	
T_{SD}	Shutter Pulse delay	1.0	1.6	10.0	µs	
T_{H}	HCCD Clock Period	25.0	50.0	200.0	ns	
T_{VR}	VCCD rise/fall time	0.0	0.1	1.0	µs	
T_{VE}	Vertical Clock Edge Alignment	0.0		100.0	ns	

Progressive Frame Timing



Frame Timing for Vertical Binning by 2

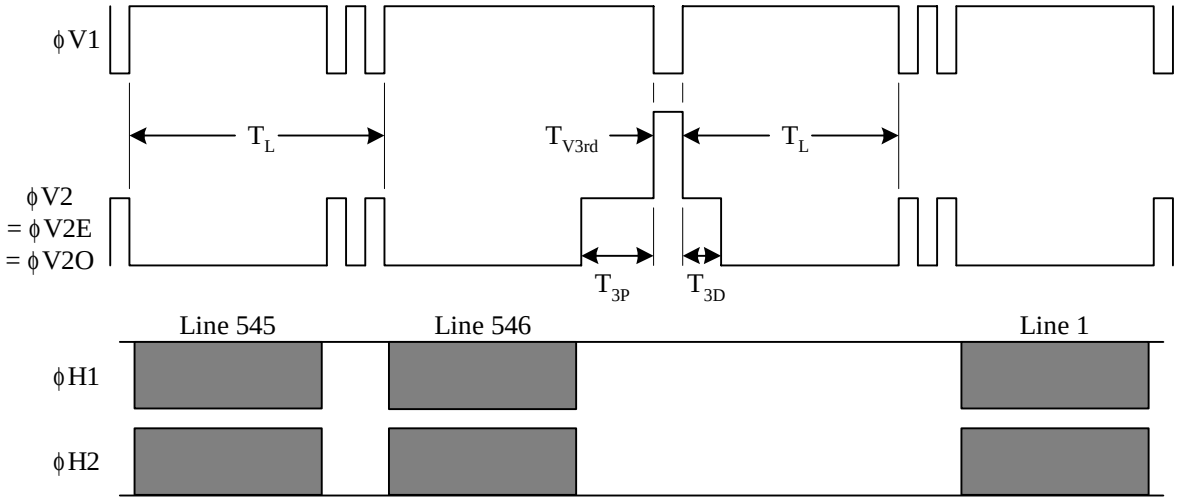


Figure 4 - Progressive Frame Timing

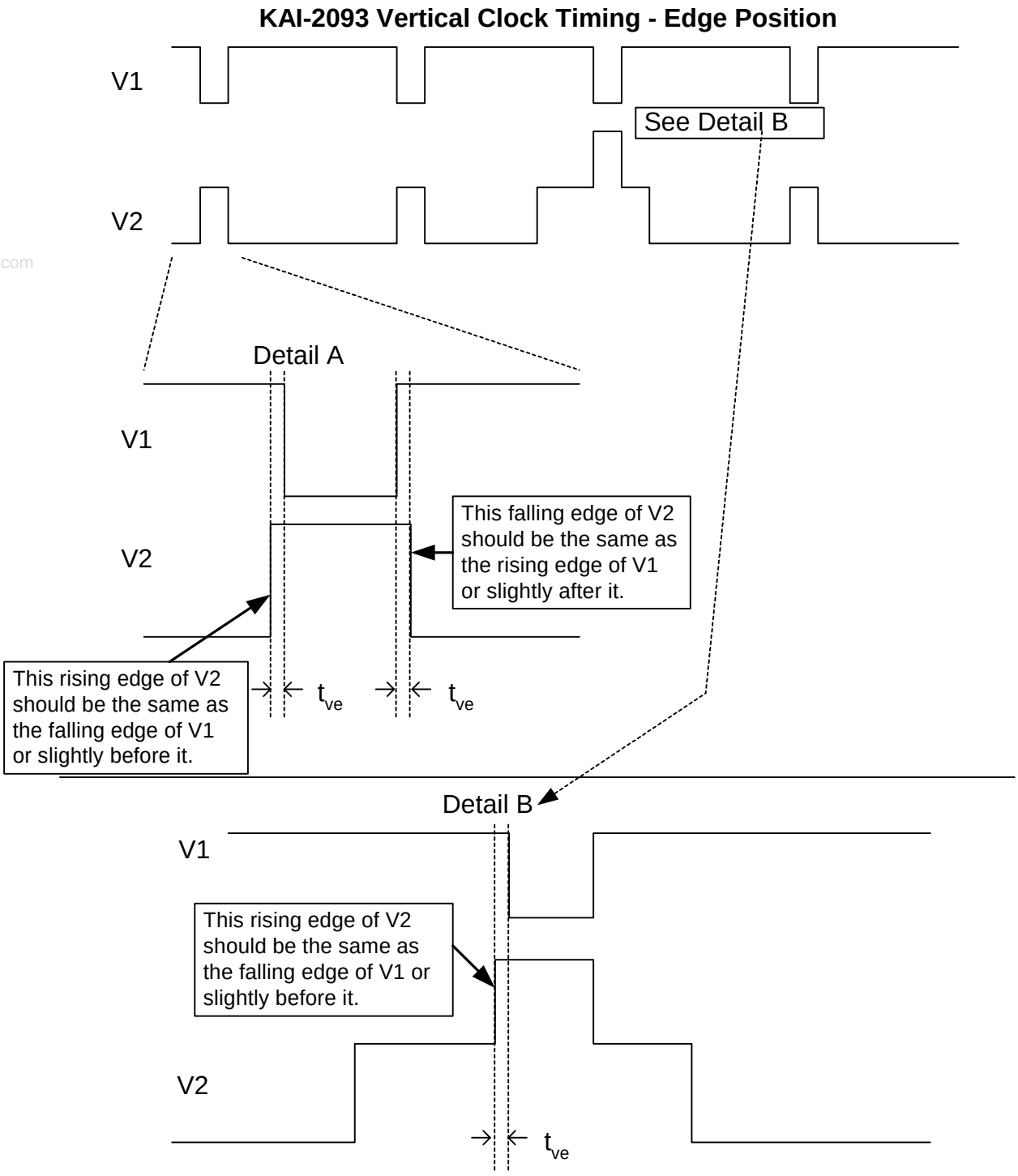
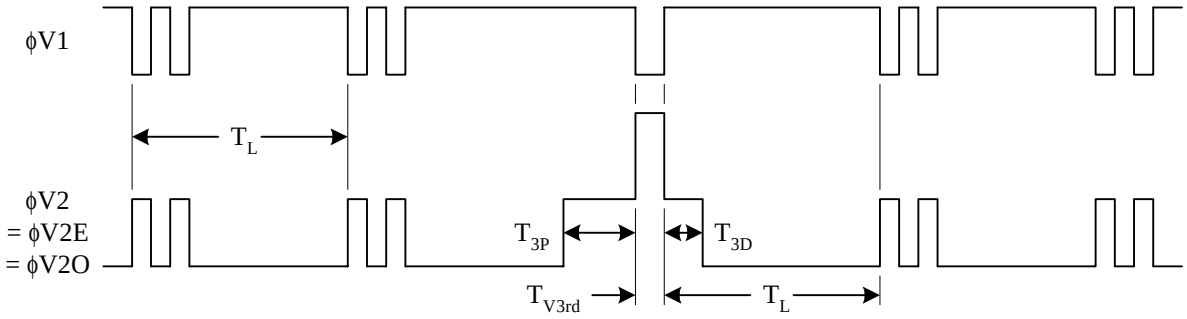


Figure 5 - Ideal Vertical Clock Edge Position

Interlaced Frame Timing - Field Integration Mode - Even Field Readout



Interlaced Frame Timing - Field Integration Mode - Odd Field Readout

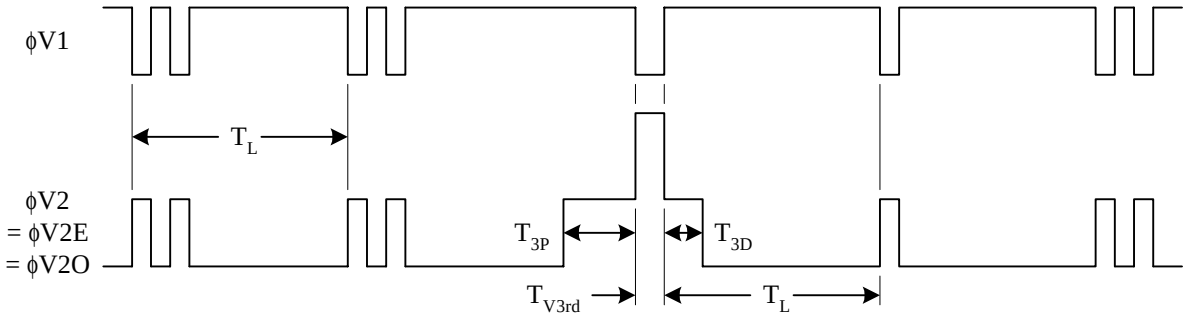
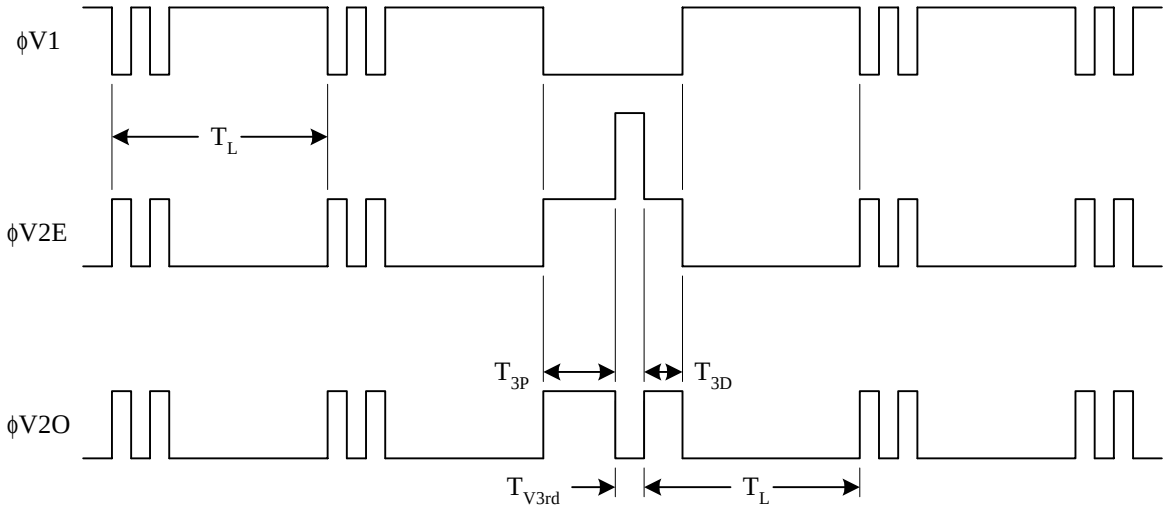


Figure 6 - Interlaced Frame Timing - Field Integration Mode

Interlaced Frame Timing - Frame Integration Mode - Even Field Readout



Interlaced Frame Timing - Frame Integration Mode - Odd Field Readout

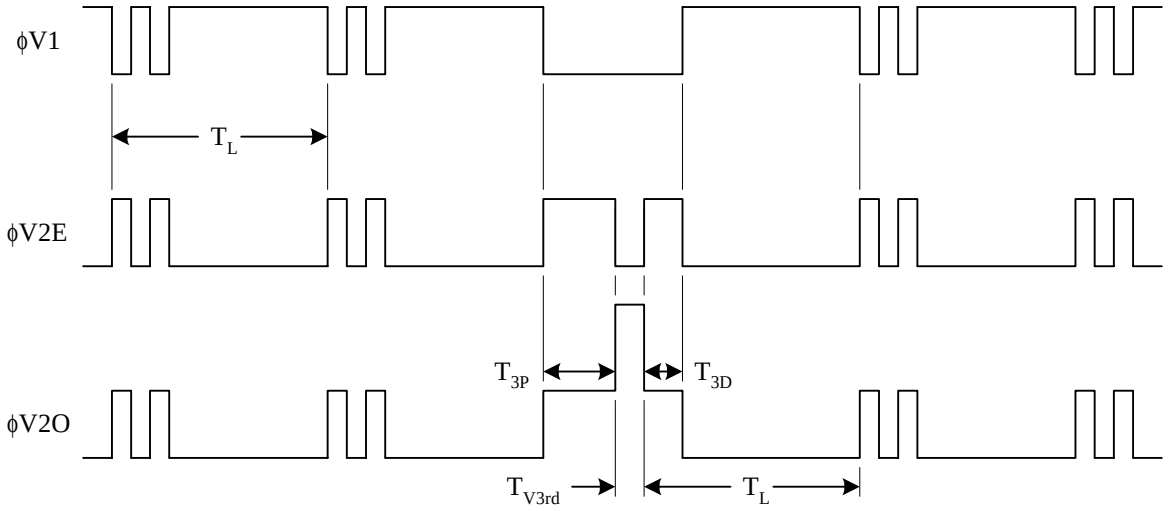
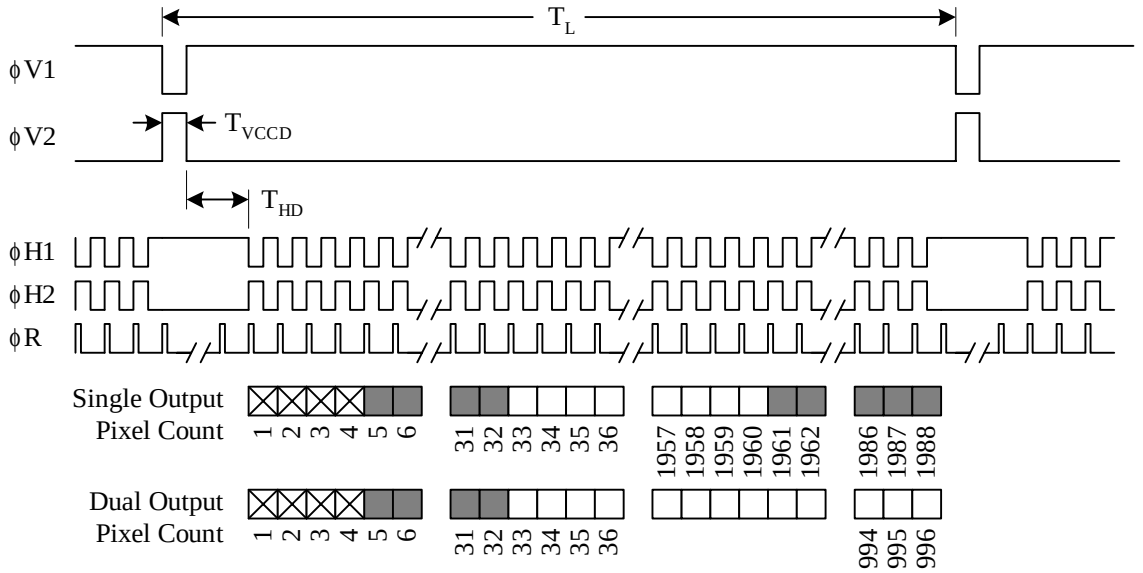


Figure 7 - Interlaced Frame Timing - Frame Integration Mode

Progressive Line Timing



Interlaced Line Timing
and Line Timing for Vertical Binning by Two

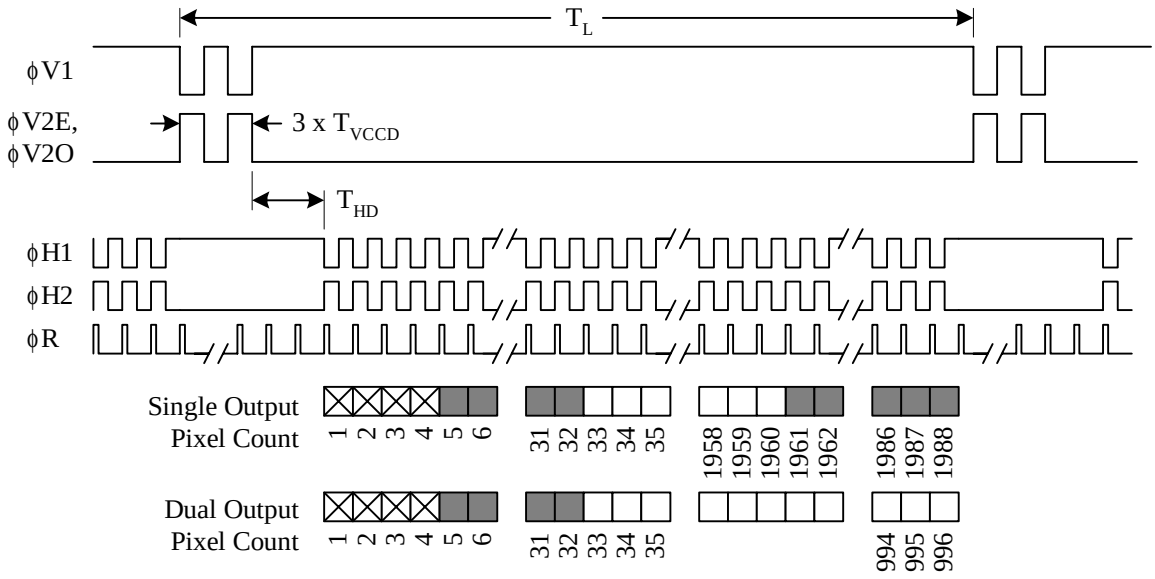
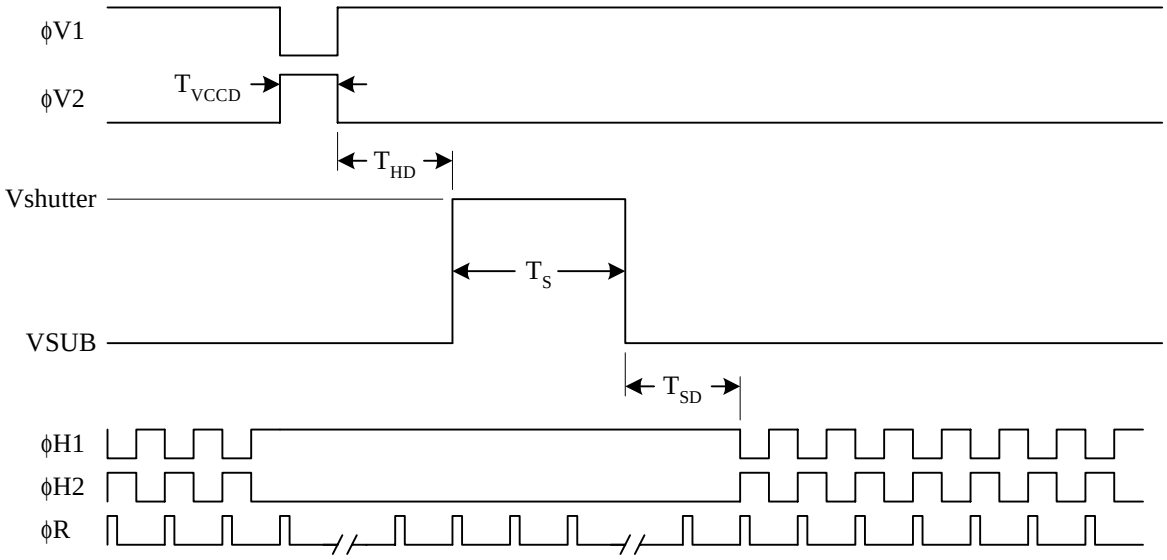


Figure 8 - Line Timing

Electronic Shutter Line Timing



Integration Time Definition

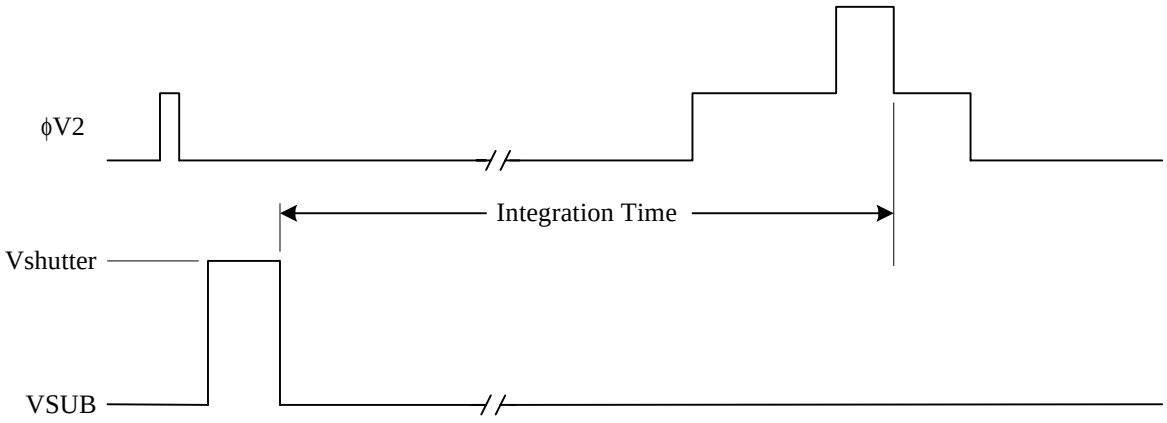


Figure 9 - Electronic Shutter Timing Diagram

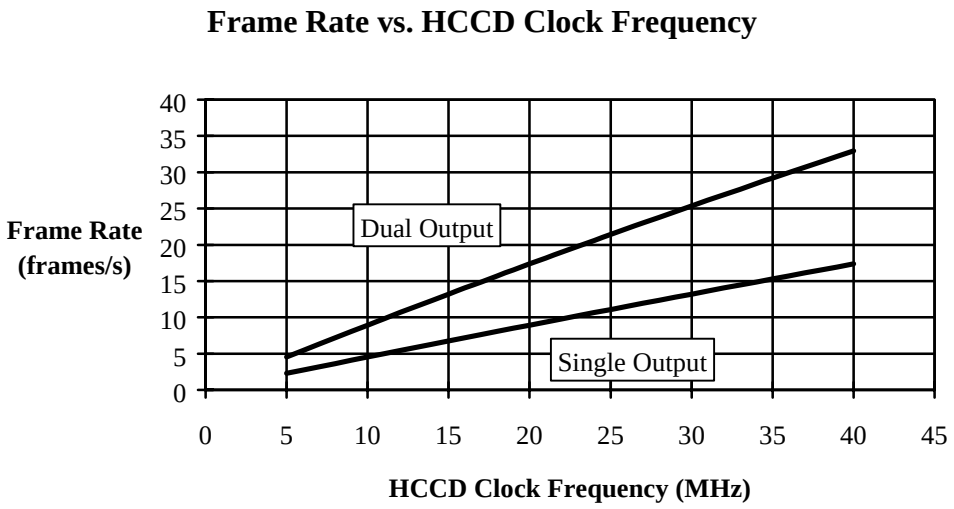


Figure 10 - Progressive Frame Rate vs. HCCD Clock Frequency

4.1 Performance Specifications

Performance Test Conditions

Temperature	40°C
Integration Time	33ms (40 MHz HCCD frequency, 30fps frame rate)
Operation	Nominal voltages and timing
Image defects are excluded from performance tests.	

Optical Specifications

Symbol	Description	Min.	Nom.	Max.	Units	Notes
QE_{max}	Peak Quantum Efficiency	33	36		%	1
λQE	Peak Quantum Efficiency Wavelength		490		nm	1
QE(540)	Quantum Efficiency at 540nm	31	33		%	1
θQE*h*	Microlens Acceptance Angle (horizontal)	±12	±13		degrees	2
θQE*v*	Microlens Acceptance Angle (vertical)	±25	±30		degrees	2
NL	Maximum Photoresponse Nonlinearity		2		%	3, 4
ΔG	Maximum Gain Difference Between Outputs		10		%	3, 4
ΔNL	Maximum Signal Error caused by Nonlinearity Differences		1		%	3, 4

1. For monochrome sensors.
2. Value is the angular range of incident light for which the quantum efficiency is at least 50% of QE_{max} at a wavelength of λQE. Angles are measured with respect to the sensor surface normal in a plane parallel to the horizontal axis (θQE*h*) or in a plane parallel to the vertical axis (θQE*v*).
3. Value is over the range of 10% to 90% of photodiode saturation.
4. Value is for the sensor operated without binning.

CCD Specifications

Symbol	Description	Min.	Nom.	Max.	Units	Notes
VNe	Vertical CCD Charge Capacity	45	50		ke^-	
HNe	Horizontal CCD Charge Capacity		100		ke^-	
PNe	Photodiode Charge Capacity	35	40		ke^-	1
Id	Dark Current		0.3	1.0	nA/cm^2	
Lag	Image Lag		< 10	50	e^-	2
Xab	Antiblooming factor	100	300			3, 4, 5, 6
Smr	Vertical Smear		-75	-72	dB	3, 4

1. This value depends on the substrate voltage setting. Higher photodiode saturation charge capacities will lower the antiblooming specification. Substrate voltage will be specified with each part for nominal photodiode charge capacity.
2. This is the first field decay lag at 70% saturation. Measured by strobe illumination of the device at 70% of photodiode saturation, and then measuring the subsequent frame's average pixel output in the dark.
3. Measured with a spot size of 100 vertical pixels.
4. Measured with F/4 imaging optics and continuous green illumination centered at 550 nm.
5. A blooming condition is defined as when the spot size doubles in size.
6. Antiblooming factor is the light intensity that causes blooming divided by the light intensity which first saturates the photodiodes.

Output Amplifier Specifications

Symbol	Description	Nominal	Unit	Notes
P_d	Power Dissipation		mW	1
F_{-3dB}	Bandwidth	140	MHz	1
C_L	Max Off-chip Load	10	pF	2
A_v	Gain	0.75		1
$\Delta V/\Delta N$	Sensitivity	14	$\mu V/ e^-$	1

1. For a 5 mA output load on each amplifier.
2. With total output load capacitance of C_L= 10 pF between the outputs and AC ground.

General Specifications

Symbol	Description	Nominal	Units	Notes
n_{e-T}	Total Noise	40	e^- rms	1
DR	Dynamic Range	60	dB	2

1. Includes system electronics noise, dark pattern noise and dark current shot noise at 20 MHz.
2. Uses 20LOG(PNe/n_{e-T})

4.2 Typical Quantum Efficiency

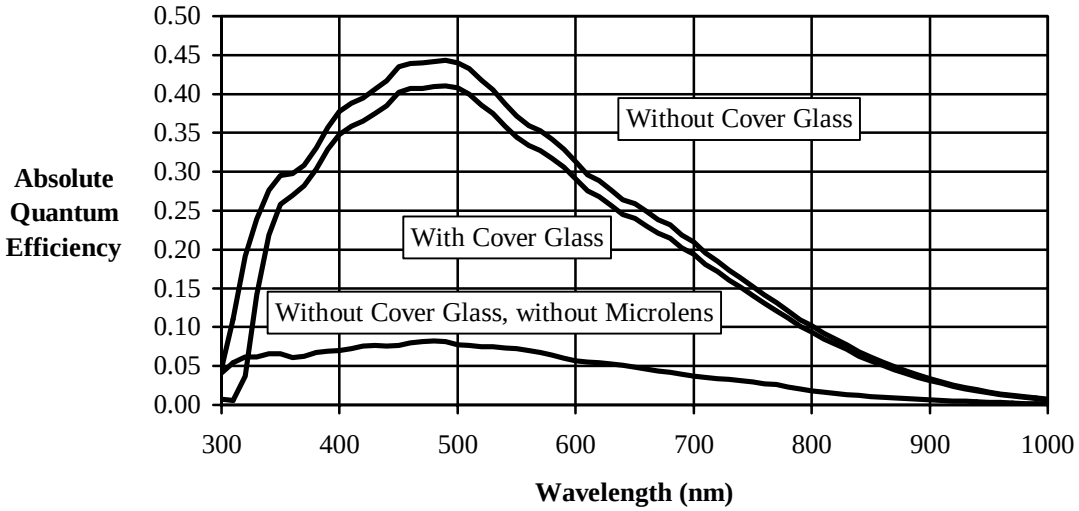


Figure 11 - Quantum Efficiency Spectrum for Monochrome Sensors

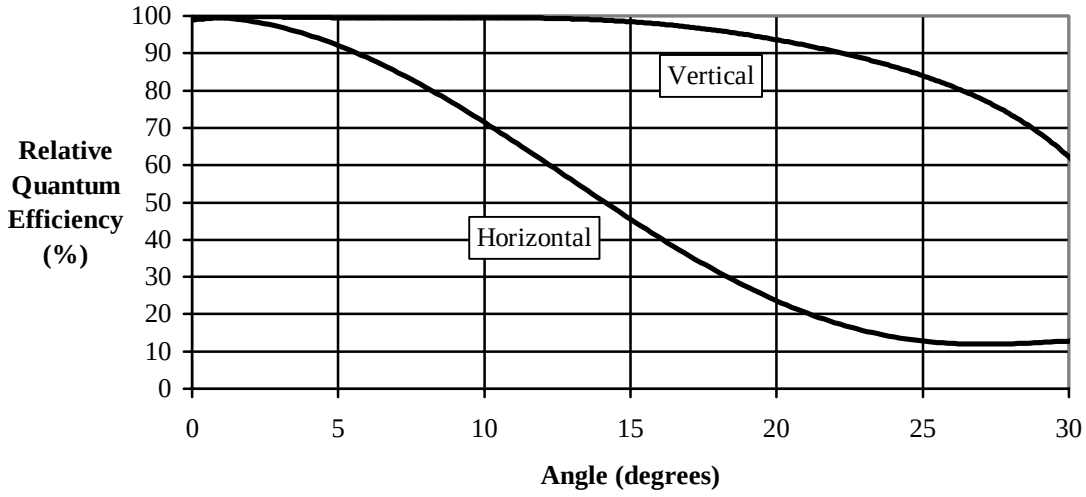


Figure 12 - Angular Dependence of Quantum Efficiency

For the curve marked “Horizontal”, the incident light angle is varied in a plane parallel to the HCCD.
For the curve marked “Vertical”, the incident light angle is varied in a plane parallel to the VCCD.

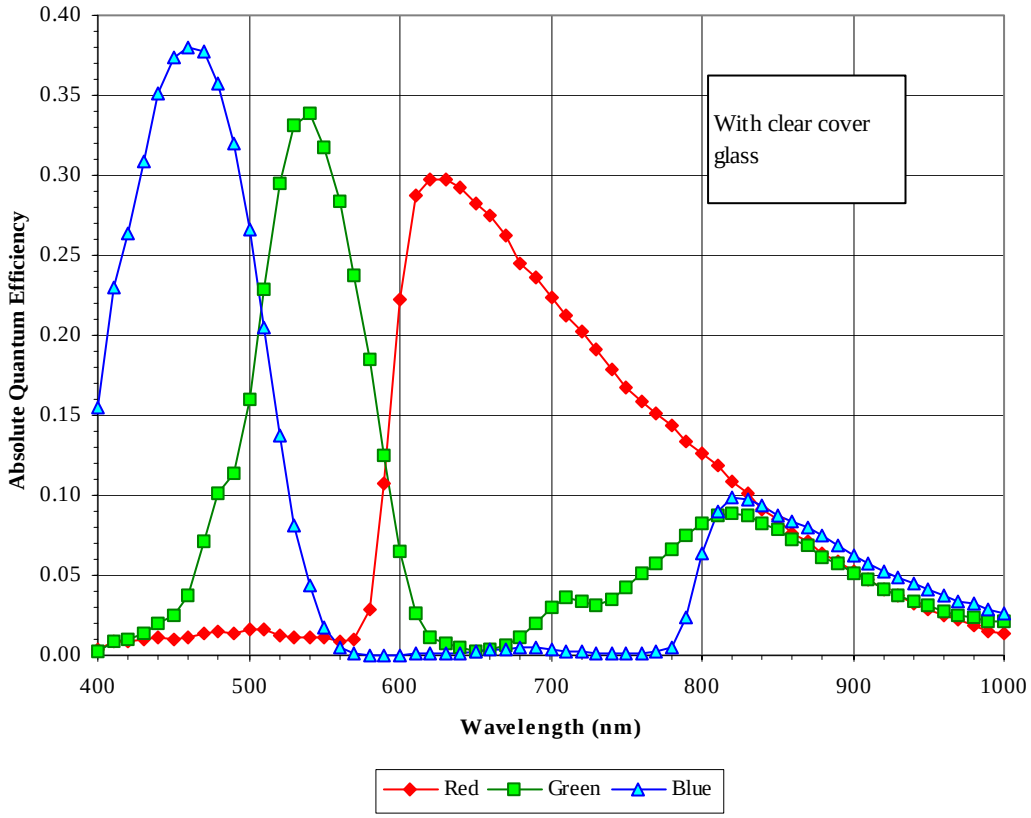


Figure 13 – Quantum Efficiency Spectrum for Color Filter Array Sensors

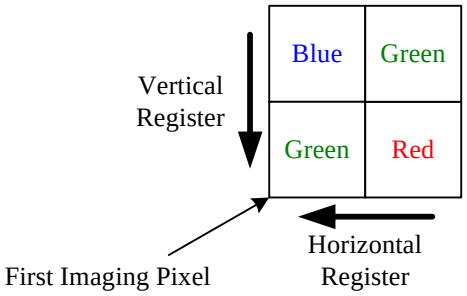


Figure 14 – Color Filter Array Pattern

4.3 Operation Notes

Progressive and Interlaced Timing
Progressive and interlaced output modes are achieved by the applying the proper waveforms to the vertical clock input pins ϕV1, ϕV2E and ϕV2O. For progressive output, ϕV2 = ϕV2E = ϕV2O, with each of the 1092 lines read out individually using the timing in Figure 4.

For interlaced output, there are two modes, field integration mode and frame integration mode. In both modes, 1092/2 = 546 lines are read in each frame readout, with one even frame readout and one odd frame readout necessary for a complete frame. Field integration mode bins together alternate lines, and the timing is shown in Figure 5. As with progressive readout, ϕV2 = ϕV2E = ϕV2O.

Frame integration mode reads out the photodiodes of the even and odd lines separately, and the timing is shown in Figure 6. In this case, ϕV2E and ϕV2O are clocked individually.

Single Output Mode
When operating the sensor in single output mode all pixels of the image sensor will be shifted out the Video L output (pin 31). To conserve power and lower heat generation the output amplifier for Video R may be turned off by connecting VDDR (pin 24) and VOUTR (pin 18) to GND (zero volts).

The ϕH1 timing from the timing diagrams should be applied to ϕH1SL, ϕH1BL, ϕH1SR, ϕH2BR, and the ϕH2 timing should be applied to ϕH2SL, ϕH2BL, ϕH2SR, ϕH1BR. In other words, the clock driver generating the ϕH1 timing should be connected to pins 4, 3, 13, and 15. The clock driver generating the ϕH2 timing should be connected to pins 2, 5, 12, and 14.

The horizontal CCD should be clocked for 4 empty pixels plus 28 light shielded pixels plus 1928 photoactive pixels plus 28 light shielded pixels for a total of 1988 pixels.

Dual Output Mode
In dual output mode the connections to the ϕH1BR and ϕH2BR pins are swapped from the single output mode to change the direction of charge transfer of the right side horizontal shift register. In dual output mode both VDDL and VDDR (pins 25, 24) should be connected to 15 V.

The ϕH1 timing from the timing diagrams should be applied to ϕH1SL, ϕH1BL, ϕH1SR, ϕH1BR, and the ϕH2 timing should be applied to ϕH2SL, ϕH2BL, ϕH2SR, ϕH2BR. The clock driver generating the ϕH1 timing should be connected to pins 4, 3, 13, and 14. The clock driver generating the ϕH2 timing should be connected to pins 2, 5, 12, and 15.

The horizontal CCD should be clocked for 4 empty pixels plus 28 light shielded pixels plus 964 photoactive pixels for a total of 996 pixels.

If the camera is to have the option of dual or single output mode, the clock driver signals sent to ϕH1BR and ϕH2BR may be swapped by using a relay. Another alternative is to have two extra clock drivers for ϕH1BR and ϕH2BR and invert the signals in the timing logic generator. If two extra clock drivers are used, care must be taken to ensure the rising and falling edges of the ϕH1BR and ϕH2BR clocks occur at the same time (within 3 ns) as the other HCCD clocks.

Exposure Control

If the sensor is operated at 20 MHz horizontal CCD frequency then the frame rate will be 9 fps and the integration time will be 1/9 s or 111 ms. To achieve shorter integration times, the electronic shutter option may be used by applying a pulse to the substrate (pins 22 and 27). The time between the falling edge of the substrate pulse and the falling edge of the transition of the ϕV2 clock from ϕV2H to ϕV2M is defined as the integration time. The substrate pulse and integration time are shown in Figure 8.

Integration times longer than one frame time (111 ms in this example) do not require use of the electronic shutter. Without the electronic shutter the integration time is defined as the time between when the ϕV2 clock is at the ϕV2H level of 9.5 V (when the ϕV2 clock is at the ϕV2H level charge collected in the photodiodes is transferred to the vertical shift register). To extend the integration time, increase the time between each ϕV2H level of the ϕV2 clock. While the photodiodes are integrating photoelectrons the vertical and horizontal shift registers should be continuously clocked to prevent the collection of dark current in the vertical shift register. This is most easily done by increasing the number of lines read out of the image sensor. For example, to double the integration time read out 2184 lines instead of 1092 lines (but remember only the first 1092 lines will contain image data).

Depending on the image quality desired and temperature of the sensor, integration times longer than one second may require the sensor to be cooled to control dark current. The output amplifiers will also generate a non-uniform dark current pattern near the bottom corners of the sensor. This can be reduced at long integration times by only turning on VDD to each amplifier during image readout. If the vertical and horizontal shift registers are also stopped during integration time, the dark current in the shift registers should be flushed out completely before transferring charge from the photodiodes to the vertical shift register.

Dark References

There are 28 light shielded columns at the left and right side of the image sensor. The first and last two light shielded columns should not be used as a dark reference due to some light leakage under the edges of the light shielding. Only the center 24 columns should be used for dark reference line clamping. There are 4 light shielded rows at the top and bottom of the image sensor. Only the center two light shielded rows should be used as a dark reference.

Connections to the Image Sensor

The reset clock signal operates at the pixel frequency. The traces on the circuit board to the reset clock pins should be kept short and of equal length to ensure that the reset pulse arrives at each pin simultaneously. The circuit board traces to the horizontal clock pins should also be placed to ensure that the clock edges arrive at each pin simultaneously. If reset pulses and the horizontal clock edges are misaligned the noise performance of the sensor will be degraded and balancing the offset and gain of the two output amplifiers will be difficult.

The bias voltages on OG, RD, VSS and VDD should be well filtered with capacitors placed as close to the pins as possible. Noise on the video outputs will be most strongly effected by noise on VSS, VDD, GND, and VSUB. If the electronic shutter is not used then a filtering capacitor should also be placed on VSUB. If the electronic shutter is used, the VSUB voltage should be kept as clean and noise free as possible.

The voltage on VSS may be set by using the 0.6 to 0.7 volt drop across a diode. Place the diode from VSS to GND. To disable one of the output amplifiers connect VDD to GND, do not let VDD float.

The ESD voltage must reach its operating point before any of the horizontal clocks reach their low level. If any pin on the sensor comes within 1 V of the ESD pin the electrostatic damage protection circuit will become active and will not turn off until all voltages are powered down. Operating the sensor with the ESD protection circuit active may damage the sensor.

4.4 Defect Specifications

Defect Test Conditions

Temperature	40°C
Integration Time	33ms (40 MHz HCCD frequency, no binning, 30fps frame rate)
Light source	Continuous green illumination centered at 550nm
Operation	Nominal voltages and timing

Defect Definitions

Name	Definition	Maximum Number
Major Defective Pixel	A pixel whose signal deviates by more than 25 mV from the mean value of all active pixels under dark field condition or by more than 15% from the mean value of all active pixels under uniform illumination of 80% of saturation	10
Minor Defective Pixel	A pixel whose signal deviates by more than 8 mV from the mean value of all active pixels under dark field conditions	100
Cluster Defect	A group of 2 to 10 contiguous major defective pixels with a width no wider than 2 defective pixels	4
Column Defect	A group of more than 10 contiguous major defective pixels along a single column	0

Note: There will be at least two non-defective pixels separating any two major defective pixels.

5.1 Quality Assurance and Reliability

5.1.1 Quality Strategy: All devices will conform to the specifications stated in this document. This is accomplished through a combination of statistical process control and inspection at key points of the production process.

5.1.2 Replacement: All devices are warranted against failures in accordance with the Terms of Sale.

5.1.3 Cleanliness: Devices are shipped free of contamination, scratches, etc. that would cause a visible defect.

5.1.4 ESD Precautions: Devices are shipped in static-safe containers and should only be handled at static-safe work stations.

5.1.5 Reliability: Information concerning the quality assurance and reliability testing procedures and results are available from the Image Sensor Solutions Division, and can be supplied upon request.

5.1.6 Test Data Retention: Devices have an identifying number traceable to a test data file. Test data is kept for a period of 2 years after date of shipment.

5.2 Ordering Information

Address all inquiries and purchase orders to:

Image Sensor Solutions
Eastman Kodak Company
Rochester, New York 14650-2010
Phone: (585) 722-4385
Fax: (585) 477-4947
E-mail: imagers@kodak.com

Kodak reserves the right to change any information contained herein without notice. All information furnished by Kodak is believed to be accurate.

WARNING: LIFE SUPPORT APPLICATIONS POLICY

Kodak image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of the Eastman Kodak Company. Product warranty is limited to replacement of defective components and does not cover injury or property or other consequential damages.

6.1 Revision Changes

Revision Number	Description of Changes
0	Initial formal version.
1	• Page 8 section 3.5 AC Timing Conditions table: Added Tve: Vertical Clock Edge Alignment • Page 10: Added Figure 5 Vertical Clock Timing – Edge Position • Page 15: Updated Figure 9 Frame Rate to show dual mode out to 40MHz. Previous plot cut off dual mode at 35 MHz • Page 22: Added that a cluster defect will be no wider that two defective pixels. • Page 22: Added a note that there will be at least two good pixels between any two major defects (pixels or clusters) • Removed appendix 1 • Added revision changes
2	Section 4.2: Updated the color Quantum Efficiency plot for the new pigment Color Filter Arrays.