M5244FP

LEVEL CONTROLLER FOR PHOTO DETECTION

DESCRIPTION

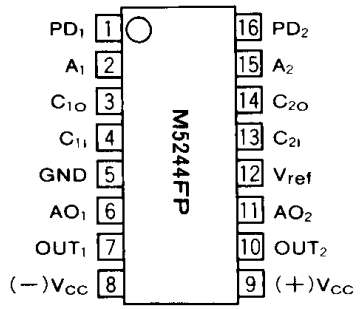
M5244FP is a photo-reception amplifier which performs the impedance conversion for small signals received by a photo-reception diode, converts their absolute values into binary-code signals and outputs the results to a comparator.

The input stage performs the impedance conversion using a J-FET type high-sensitive operational amplifier. Amplifiers, DC servo circuits, and comparators in the later stages output H/L (binary-code) signals. Thus, this device provides high performance and functions and is best suitable for photo-reception devices such as faximiles, etc.

FEATURES

- SOP package is used to decrease the size and weight of application devices.
- Contains a Bi-FET operational amplifier (equivalent to that of M5238) with high-input impedance, allowing few nA of input signals to be processed.
- Contains 2-stage of low-noise operation circuits whose gain has been set internally. (Total gain = about 60dB)
- Can accept weak analog signals, amplify them, and use them as a monitor output pin. (Analog output pin)
- Contains very accurate zero compensation circuits.
  - DC servo circuit
  - Low level detection circuit
- Contains a highly sensitive comparator with hysteresis characteristics.
- Requires few external devices.
- You can easily design the photo-reception sections using 4, 6, or more devices because the device contains two circuits.

PIN CONFIGURATION (TOP VIEW)



Outline 16P2S

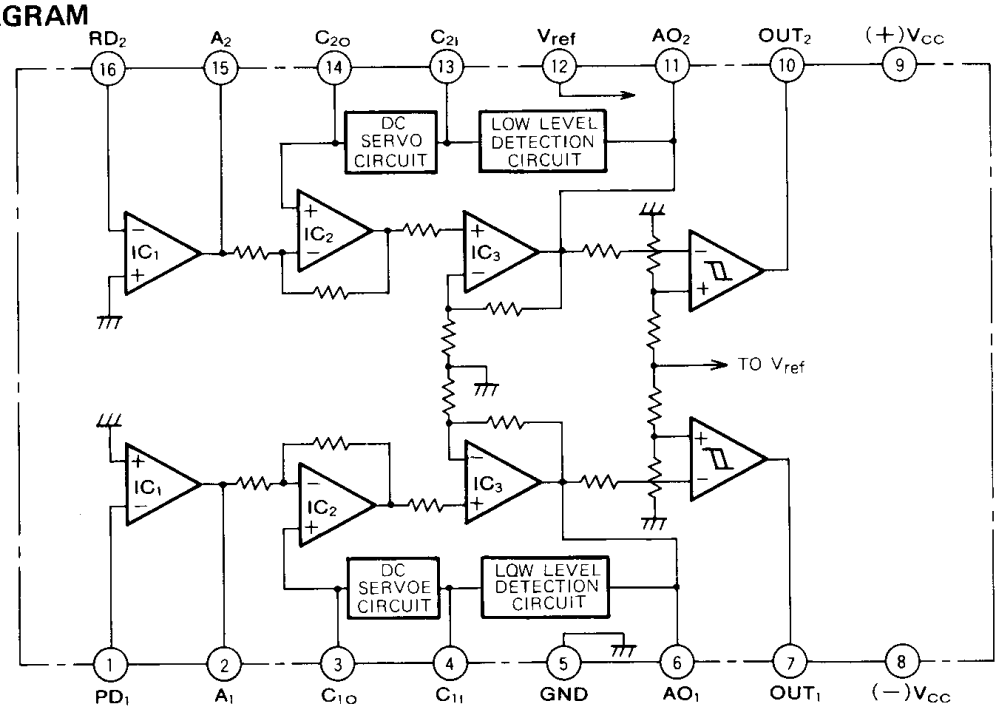
APPLICATION

OA equipments such as faximiles which use photo-reception units

RECOMMENDED OPERATING CONDITIONS

(+) V_{CC} . . . . . +5V
(−) V_{CC} . . . . . −12V
V_{ref} . . . . . +2V

BLOCK DIAGRAM



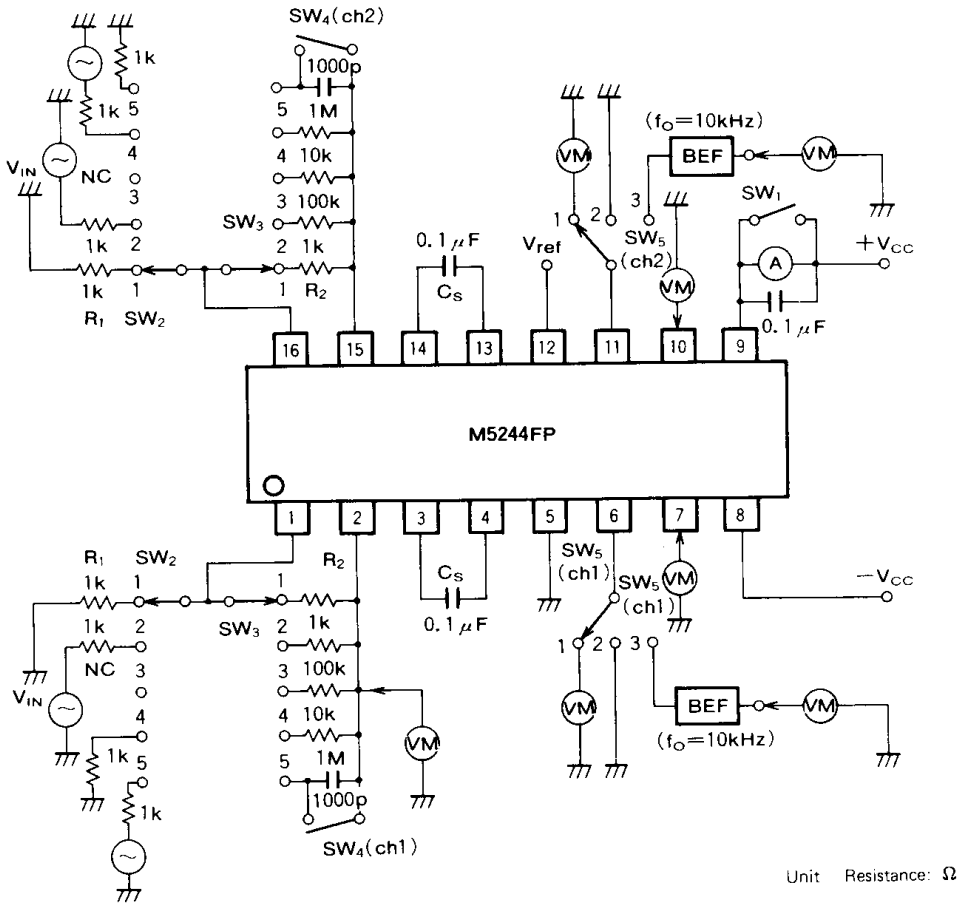
ABSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		±15(30)	V
Pd	Power dissipation		550	mW
K_θ	Thermal derating	Ta ≧ 25℃	5.5	mW/℃
Topr	Operating temperature		−20 ~ +75	℃
Tstg	Storage temperature		−55 ~ +125	℃

ELECTRICAL CHARACTERISTICS (Ta = 25℃, V_{CC} = 5V, $-V_{CC}$ = −12V, Vref = +2V, Cs = 0.1μF, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{CC}	Circuit current while no signal is present	V_I = 0		12.4	18	mA
V_{IO1}	IC1 input offset voltage			3	15	mV
G_V	Voltage gain	f = 10kHz, V_I = −60dBm R_1 = 1kΩ, R_2 = 1kΩ	57	60	63	dB
V_O	IC1 output voltage	V_I = −20dBm, f = 10kHz R_1 = 1kΩ, R_2 = 10kΩ	−1.5	0	1.5	dBm
V_{OH}	Comparator output voltage	Vref = 200mV	4.6	4.9		V
V_{OL}	Comparator output voltage	Vref = −200mV		0.02	0.2	V
V_{AOH}	Analog output voltage	f = 10kHz, V_I = −60dBm Vref = 5V, R_1 = R_2 = 1kΩ	4.6	4.9		V
V_{AOL}	Analog output voltage	f = 10kHz, V_I = −60dBm Vref = −400mV, R_1 = R_2 = 1kΩ		0.02	0.2	V
V_{NO}	Analog output noise voltage	R_1 = R_2 = 1kΩ		20	50	mVrms
t_r	Comparator output response			2		μs
V_{NC}	Comparator inversion noise	f = 10kHz, V_I = −60dBm, BEF (f_O = 10kHz)		40	100	mVrms
CS	Channel separation	f = 10kHz, V_I = −60dBm		−31	−20	dB
I_B	IC1 input bias current			0.1	10	nA
V_A	Voltage at pin A1 and A2	$V_A = I_B \times Rf + V_{IO1}$ (Rf = 1MΩ)		3.1	16	mV

TEST CIRCUIT



Unit Resistance: Ω

		SW1	SW2	SW3	SW4	SW2	VIN Voltage	Vref Voltage	Test pin	
ICC		OFF	1	1	ON	—	—	+2V	⑨	
VIO1	The same test circuit for ch1 and ch2	ON	1	2	ON	—	—	+2V	②, ⑮	
GV		ON	2	1	ON	1	−60dBm	+2V	⑥, ⑪	f=10kHz
VO		ON	2	3	ON	—	−20dBm	+2V	②, ⑮	f=10kHz
VOH		ON	3	1	ON	2	—	+200mV	⑦, ⑩	
VOL		ON	3	1	ON	2	—	+200mV	⑦, ⑩	
VAOH		ON	2	1	ON	1	−60dBm	+5V	⑦, ⑩	f=10kHz
VAOL		ON	2	1	ON	1	−60dBm	−400mV	⑦, ⑩	f=10kHz
VNO		ON	1	1	ON	1	—	+2V	⑥, ⑪	
VNO		ON	2	1	ON	3	−60dBm	+2V	⑥, ⑪	After passing the band-rejection filter
VA		ON	3	4	ON	—	—	+2V	②, ⑮	$V_A = I_B \cdot Rf + V_{IO}$
IB		ON	3	5	ON→OFF	—	—	+2V	②, ⑮	$I_B = -\frac{c}{t} \cdot V_O$
CS	ch1	ON	4	1	ON	1	−60dBm	+2V	⑥	ch1:OFF, ch2:ON
	ch2	ON	5	1	ON	1	−60dBm	+2V	⑪	ch1:ON, ch2:OFF

PRINCIPLE OF OPERATIONS

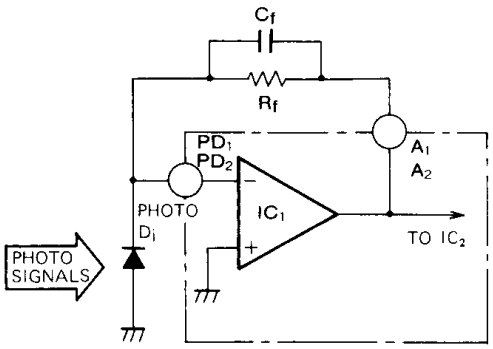
First-stage amplifier

The input part of IC_1 has the FET configuration. The photo-reception element (i.e. photo D_i) connected to PD_1 and PD_2 pins will receive photo signals as shown in the figure right. Then, the current change at the photo D_i is converted into voltage and it is supplied to the input of the second-stage amplifier.

Feedback resistor R_f, feedback capacitor C_f, and photo-reception element should be connected externally. R_f and C_f should be set to the most proper values according to the input signal level, noise level of analog output signals, and the required rising speed.

(Note)

When the input signal is very weak (that is, when the current through the photo D_i is few nA level and the R_f value is about 1MΩ), provide enough shield around PD_1 and PD_2 pins.



Second- and third-stage amplifiers

The total gain of second- and third-stage amplifiers is 60dB ± 3dB. The second-stage has a 30dB of inversion amplifier and the third-stage has a 30dB of non-inversion amplifier.

The output from the third-stage amplifier is connected to AO_1 and AO_2 pins (analog output pins) and are used as monitor output pins.

Zero compensation circuit

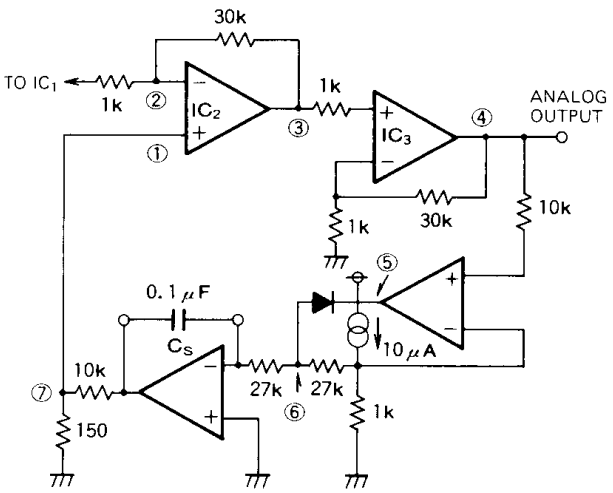
This device contains a zero compensation circuit consisting of a low level detection circuit and a DC servo circuit to cancel the DC potential such as the input offset voltage in the IC.

The feedback capacitor C_S in the DC servo circuit is connected externally and its value should be around 0.1μF. The zero compensation voltage range is internally set to ±70mA (@V_{CC} = ±5V).

The zero compensation circuit will set the analog output pin close to the GND potential level when the analog output pin has no input signal as shown in the following operational mechanism.

In the figure right if the potential difference between ① and ② of IC_2 is V_{IO}, the potential at each point forms the following loops to perform the zero compensation:

Potential at ① : 0 (V)
Potential at ② : V_{IO} (V)
Potential at ③ : V_{IO} x 30 (V)
Potential at ④ : V_{IO} x 900 (V)
Potential at ⑤ : Turns to HIGH or LOW by comparing the potential at ④ with +10mA.
Potential at ⑥ : Becomes +10mA or LOW level depending on the potential at ⑤.
Potential at ⑦ : This potential is found by dividing the HIGH or LOW level by 10k to 150Ω and it changes the potential at ①. This draws a loop which cancels the voltage difference between ① and ②.

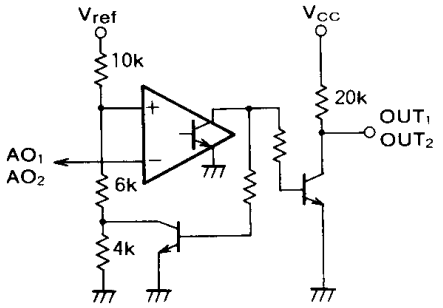


Unit Resistance: Ω

LEVEL CONTROLLER FOR PHOTO DETECTION

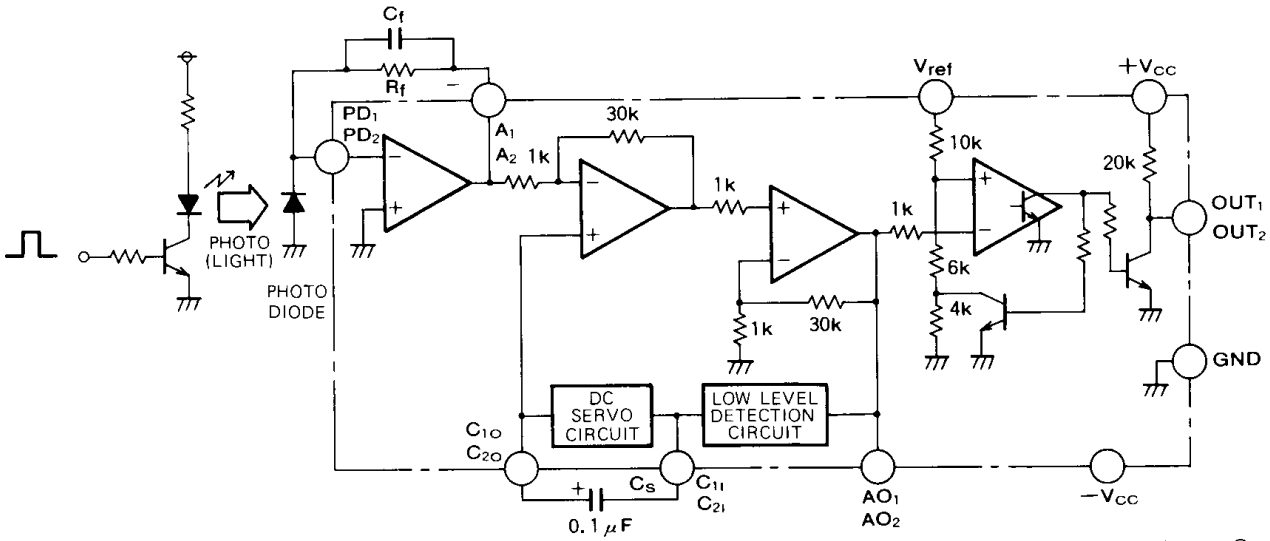
Voltage Comparator

This separates analog output signals (from AO_1 and AO_2) to HIGH ro LOW. (The comparator output turns to HIGH at the GND level.) The voltage to be compared is sent externally and divided into 1/2 to be input. This has the hysteresis characteristics and its width is 250mV (@V_{ref} = 2V).

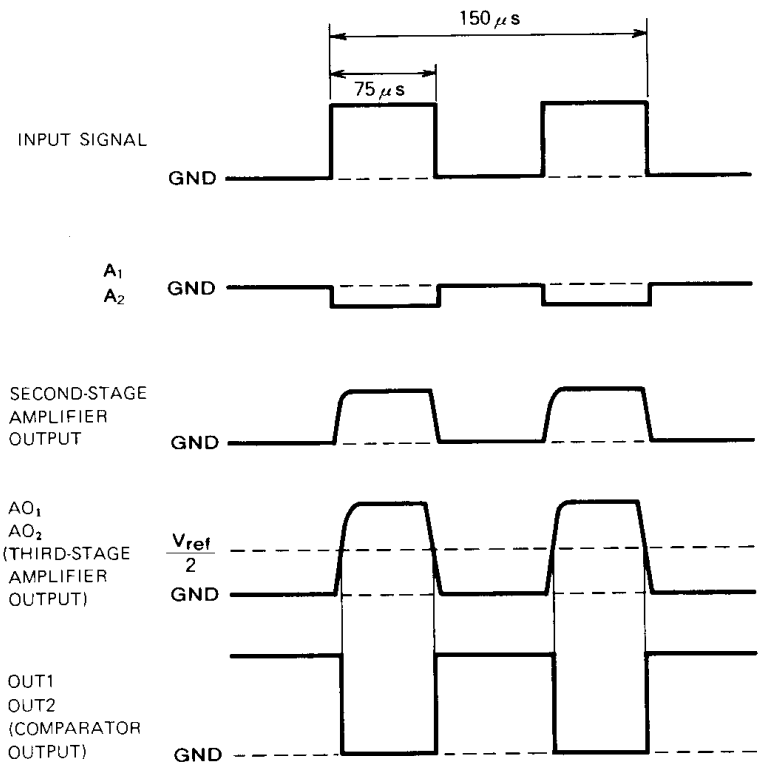


Unit Resistance: Ω

SIGNAL TRANSMISSION PATH

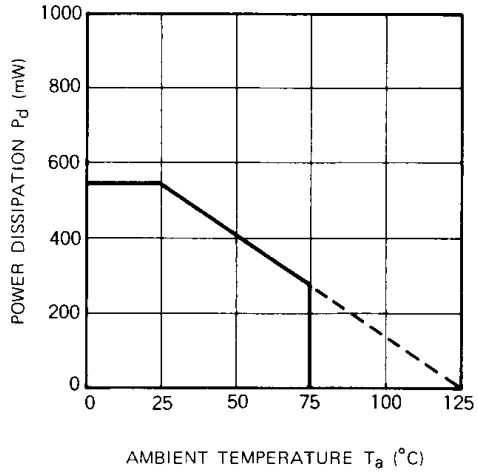


Unit Resistance: Ω

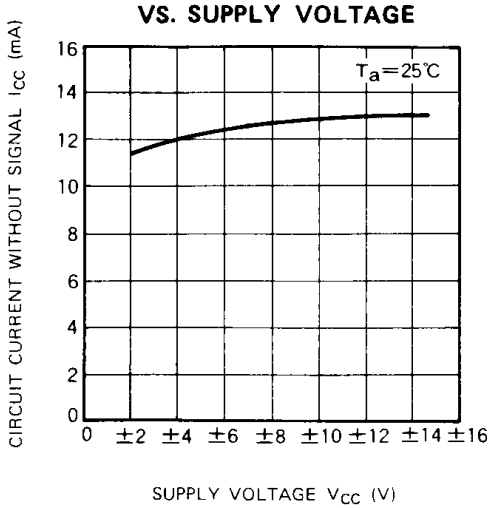


TYPICAL CHARACTERISTICS

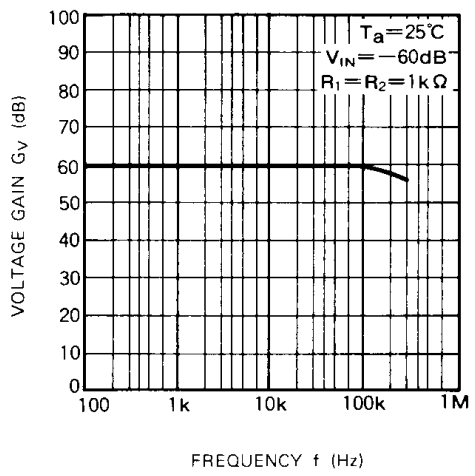
THERMAL DERATING (MAXIMUM RATING)



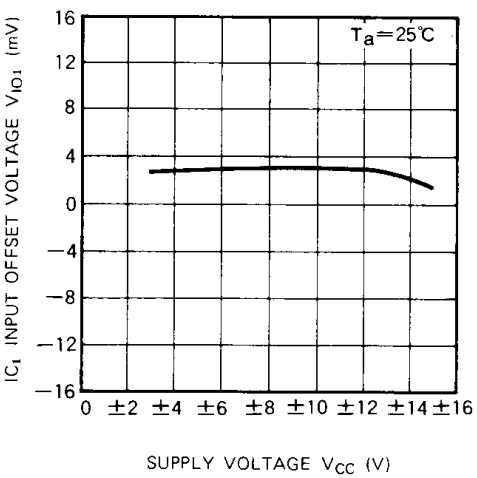
CIRCUIT CURRENT WITHOUT SIGNAL VS. SUPPLY VOLTAGE



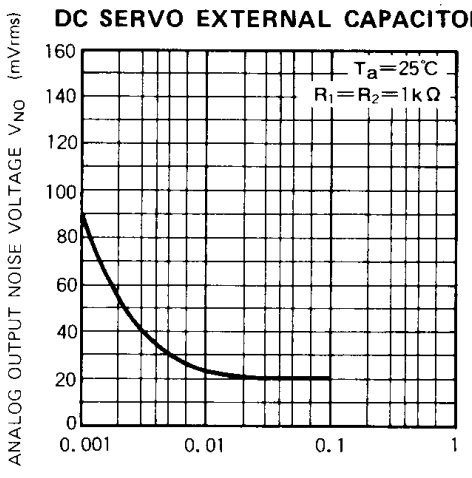
VOLTAGE GAIN VS. FREQUENCY RESPONSE



IC1 INPUT OFFSET VOLTAGE VS. SUPPLY VOLTAGE



ANALOG OUTPUT NOISE VOLTAGE VS. DC SERVO EXTERNAL CAPACITOR



COMPARATOR INVERSION NOISE VS. DC SERVO EXTERNAL CAPACITOR