SM3 Device
SONET 3:1 Mux/Demux
TXC-02201

DATA SHEET

FEATURES

- Multiplexes/demultiplexes three serial STS-1 signals from an STS-3
- Byte parallel or nibble parallel STS-3 interface
- Scrambling and B1 BIP-8 byte functions enabled with an STS-3 byte interface
- Loss of STS-3 receive detector and loss of STS-1 transmit signal detectors
- Provides reference timing for transmit timing
  -From higher order multiplexer for STS-3 nibble interface
  -From 155 MHz clock for STS-3 byte interface

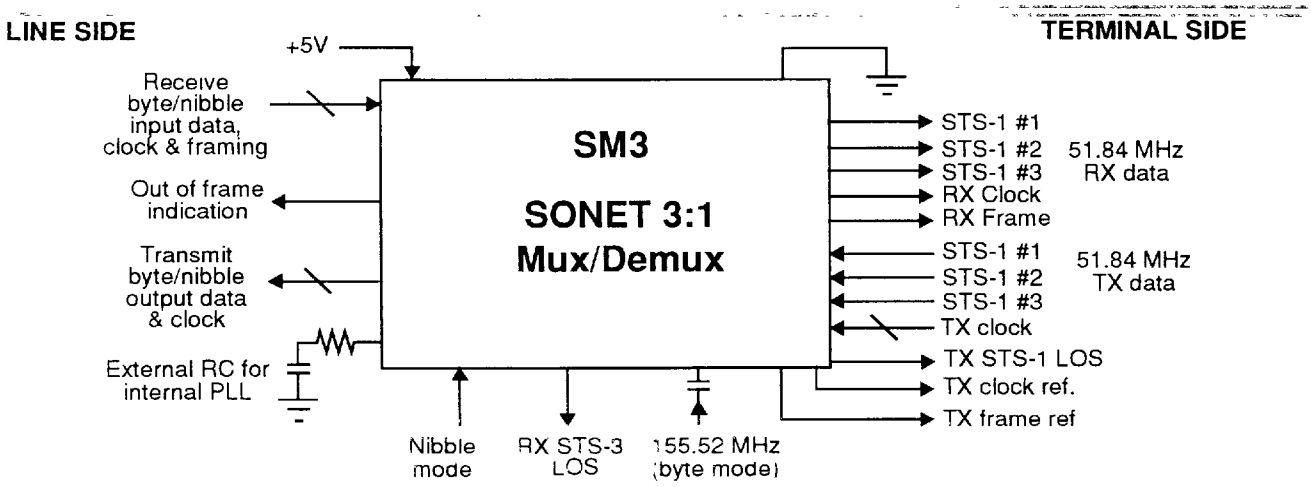
DESCRIPTION

The SM3 is a CMOS VLSI device that provides the functions needed to multiplex and demultiplex three STS-1 signals to and from an STS-3 signal. The SM3 provides either a byte parallel or nibble parallel interface on the line side. When the byte interface is selected, the SM3 performs the line signal scrambling/descrambling and the B1 generation and detection functions.

On the terminal side, the SM3 provides three serial interfaces for the STS-1 signals. Each of the serial interfaces can be directly connected to a TranSwitch SONET Overhead Terminator (SOT-1), TXC-03001, or to other transport and path overhead terminating circuitry. STS-1 transmit reference timing in the STS-3 byte interface mode is provided by using an external 155 MHz clock. For an STS-3 nibble interface, the STS-1 reference timing is provided by the SM3 from the higher order multiplexer circuits.

APPLICATIONS

- Digital cross-connects
- OC-N multiplexers
- OC-3 add/drop multiplexers
- SONET Integrated Digital Loop Carrier (IDLC)
- Test equipment



Document Number:
TXC-02201-MB
Ed. 4, April 1994

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BLOCK DIAGRAM

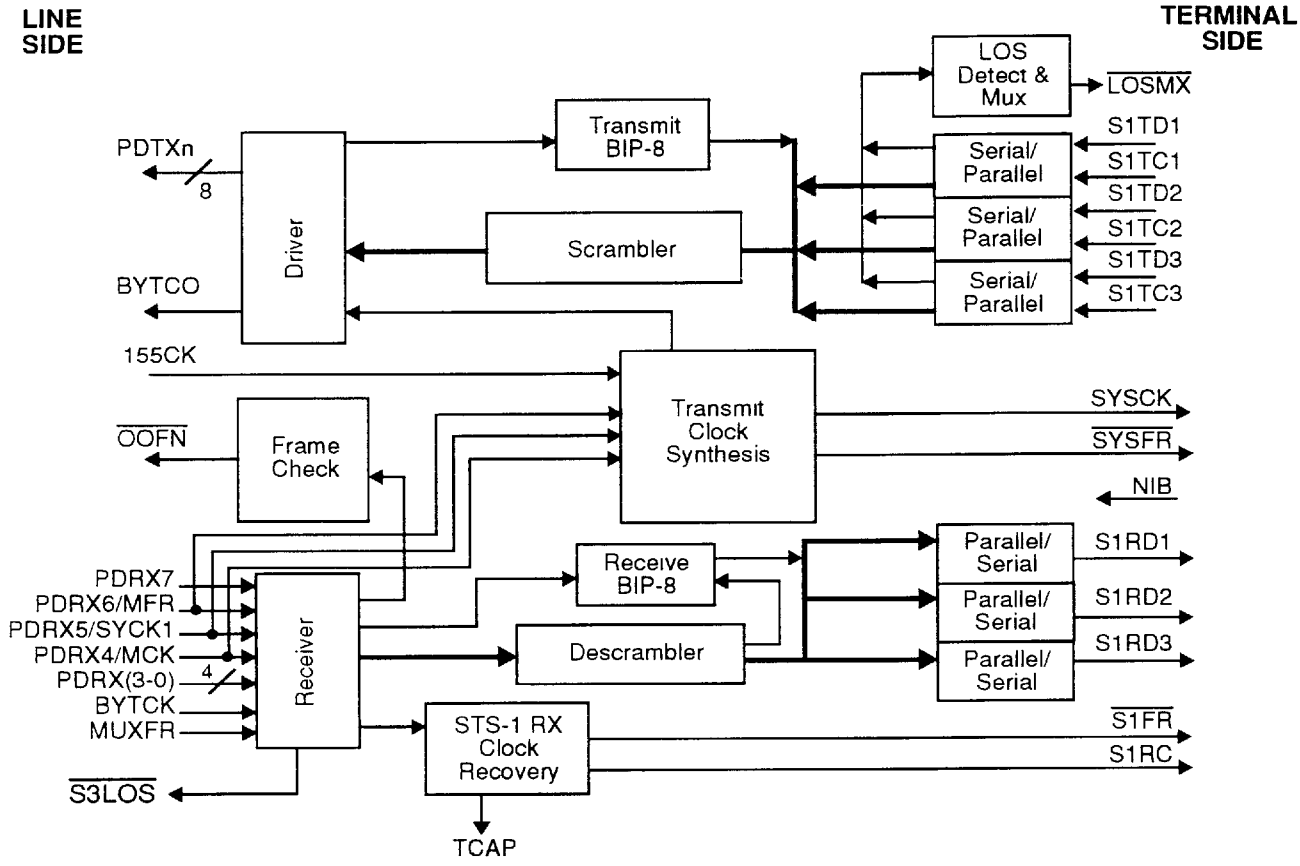


Figure 1. SM3 Block Diagram

BLOCK DIAGRAM DESCRIPTION

Figure 1 is a simplified block diagram of the SM3 and its signal leads. The Receiver Block accepts either byte or nibble parallel data. Byte wide receive data, (PDRX7-0), is clocked into the SM3 on positive transitions of the clock (BYTCK). The most significant bit, which is the first bit received, corresponds to PDRX7. The positive framing pulse, one clock cycle wide, indicates the last A2 byte, and is used by the SM3 for frame alignment. The SM3 monitors the receive signal and provides an STS-3 loss of signal ($\overline{S3LOS}$) alarm indication when the incoming data or clock is stuck high or low. The byte/nibble data is converted to serial data prior to the loss of signal detector. When the byte interface is selected, the SM3 performs the scrambling/descrambling and B1 BIP-8 generation/detection functions.

When the nibble (NIB) control lead is an active high, the SM3 receiver interfaces to nibble-wide data, PDRX3-0. The nibble parallel interface is intended for higher order multiplexer systems, such as OC-12 systems. Nibble wide data is clocked into the SM3 on positive transitions of the clock signal (BYTCK). The most significant bit, which is the first bit received, corresponds to PDRX3. When the nibble interface is selected, the scrambler/descrambler and B1 generator/detector functions are disabled. It is assumed that the higher order multiplexer circuits will perform those functions. The PDRX7 lead must be grounded, and the PDRX(6-4) leads perform other functions. The PDRX6 lead is used to input a framing pulse (MFR), the PDRX5 lead is used to input an STS-1 reference clock (SYCK1), and the PDRX4 lead is used to input a clock signal (MCK).

The SM3 converts the STS-3 byte wide parallel descrambled data or nibble wide parallel data into three STS-1 signals (S1RD1, S1RD2, and S1RD3). Data (S1RD1, S1RD2, and S1RD3) is clocked out of the SM3 on positive transitions of the common clock signal (S1RC). The data present on the S1RD1 signal corresponds to STS-1 No. 1 in the STS-3 signal. The 51.84 MHz STS-1 serial clock (S1RC) is derived from the incoming 19.44 Mbyte/s byte clock (BYTCK), or from the 38.88 Mbyte/s nibble clock (BYTCK) by the Clock Recovery Block.

In the transmit direction, three STS-1 signals (S1TD1, S1TD2, and S1TD3) are clocked into the SM3 on the positive transitions of their associated clock signals (S1TC1, S1TC2, and S1TC3). In the nibble mode, the clock signal (MCK), framing pulse (MFR), and STS-1 reference clock signal (SYCK1) are reference signals generated by the higher order multiplexer circuit. They are used by the Transmit Clock Synthesis Block for generating a synchronous STS-1 transmit line reference clock signal (SYSCK), and a framing pulse ($\overline{\text{SYSFR}}$) for the TranSwitch SOT-1 or other STS-1 circuitry. The SOT-1 uses the SM3 generated STS-1 clock signal (SYSCK) and framing pulse ($\overline{\text{SYSFR}}$) for synchronizing the STS-1 frame. The clock signal (MCK) and framing pulse (MFR) are also used to generate a synchronous nibble clock (BYTCO).

For the byte-parallel interface (a low on the NIB control lead), the STS-1 reference clock (SYSCK), reference framing pulse ($\overline{\text{SYSFR}}$), and STS-3 byte clock (BYTCO) are synthesized from the 155.52 MHz clock signal (155CK).

Each of the three transmit STS-1 signals is monitored for loss of signal. A common multiplexed signal lead ($\overline{\text{LOSMX}}$) is used to indicate a loss of signal for any of the three STS-1 signals. The SM3 multiplexes the three STS-1 signals to form the STS-3 signal. The STS-3 signal interface is either nibble wide, PDTX(7-4), or byte-wide, PDTX(7-0). The most significant bit and the first bit transmitted corresponds to PDTX7. Parallel data is clocked out of the SM3 on positive transitions of the clock (BYTCO).

A conceptual view of multiplexing/demultiplexing three STS-1 signals to and from an STS-3 signal is shown in Figure 2. An STS-1 signal has a structure that consists of 90 columns by nine rows for a total of 810 bytes. The frame rate is 125 microseconds (i.e., 8000 frames per second) which corresponds to a bit rate of 51.84 Mbit/s or 64 kbit/s per byte. The first three columns by nine rows are assigned for transport overhead. The remaining 87 columns and nine rows are assigned for the STS-1 payload. The frame is transmitted row by row, starting with the framing bytes A1 and A2.

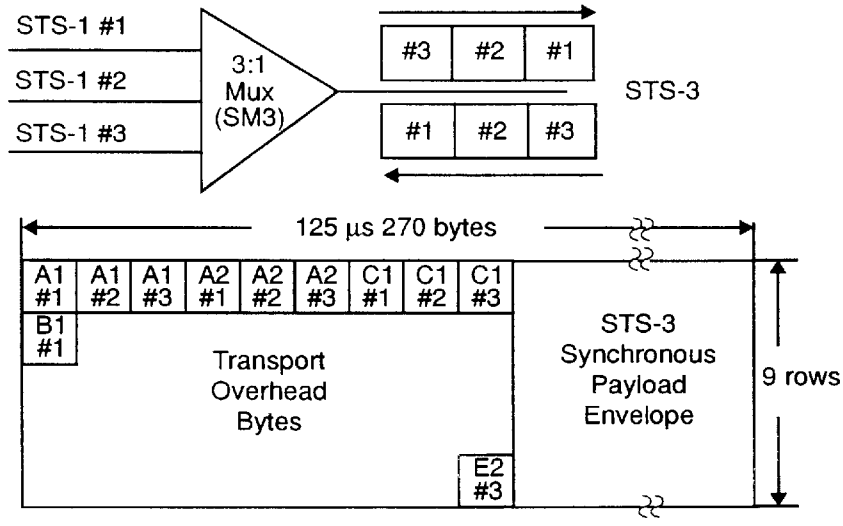


Figure 2. STS-3 Format

In an STS-3 signal, there are three times as many bytes assigned for a 125 microsecond frame which corresponds to a bit rate of 155.52 Mbit/s. An STS-3 frame consists of 270 columns by nine rows for a total of 2430 bytes. The transport overhead bytes in the STS-3 signal are assigned to the first nine columns by nine rows (counting left to right). This accommodates the three columns assigned as transport overhead bytes in each of the STS-1 signals. The bytes from each of the three STS-1 signals are interleaved into the STS-3 signal as shown in Figure 2. The first row consists of the framing pattern A1 STS-1 No. 1, A1 STS-1 No. 2, A1 STS-1 No. 3, A2 STS-1 No. 1, etc.

The order of transmission of the bytes in the frame is row by row, from left to right, starting with row 1. Thus, the framing pattern formed is F6F6F6282828 Hex. In an STS-3 signal, not all of the STS-1 transport overhead bytes are assigned for use. Table 1 summarizes the transport overhead bytes that are required in each of the STS-1 signals when they are multiplexed into an STS-3 signal. An X in the table indicates that the byte is assigned, while a dash indicates that it is unused. The contents of an unused byte carries the value of zero. The STS-1 C1 byte carries the binary number corresponding to its order of appearance in the STS-3 signal. If the STS-3 signal is converted to an OC-3 signal, all of the bytes in the signal, except the six A1 and A2 framing bytes and three C1 bytes, are scrambled, and a BIP-8 is calculated and inserted into the STS-1 No. 1 B1 byte. The remaining bytes (2349 bytes) are assigned to carry the STS-1 payloads. Since each of the STS-1 frames has a unique payload pointer to indicate the location of the SPE in the frame, the associated SPEs do not require them to be aligned.

Table 1. STS-3 Byte Assignment

Byte	STS#1	#2	#3
A1,A2	X	X	X
C1	X	X	X
B1	X	--	--
E1	X	--	--
F1	X	--	--
D1-D3	X	--	--
H1-H3	X	X	X
B2	X	X	X
K1,K2	X	--	--
D4-D12	X	--	--
Z1-Z3	X	X	X
E2	X	--	--

PIN DIAGRAM

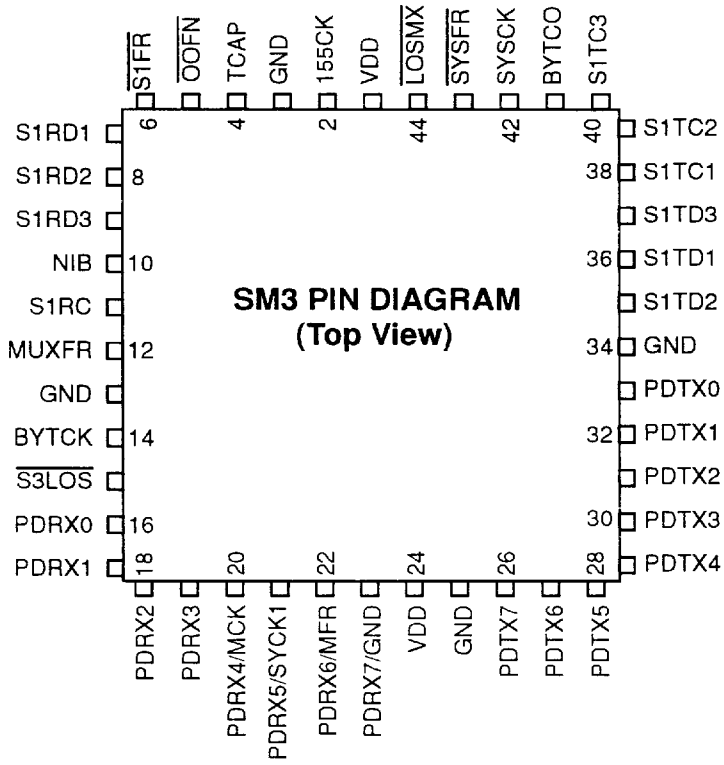


Figure 3. SM3 Pin Diagram with Numbers and Names

PIN DESCRIPTIONS

Power Supply and Ground

Symbol	Pin No.	I/O/P*	Type	Name/Function
VDD	1,24	P		**VDD:** 5-volt supply, +/-5%.
GND	3,13,25,34	P		**Ground:** 0 volts reference.

*Note: I = Input; O = Output; P = Power

STS-3 Receive and Transmit Interface

Symbol	Pin No.	I/O/P	Type	Name/Function
MUXFR	12	I	TTL	**Receive Multiplexer Framing Pulse:** A 125 micro-second framing pulse that must be synchronous with the STS-1 No. 3 A2 byte or the last A2 nibble. The positive framing pulse determines the location of the first C1 byte and is used for STS-3 frame alignment.

Symbol	Pin No.	I/O/P	Type	Name/Function
BYTCK	14	I	TTL	**STS-3 Receive Byte/Nibble Clock:** The clock rate for clocking byte data into the SM3 is 19.44 MHz, while the clock rate for clocking nibble data into the SM3 is 38.88 MHz. Receive byte or nibble parallel data is clocked into the SM3 on positive transitions of this clock.
PDRX7/ GND PDRX6/ MFR PDRX5/ SYCK1 PDRX4/ MCK PDRX3-0	23 22 21 20 19-16	I	TTL	**STS-3 Receive Byte/Nibble Data (PDRX7-0):** Byte and nibble wide data is clocked into the SM3 on positive transitions of the clock (BYTCK). PDRX7 corresponds to the most significant bit in the byte and the first bit received. For nibble operation, the most significant bit is PDRX3, and the PDRX7 bit must be held low. **Nibble Framing Pulse (MFR):** In the nibble mode, the framing pulse is used to establish a reference for outputting the next STS-3 frame. The MFR pulse is clocked into the SM3 on positive transitions of the clock (MCK). Sixteen clock cycles later, the first nibble in the next STS-3 (first four bits of byte A1 No. 1) is clocked out of the SM3. In addition, the MFR pulse is used to generate the STS-1 transmit framing reference pulse ($\overline{SYSFR}$). **STS-1 Reference Clock (SYCK1):** The 51.84 MHz reference input clock is used to generate the STS-1 transmit reference clock (SYSCK). **Nibble Reference Clock (MCK):** A 38.88 MHz nibble reference clock that is used to generate the transmit nibble clock (BYTCO).
PDTX(7-0)	26-33	O	TTL4mA	**STS-3 Transmit Byte/Nibble Data:** Byte and nibble wide data is clocked out of the SM3 on positive transitions of the clock (BYTCO). PDTX7 corresponds to the most significant bit in the byte and the first bit transmitted. For nibble operation, signal leads PDTX(7-4) are used to transmit the nibble. The most significant bit for the nibble is PDTX7. Bits PDTX(3-0) are disabled in the nibble interface mode.
BYTCO	41	O	TTL4mA	**STS-3 Transmit Byte/Nibble Clock:** Transmit byte or nibble parallel data is clocked out of the SM3 on positive transitions of this clock. For the STS-3 nibble interface, this clock is derived from the nibble clock reference signal (MCK). For the STS-3 byte interface, this clock is derived from the 155.52 transmit reference clock (155CK).

STS-1 Transmit Interfaces

Symbol	Pin No.	I/O/P	Type	Name/Function
S1TD1	36	I	TTL	**STS-1 Transmit Data:** The 51.84 Mbit/s serial signal corresponding to STS-1 No. 1 is connected to this lead. Data is clocked into the SM3 on positive transitions of the STS-1 clock signal (S1TC1).
S1TD2	35	I	TTL	**STS-1 Transmit Data:** The serial 51.84 Mbit/s signal corresponding to STS-1 No. 2 is connected to this lead. Data is clocked into the SM3 on positive transitions of the STS-1 clock signal (S1TC2).
S1TD3	37	I	TTL	**STS-1 Transmit Data:** The serial 51.84 Mbit/s signal corresponding to STS-1 No. 3 is connected to this lead. Data is clocked into the SM3 on positive transitions of the STS-1 clock signal (S1TC3).
S1TC1	38	I	TTL	**STS-1 Transmit Clock:** The clock corresponding to the STS-1 No. 1 signal is connected to this lead. When the SM3 is connected to a TranSwitch SOT-1, a common reference STS-1 clock (SYSCK) and framing pulse ($\overline{\text{SYSFR}}$) are provided by the SM3 for deriving this clock.
S1TC2	39	I	TTL	**STS-1 Transmit Clock:** The clock corresponding to the STS-1 No. 2 signal is connected to this lead. When the SM3 is connected to a TranSwitch SOT-1, a common reference STS-1 clock (SYSCK) and framing pulse ($\overline{\text{SYSFR}}$) are provided by the SM3 for deriving this clock.
S1TC3	40	I	TTL	**STS-1 Transmit Clock:** The clock corresponding to the STS-1 No. 3 signal is connected to this lead. When the SM3 is connected to a TranSwitch SOT-1, a common reference STS-1 clock (SYSCK) and framing pulse ($\overline{\text{SYSFR}}$) are provided by the SM3 for deriving this clock.
SYSCK	42	O	TTL12mA	**STS-1 Reference Clock:** A 51.84 MHz clock provided by the SM3 for STS-1 transmit retiming, and for clocking out data from the three TranSwitch SOT-1s or other circuitry. In the nibble mode, the reference clock (SYSCK) and framing pulse ($\overline{\text{SYSFR}}$) are derived from the STS-1 clock (SYCK1) and framing pulse (MFR). In the byte mode, the reference clock (SYSCK) and framing pulse ($\overline{\text{SYSFR}}$) are derived from the 155.52 MHz transmit clock (155CK).

Symbol	Pin No.	I/O/P	Type	Name/Function
$\overline{\text{SYSFR}}$	43	O	TTL12mA	**STS-1 Reference Framing Pulse:** An active low, one clock wide framing pulse that is provided by the SM3 for frame synchronization of the STS-1 signals in the TranSwitch SOT-1 devices or other circuitry. The reference framing pulse occurs once every 125 microseconds. The SM3 must receive each new STS-1 frame within five to seven clock cycles (SYSCK) to be considered valid.
155CK	2	I		**155 MHz Transmit Reference Clock:** This clock is used in the STS-3 byte interface mode for generating the STS-1 transmit reference clock (SYSCK) and framing pulse ($\overline{\text{SYSFR}}$), and the STS-3 clock signal (BYTCO). The 155 MHz clock is not required by the SM3 for the STS-3 nibble interface. The signal may be sine-like in shape but must be at least 1.5V peak-to-peak and AC-coupled with a 56 pF capacitor.

STS-1 Receive Interfaces

Symbol	Pin No.	I/O/P	Type	Name/Function
$\overline{\text{S1FR}}$	6	O	TTL12mA	**STS-1 Framing Pulse:** An active low, one clock cycle wide framing pulse is provided for STS-1 frame synchronization for the TranSwitch SOT-1 or other circuitry. The frame pulse is common for all three STS-1 signals, and is synchronous with the first bit of C1.
S1RD1	7	O	TTL4mA	**STS-1 Receive Data:** The 51.84 Mbit/s serial signal corresponding to STS-1 No. 1 is provided on this lead. Data is clocked out of the SM3 on positive transitions of the STS-1 clock signal (S1RC). B1 error indications in the STS-3 byte interface mode are provided in the corresponding bit position of the B1 byte.
S1RD2	8	O	TTL4mA	**STS-1 Receive Data:** The 51.84 Mbit/s serial signal corresponding to STS-1 No. 2 is provided on this lead. Data is clocked out of the SM3 on positive transitions of the STS-1 clock signal (S1RC).
S1RD3	9	O	TTL4mA	**STS-1 Receive Data:** The 51.84 Mbit/s serial signal corresponding to STS-1 No. 3 is provided on this lead. Data is clocked out of the SM3 on positive transitions of the STS-1 clock signal (S1RC).
S1RC	11	O	TTL12mA	**STS-1 Receive Clock:** A 51.84 MHz clock that is common to all three STS-1 signals. The STS-1 clock is derived from the STS-3 signal using an internal clock recovery circuit.

Control Leads

Symbol	Pin No.	I/O/P	Type	Name/Function
NIB	10	I	TTLr	**Nibble Interface:** When an active high is placed on the NIB control lead, the SM3 STS-3 line side is a nibble interface. In the nibble mode, the STS-1 transmit reference clock signal (SYSCK) and framing pulse ($\overline{\text{SYSFR}}$) are derived from the 51.84 MHz input STS-1 clock signal (SYCK1) and input framing pulse (MFR). The reference 38.88 MHz clock signal (MCK) and input framing pulse (MFR) are also used to generate the transmit nibble clock signal (BYTCO), and timing for the STS-3 signal. The B1 generator/detector and scrambler/descrambler functions are disabled in the nibble mode. When a low is placed on the NIB lead, the STS-3 line side is byte interface. The STS-1 reference clock (SYSCK) and framing pulse ($\overline{\text{SYSFR}}$), and the STS-3 transmit byte clock (BYTCO) are derived from the 155 MHz reference clock (155CK). The scrambler/descrambler and B1 generator/detector are enabled when the byte interface is selected.

Alarm Leads

Symbol	Pin No.	I/O/P	Type	Name/Function
$\overline{\text{OOFN}}$	5	O	TTL4mA	**Out of Frame Alarm:** An active low STS-3 out of frame alarm occurs when four or more consecutive errored framing patterns are received. Recovery occurs when two successive error free framing patterns are received.
$\overline{\text{S3LOS}}$	15	O	TTL4mA	**STS-3 Loss of Signal:** An active low STS-3 loss of signal alarm occurs when the byte wide data (PDRXn) is stuck high or low for 270 bytes (one row) or 13 microseconds. For the STS-3 nibble interface, the STS-3 loss of signal alarm occurs if the receive nibble wide data (PDRXn) is stuck high or low for 4860 nibbles (nine rows) or 125 microseconds. In addition, an alarm occurs if the receive STS-3 clock (BYTCK) is stuck high or low for 270 clock cycles or approximately 13 microseconds. Recovery occurs when the SM3 detects valid byte data for 125 microseconds, valid nibble data for 250 microseconds, or a clock signal for 125 microseconds.

Symbol	Pin No.	I/O/P	Type	Name/Function
$\overline{\text{LOSMX}}$	44	O	TTL4mA	**Loss of Signal Multiplexed STS-1 Signals:** An active low loss of signal indication occurs for a data signal (S1TDn) if it is lost (stuck high or low) for 125 microseconds or more. The alarm indication is provided on a multiplexed loss of signal ($\overline{\text{LOSMX}}$) signal lead. Each STS-1 loss of signal indication is two clock cycles (385.8 nanoseconds) long and repeats as an active low pulse. The STS-1 No. 1 signal is synchronized with the positive transition of the framing pulse ($\overline{\text{SYSFR}}$). Recovery occurs when the SM3 detects a valid STS-1 signal for 250 microseconds.

Pins With External Components

Symbol	Pin No.	I/O/P	Type	Name/Function
TCAP	4			**External RC:** An external series RC network is connected to this pin. A 1000 picofarad ±10% and a 1.2K ohm ±5% resistor are required.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	-0.3	7.0	V
DC input voltage	V_{IN}	-0.5	V_{DD} + 0.5	V
Continuous power dissipation	P_C		1000	mW
Ambient operating temperature	T_A	-40	85	°C
Operating junction temperature	T_J		150	°C
Storage temperature range	T_S	-55	150	°C

*Note: Operating conditions exceeding those listed in Absolute Maximum Ratings may cause permanent failure. Exposure to absolute maximum ratings for extended periods may impair device reliability.

THERMAL CHARACTERISTICS

Parameter	Min	Typ	Max	Unit	Test Conditions
Thermal Resistance: Junction to Ambient			46	°C/W	

POWER REQUIREMENTS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	4.75	5.0	5.25	V	
I_{DD}			150	mA	V_{DD} = 5.25V
P_{DD}			790	mW	V_{DD} = 5.25V

INPUT, OUTPUT, AND I/O PARAMETERS

Input Parameters For TTL

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current			10	µA	$V_{DD} = 5.25$
Input capacitance		5.5		pF	

Input Parameters For TTLr

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current		50	120	µA	$V_{DD} = 5.25$
Input capacitance		5.5		pF	

Note: Input has a 100K (nominal) internal pull-up resistor.

Output Parameters For TTL4mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	V_{DD} - 0.5			V	$V_{DD} = 4.75$; $I_{OH} = -2.0$ mA
V_{OL}			0.4	V	$V_{DD} = 4.75$; $I_{OL} = 4.0$ mA
I_{OL}			4.0	mA	
I_{OH}			-2.0	mA	
t_{RISE}	2.8	6.5	9.2	ns	$C_{LOAD} = 15$ pF
t_{FALL}	1.3	2.3	3.4	ns	$C_{LOAD} = 15$ pF

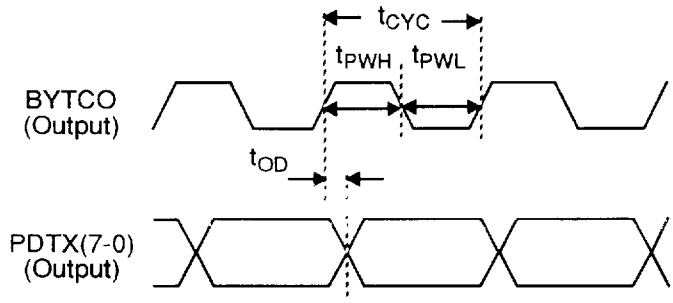
Output Parameters For TTL12mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	V_{DD} - 0.5			V	$V_{DD} = 4.75$; $I_{OH} = -6.0$ mA
V_{OL}			0.4	V	$V_{DD} = 4.75$; $I_{OL} = 12.0$ mA
I_{OL}			12.0	mA	
I_{OH}			-6.0	mA	
t_{RISE}	1.7	3.3	4.8	ns	$C_{LOAD} = 25$ pF
t_{FALL}	0.9	1.3	1.7	ns	$C_{LOAD} = 25$ pF

TIMING CHARACTERISTICS

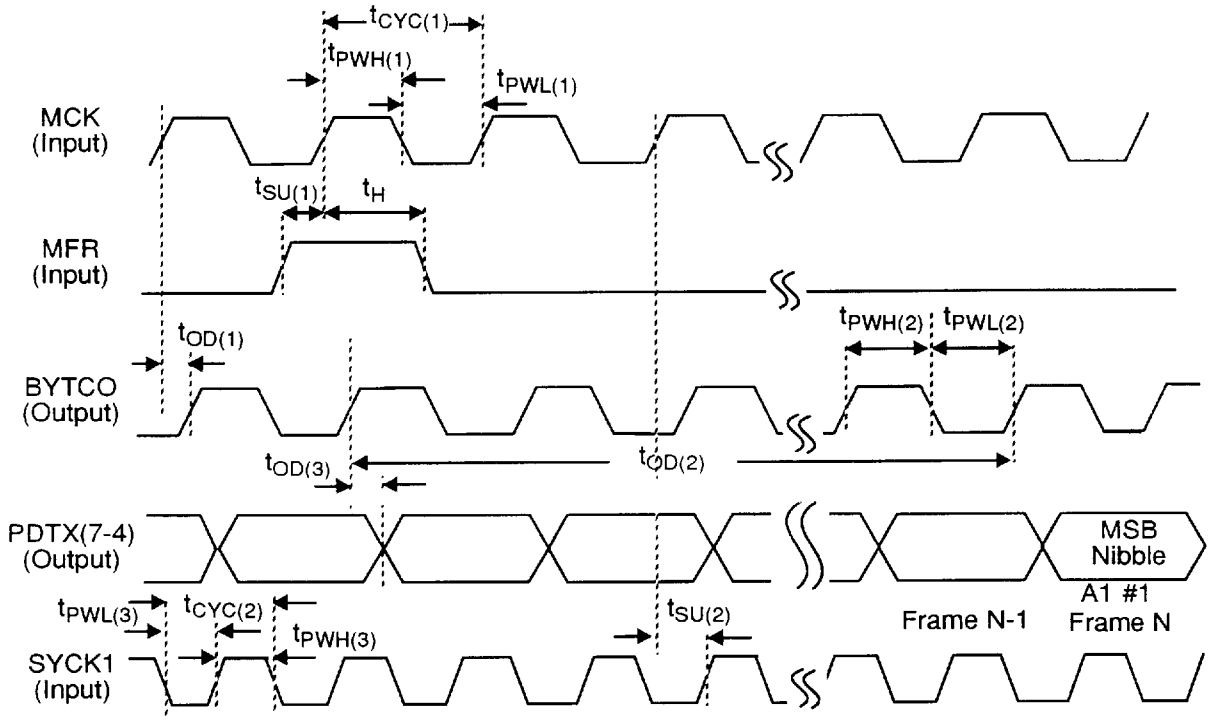
Detailed timing diagrams for the SM3 are illustrated in Figures 4 through 9. All output times are measured with 25 pF load capacitance except STSCK, $\overline{\text{SYSFR}}$, S1RC, and $\overline{\text{S1RF}}$ which are measured with 75 pF load capacitance. Timing parameters are measured at 1.4V.

Figure 4. STS-3 Byte Transmit Timing



Parameter	Symbol	Min	Typ	Max	Unit
BYTCO clock period	t_{CYC}	51.4			ns
BYTCO high time	t_{PWH}	TBD			ns
BYTCO low time	t_{PWL}	TBD			ns
PDTX output delay after BYTCO↑	t_{OD}	3		11	ns

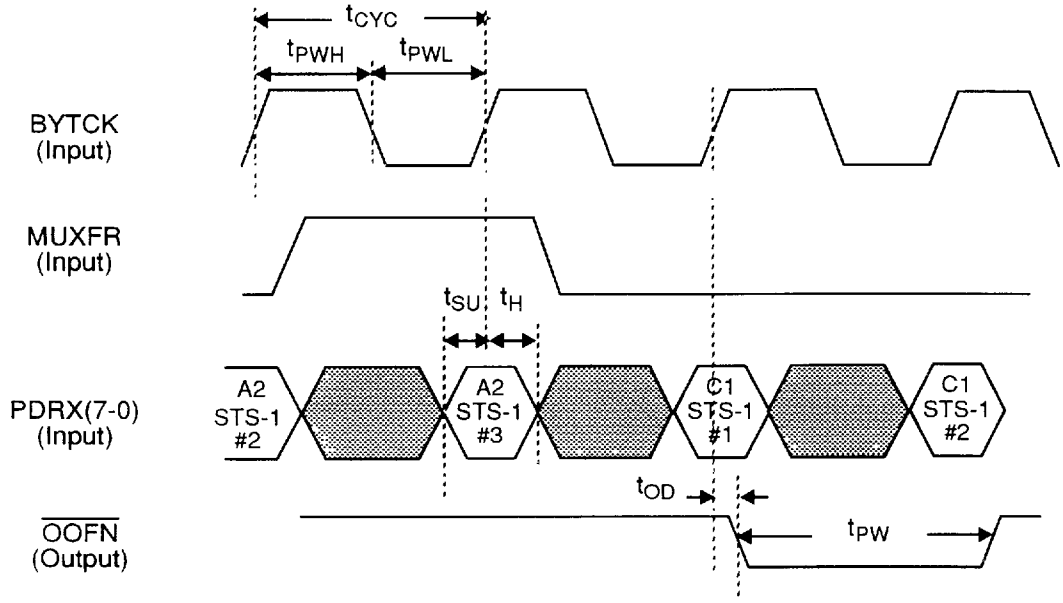
Figure 5. STS-3 Nibble Transmit Timing



Parameter	Symbol	Min	Typ	Max	Unit
MCK clock period	$t_{CYC(1)}$	25.7			ns
MCK high time	$t_{PWH(1)}$	TBD			ns
MCK low time	$t_{PWL(1)}$	TBD			ns
MFR set-up time to MCK↑	$t_{SU(1)}$	5			ns
MFR hold time after MCK↑	t_H	3			ns
BYTCO output delay after MCK↑	$t_{OD(1)}$	4		16	ns
BYTCO new frame output delay after MFR clocked in on MCK↑	$t_{OD(2)}$		16 $t_{CYC(1)}$		ns
BYTCO high time (MCK duty = 50%)	$t_{PWH(2)}$	TBD			ns
BYTCO low time (MCK duty = 50%)	$t_{PWL(2)}$	TBD			ns
PDTX output delay after BYTCO↑	$t_{OD(3)}$	5		18.5	ns
SYCK1 clock period	$t_{CYC(2)}$	19.3			ns
SYCK1 high time	$t_{PWH(3)}$	TBD			ns
SYCK1 low time	$t_{PWL(3)}$	TBD			ns
MCK set-up to SYCK1↑*	$t_{SU(2)}$	-5		5	ns

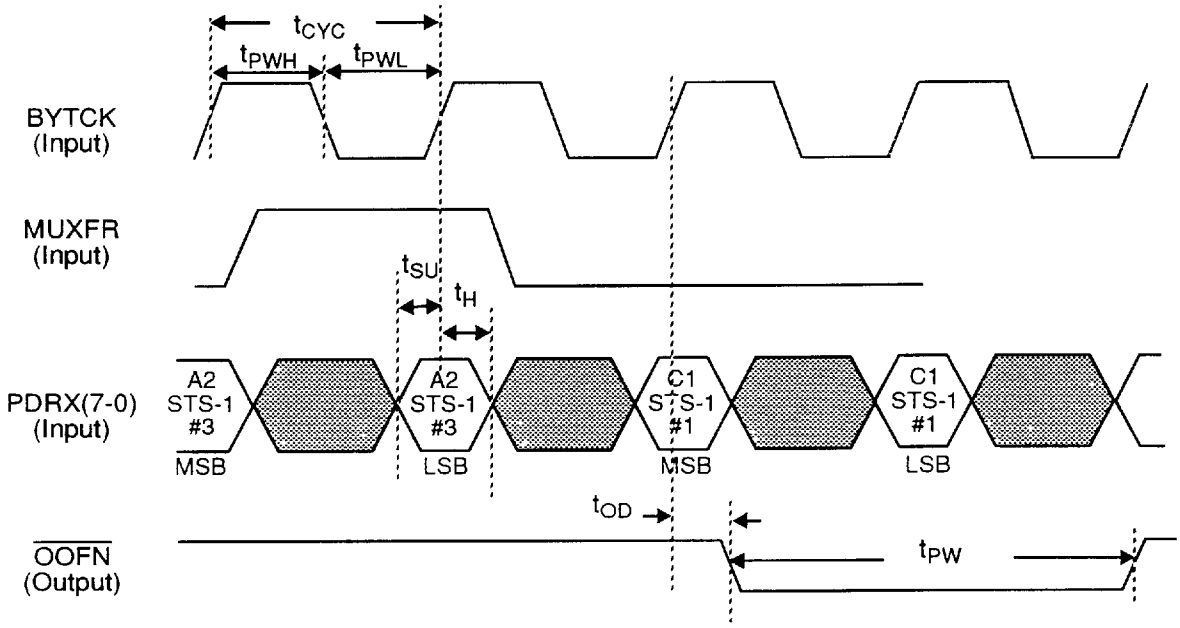
*Second MCK↑ after edge which clocks in MFR.

Figure 6. STS-3 Byte Receive Timing



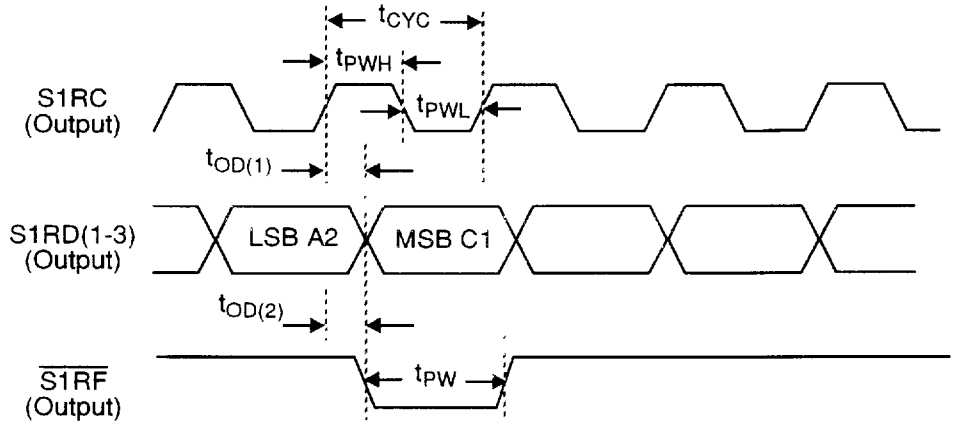
Parameter	Symbol	Min	Typ	Max	Unit
BYTCK clock period	t_{CYC}	51.4			ns
BYTCK high time	t_{PWH}	TBD			ns
BYTCK low time	t_{PWL}	TBD			ns
PDRX set-up time to BYTCK↑	t_{SU}	7			ns
PDRX hold time after BYTCK↑	t_H	3			ns
$\overline{\text{OOFN}}$ output delay after BYTCK↑	t_{OD}	TBD		TBD	ns
$\overline{\text{OOFN}}$ pulse width	t_{PW}		t_{CYC}		ns

Figure 7. STS-3 Nibble Receive Timing



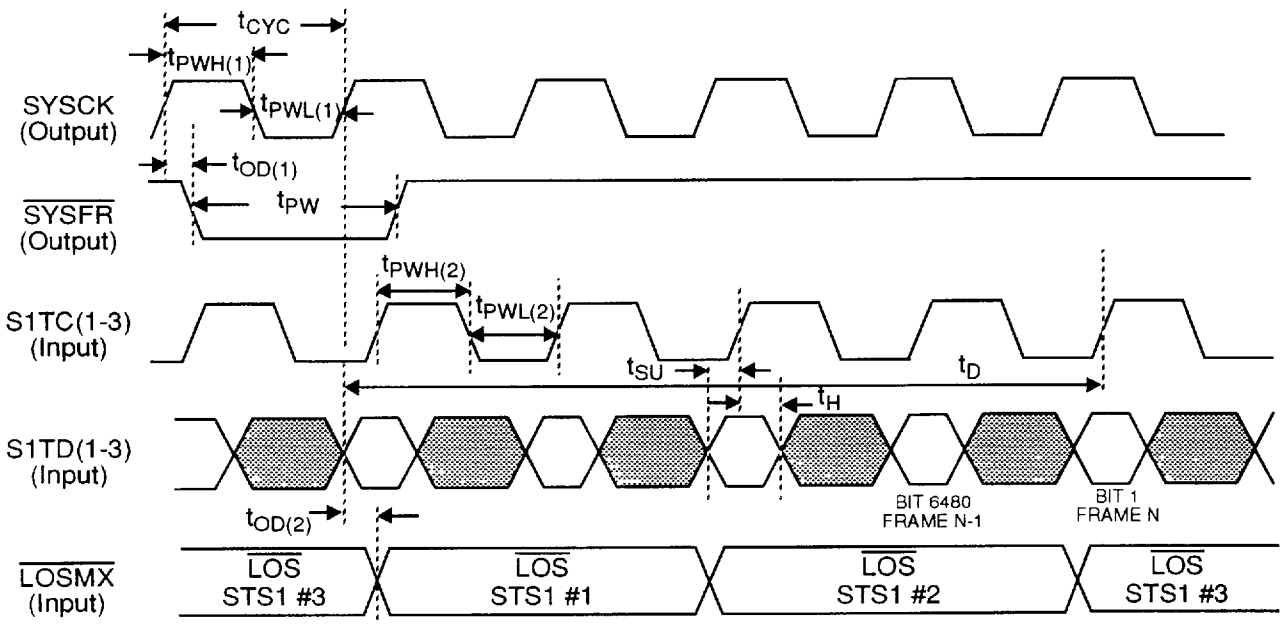
Parameter	Symbol	Min	Typ	Max	Unit
BYTCK clock period	t_{CYC}	25.7			ns
BYTCK high time	t_{PWH}	TBD			ns
BYTCK low time	t_{PWL}	TBD			ns
PDRX set-up time to BYTCK↑	t_{SU}	5			ns
PDRX hold time after BYTCK↑	t_H	3			ns
$\overline{\text{OOFN}}$ output delay after BYTCK↑	t_{OD}	TBD		TBD	ns
$\overline{\text{OOFN}}$ pulse width	t_{PW}		2 t_{CYC}		ns

Figure 8. STS-1 Receive Timing



Parameter	Symbol	Min	Typ	Max	Unit
S1RC clock period	t_{CYC}		19.3		ns
S1RC high time	t_{PWH}	TBD			ns
S1RC low time	t_{PWL}	TBD			ns
S1RD output delay after S1RC↑	$t_{OD(1)}$	TBD		11.5	ns
$\overline{\text{S1RF}}$ output delay after S1RC↑	$t_{OD(2)}$	TBD		11.5	ns
$\overline{\text{S1RF}}$ pulse width	t_{PW}		t_{CYC}		ns

Figure 9. STS-1 Transmit Timing



Parameter	Symbol	Min	Typ	Max	Unit
SYSCK clock period	t_{CYC}		19.3		ns
SYSCK high time (SYSCK 50% duty cycle in NIB)	$t_{PWH(1)}$	TBD			ns
SYSCK low time (SYSCK 50% duty cycle in NIB)	$t_{PWL(1)}$	TBD			ns
$\overline{\text{SYSFR}}$ output delay after SYSCK↑	$t_{OD(1)}$	4		11	ns
$\overline{\text{SYSFR}}$ pulse width	t_{PW}		t_{CYC}		ns
S1TC high time	$t_{PWH(2)}$	TBD			ns
S1TC low time	$t_{PWL(2)}$	TBD			ns
S1TD set-up time to S1TC↑	t_{SU}	5			ns
S1TD hold time after S1TC↑	t_H	2			ns
$\overline{\text{LOSMX}}$ output delay after SYSCK↑	$t_{OD(2)}$	4		12.5	ns
S1TCn and bit 1 input delay after SYSCK↑ and $\overline{\text{SYSFR}}$↓	t_D	5 t_{CYC}		7 t_{CYC} + 10	ns

*Note: t_D may be different for each S1TC.

OPERATION

INTRODUCING BIP-8 B1 TRANSMIT PARITY ERRORS

BIP-8 B1 transmit parity errors in the outgoing STS-3 transmit signals for system and network testing can be intentionally inserted.

The error introduction is accomplished by forcing one or more bits in the STS-1 No. 1 B1 input byte to one (S1TD1). The SM3 calculates and introduces an incorrect parity bit in the corresponding B1 bit position of the transmitted STS-3 signal. Alternately, for each input STS-1 B1 bit in the logical zero state, the corresponding B1 bit in the STS-3 transmitted signal will be correct.

The feature is disabled whenever the SM3 detects a loss of STS-1 No. 1 input signal (S1TD1) or a loss of STS-1 No. 1 input clock (S1TC1).

In the receive direction, B1 bit errors are provided in the receive STS-1 No. 1 signal (S1RD1).

INTERFACES

Terminal Side Interface

The interface connections between an SM3 and one of three TranSwitch SONET Overhead Terminators (SOT-1s) are shown in Figure 10. The SOT-1 multiplexes and demultiplexes the path, line, and section overhead bytes to and from the STS-1 signal and provides interfaces for the two data communication channels, order-wire and APS channels, and either a parallel or serial interface for accessing the payload. The receive interface between the SM3 and SOT-1s consists of three bit-serial STS-1 data signals (S1RDn), a common framing pulse ($\overline{S1RF}$), and a common clock signal (S1RC). Data (S1RDn) is clocked out of the SM3 on positive transitions of the clock signal (S1RC) and into the SOT-1 also on positive transitions of the clock. The framing pulse ($\overline{S1RF}$) defines the start of the C1 byte in the STS-1 signal.

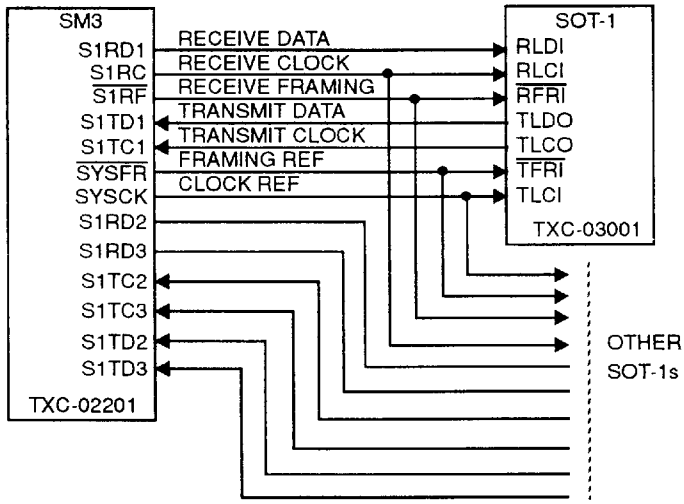


Figure 10. SM3/SOT-1 Interface

In the transmit direction, the SM3 provides an STS-1 transmit line reference clock signal (SYSCK) and a framing pulse ($\overline{SYSFR}$) for the SOT-1 or other circuitry. The reference clock signal and framing pulse are used by each of the SOT-1s to output the data signal (TLDO) and clock signal (TLCO) to the SM3 (S1TDn and S1TCn). The framing pulse defines the start of the STS-1 frame. The SM3 uses the framing pulse and transmitted framing pattern to multiplex the three STS-1 signals to form the STS-3 signal.

Line Side Interface

Figure 11 shows the interface connections between the SM3 and a TranSwitch STS-3/STM-1 Synchronizer (SYN155). Byte wide data (PDTX7-0) is clocked out of the SM3 on positive transitions of the clock (BYTCO). Data is clocked into the SYN155 on negative transitions of the clock (BYTCO). Bit 7 in the data byte is the most significant bit and is the first bit transmitted in an STS-3 signal. Received byte wide data (PDRX7-0) is clocked into the SM3 on positive transitions of the input clock (BYTCK). The input framing pulse (MUXFR) occurs during the STS-1 No. 3 A2 byte time slot.

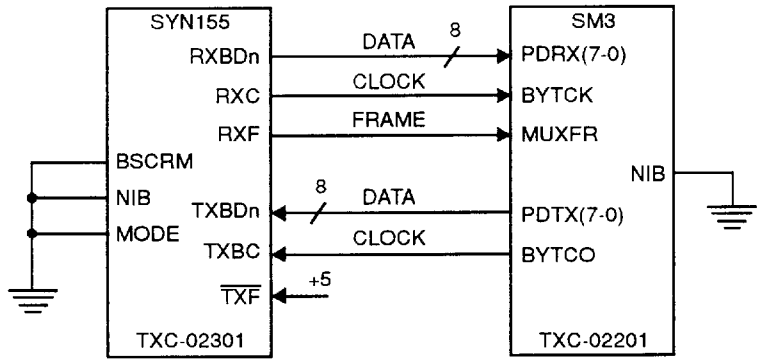


Figure 11. SM3/SYN155 Interface

The SM3 performs the SONET scrambling/descrambling and B1 generation/detection functions, while the SYN155 operates in the full tracking mode. In the full tracking mode, the SYN155 searches for the occurrence of the SONET STS-3 framing pattern (F6F6F6282828) and then verifies that is true by looking for it to repeat exactly one frame later. The RXF frame indication pulse occurs only after the frame pattern has been verified. The data is held low prior to verification. In the transmit direction, the SM3 provides byte data (19.44 Mbytes/s) and a clock signal to the SYN155.

The SYN155 also performs loss of frame detection. A loss of frame alarm (LOF) occurs if the out of frame condition persists for 3 milliseconds (24 frames). The loss of frame alarm is exited when eight consecutive correct framing patterns are detected, after the out of frame is exited.

Clock Interface

Figure 12 shows an oscillator circuit used as a system clock. This clock drives the SM3, TranSwitch's STS-3/STM-1 synchronizer (SYN155), and other circuitry as required. The SM3 requires the 155 MHz clock for the STS-3 byte interface only. The clock signal is pseudo-ECL and consists of a true and complement signal. A pseudo-ECL signal operates between +5 volts and ground.

The oscillator circuit shown in Figure 12 is modified for pseudo-ECL operation by using +5 volts and ground. A Conner-Winfield E01-453 155.52 MHz or equivalent oscillator may be used. The output of the oscillator is connected to an F100115 device, which is a low skew quad clock driver. True and complementary output signals

are provided. Each of the true and complement clock signals must be terminated with a Thevenin equivalent of approximately 50 ohms. The termination should be placed as close as possible to the differential pair transistors (2N3906). True and complement traces should be approximately the same length.

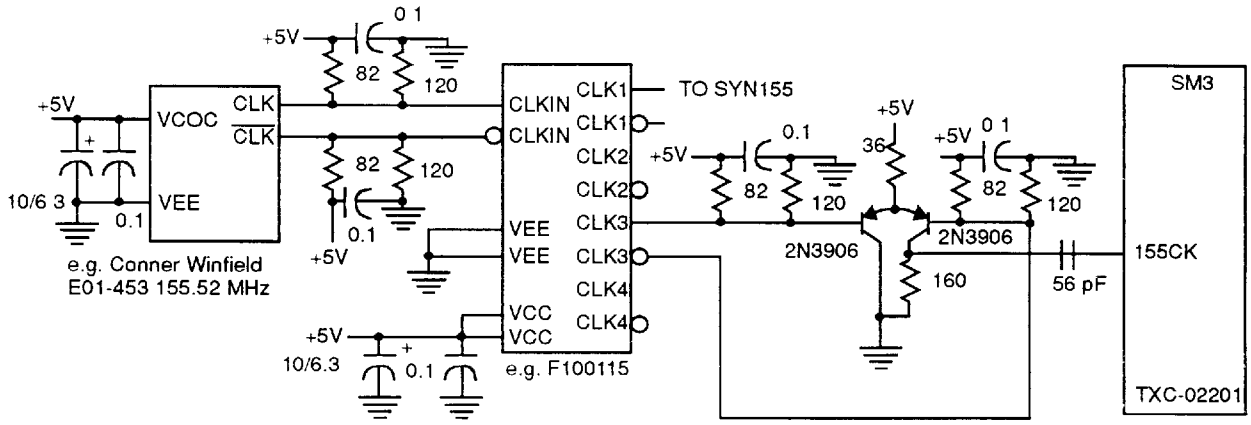


Figure 12. SM3 Clock Interface

Reference Signals

In higher order multiplexer systems such as an OC-12 system, the transmit timing required for multiplexing four STS-3 signals into an STS-12 signal is simplified by using transmit reference signals. Figure 13 shows the reference signals and transmit signals for an OC-12 system using four TranSwitch SM3s and 12 SOT-1s. The reference signals generated by the 4:1 multiplexer are a multiplexed framing pulse (MFR) that has a 125 microsecond rate, a multiplexed clock signal (MCK) that has a nibble rate of 38.88 MHz, and a 51.84 MHz STS-1 clock signal (SYCK1). They are derived from a 155.52 MHz clock signal. These signals are connected to the SM3s, and each SM3 is connected to three SOT-1s. The interface between the 4:1 multiplexer and an SM3 uses the nibble format. The scrambling/descrambling and B1 parity generation/detection for the STS-12 signal is performed in the 4:1 multiplexer.

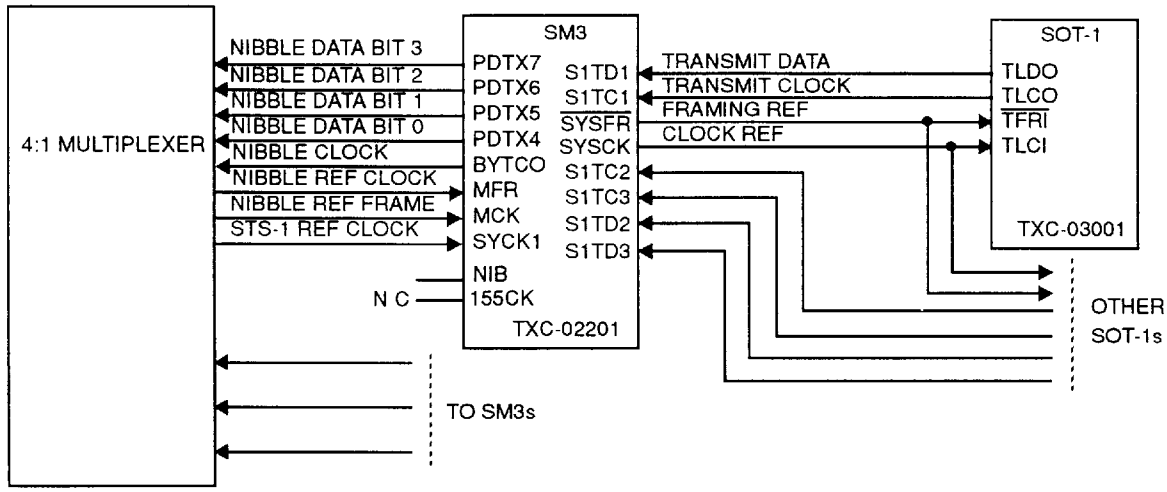


Figure 13. OC-12 Reference Timing Interface

The 4:1 multiplexer reference signals are connected to an internal reference generator within the SM3 which is used to generate an STS-1 transmit line reference clock signal (SYSCK) and a framing pulse ($\overline{SYSFR}$) for each of the SOT-1s. The SOT-1 uses the clock (SYSCK) and the framing pulse ($\overline{SYSFR}$) to clock out the serial data at 51.84 Mbit/s from the SOT-1 to the SM3. The SM3 multiplexes the three STS-1 serial bit streams into a nibble wide STS-3 signal at a 38.88 Mbit/s rate. The clock signal (MCK) and framing pulse (MFR) from the 4:1 multiplexer is also used to output nibble wide data (PDTX7-4) and defines the start of the new frame.

DESIGN CONSIDERATIONS

Because of the operating frequencies of 51.84 and 155.52 MHz, careful attention must be paid to the power supply and grounding arrangements, clock distribution, and signal interconnections between the SM3 and other devices.

TranSwitch recommends that each of the SM3 power supply connections have a decoupling capacitor. All 0.1 µF decoupling capacitors must be of good quality and high frequency, and be low lead inductance ceramic capacitors. The decoupling capacitors should be as physically close to the devices as possible. If low frequency noise is present on the +5 volt supply lead, TranSwitch recommends that an additional 10 microfarad, 6.3 volt tantalum capacitor be connected between +5 volts and ground. A multilayer board that has separate planes for ground and power is recommended.

Clock distribution at 51.84 MHz and 155.52 MHz can also be a problem. Individual clock buffers in the form of a tree are recommended for distributing the clock signals. To minimize crosstalk, unused buffers in the devices used to distribute the clock should not be used with other system signals.

System lines should be kept as short as possible to minimize ringing, over/undershoots, and to simplify timing because of propagation delays.

PACKAGE INFORMATION

The SM3 is available in a 44-pin plastic leaded chip carrier as illustrated below. All dimensions shown are in inches.

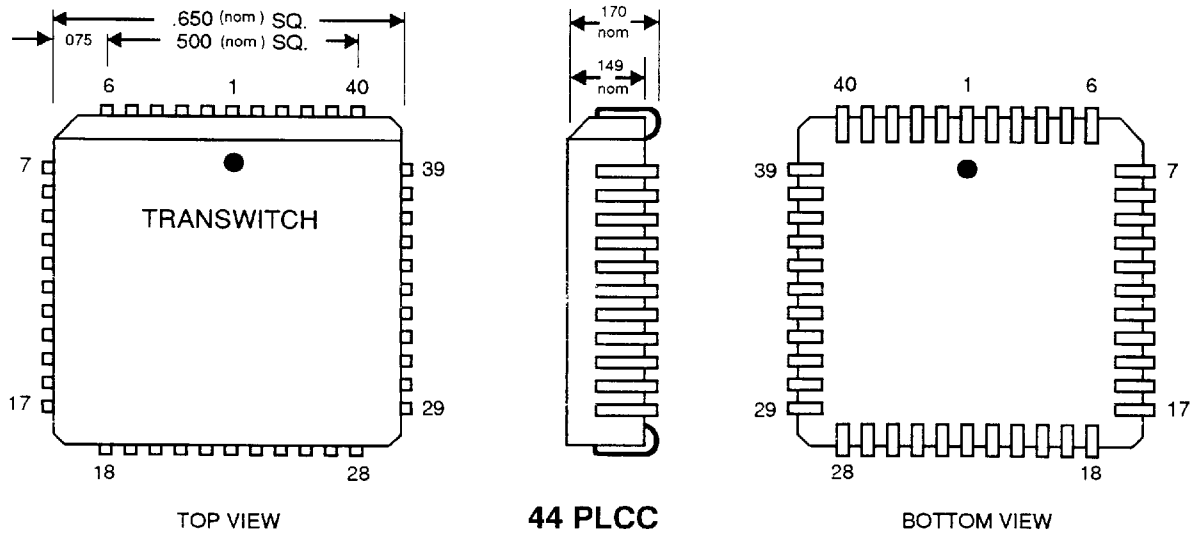


Figure 14. SM3 44-Pin Plastic Leaded Chip Carrier

ORDERING INFORMATION

Part Number: TXC-02001-BIPL 44-pin Plastic Leaded Chip Carrier

RELATED PRODUCTS

TXC-02301, SYN155 VLSI Device. Provides the features of converting STS-3 byte-parallel data to a serial 155 Mbit/s bit stream.

TXC-03001, SOT-1 (SONET Overhead Terminator) VLSI Device. Provides the multiplexing/ demultiplexing of transport and path overhead bytes from the STS-1 signal in a single chip.

STANDARDS DOCUMENTATION SOURCES

Telecommunication technical standards and reference documentation may be obtained from the following organizations:

ANSI (U.S.A.):

American National Standards Institute (ANSI)
11 West 42nd Street
New York, New York 10036

Tel: 212-642-4900
Fax: 212-302-1286

Bellcore (U.S.A.):

Bellcore
Attention - Customer Service
8 Corporate Place
Piscataway, NJ 08854

Tel: 800-521-CORE (In U.S.A.)
Tel: 908-699-5800
Fax: 908-336-2559

CCITT:

Publication Services of ITU
Place des Nations
CH 1211
Geneve 20, Switzerland

Tel: 41-22-730-5285
Fax: 41-22-730-5991

TTC (Japan):

TTC Standard Publishing Group of the
Telecommunications Technology Committee
2nd Floor, Hamamatsucho - Suzuki Building,
1 2-11, Hamamatsu-cho, Minato-ku, Tokyo

Tel: 81-3-3432-1551
Fax: 81-3-3432-1553

LIST OF DATA SHEET CHANGES

This change list identifies those areas within the updated SM3 Data Sheet that have technical differences relative to the superseded SM3 Data Sheet:

Updated SM3 Data Sheet:	Edition 4, April 1994
Superseded SM3 Data Sheet:	Edition 3B, November 1990

The page numbers indicated below of the updated data sheet include changes relative to the superseded data sheet.

Page Number of Updated Data Sheet	Summary of the Change
All	Changed edition number and date on all pages.
2-4	Expanded Block Diagram Description.
5-10	Expanded Pin Descriptions.
12	Added I/O Parameter tables.
13-18	Enhanced Figures 4 through 9.
19-22	Added Operation section.
23	Deleted Ceramic Package.
24	Added Related Products.
25	Added Standards Documentation Sources.