FAIRCHILD SEMICONDUCTOR®

PRELIMINARY
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ACE1202R
Data Encryption Standard (DES) Receiver

General Description

The ACE1202R is a custom receiver implementing the DES algorithm. The receiver is used to decrypt a pulse-width modulated (PWM) encrypted signal transmitted by a radio frequency (RF) transmitter using the ACE1202T[1]. Together, the ACE1202R and ACE1202T form an encoder/decoder chip-set used in high security applications.

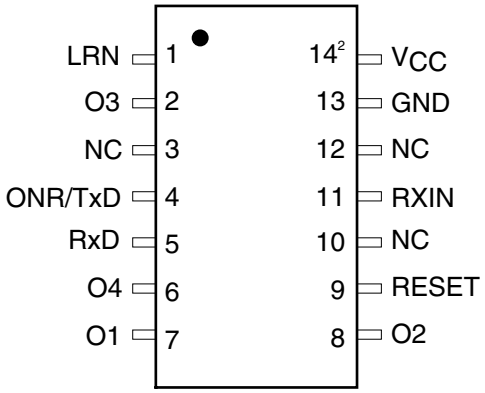
- Remote Keyless Entry
- Burglar alarms / Garage door openers
- Individualized recognition / transmission systems.
- Game protection

The ACE1202R is a member of the ACE1202 (Arithmetic Controller Engine) family of microcontrollers. The ACE1202 product family is a dedicated programmable monolithic integrated circuit for applications requiring high performance, low power, and small size. It is a fully static part fabricated using CMOS technology. For additional information regarding the ACE1202 family of microcontrollers please refer Fairchild Semiconductor's web site at www.fairchildsemi.com.

Features

- 32-bit DES Decoder
- Receiver Switched Power mode
- Up to 4 output channels
- Pulsed outputs
- RF Module switched V_{CC}
- Single supply operation (2.2 – 5.5V)
- Low Power Halt Mode (100nA @ 3.3V)
- Integrated Power-on Reset
- Brown-out Reset
- Integrated RC oscillator
- Integrated EEPROM
  - 64 byte of data EEPROM for data storage and options
  - 2K bytes of code EEPROM
  - 40 years data retention
  - 1,000,000 data writes
- 14-pin SOIC package

ACE1202REM Device Pin-out



[1] See the ACE1202T datasheet at www.fairchildsemi.com for details.

[2] Pin 14 must be de-coupled with a 100nF ceramic capacitor to GND.

2.0 Pin Description

2.1 LRN – Pin1

The LRN pin is an active low input with an internal weak pull-up and is used to disable the Learning code feature on the ACE1202R. If the Learning code feature is not needed, the LRN pin may be left unconnected avoiding the use of an external pull-up resister since it exists internally.

The Learning code feature is activated by applying a logic '0' to the LRN pin. This then disables the ACE1202R from receiving the DES and Counter Synchronization frames.

The LRN pin can also used to enter the programming mode if the ForceProgr flag in the OPTION register is set. (See Section 11.0)

2.2 O1 to O4 – Pins 7, 8, 2 and 6

These output pins are activated, according with the value received in Data Field, upon reception of a valid NORMAL frame (Fix and DES code must match internal memory). The outputs can be programmed to behave in three different modes:

1) Stable Output Levels (direct or inverted)

2) Pulsed (direct or inverted) with programmable pulse duration

3) Output Toggle: Active output change state every valid frame received (direct or inverted)

See Section 8.4 and 8.8.

2.3 ONR/TxD – Pin 4

The ONR/TxD pin is a multiplexed output used in both the PWM and NRZ modes.

In the PWM mode, the ONR/TxD pin assumes the ONR (Turn ON Receiver) function. The ONR pin option is used to wakeup the external RF module in order to save current consumption in the entire system. (See Section 9.0 for further information regarding the PWM mode.)

In NRZ mode, the ONR/TxD pin assumes the TxD function. The TxD pin option is used to transmit information to an external unit (PC or ACE1202T) in the NRZ format. (See Section 11.0 for further information regarding the NRZ mode.)

2.4 RxD – Pin 5

In NRZ mode, the RxD pin is an input accepting serial data transmitted by the PC or the ACE1202T. The RxD pin is not used in the PWM mode and can be left floating.

2.5 RXIN – Pin 11

In PWM mode, the RXIN pin is the receiving input line from the external RF module expecting only active high data. The RXIN pin is not used while in the NRZ mode and can be left floating.

2.6 RESET – Pin 9

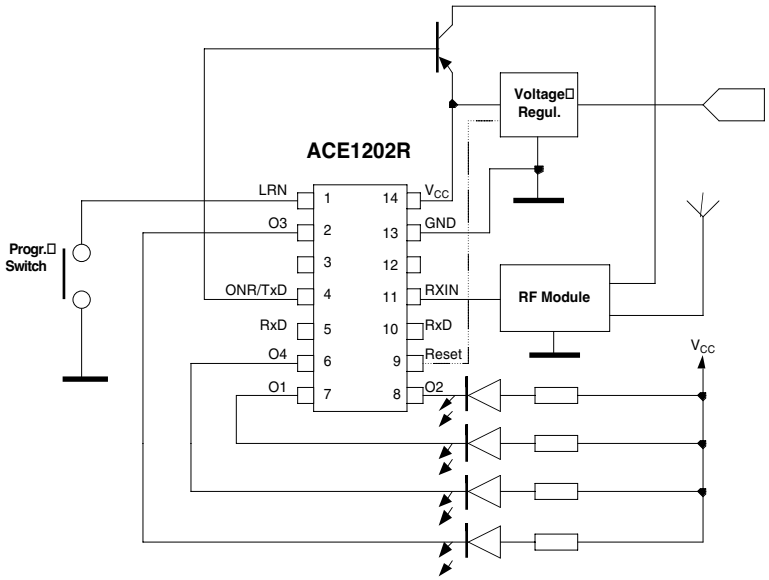
The RESET pin is an active low input and is used to externally reset the ACE1202R. However, since the ACE1202R has an internal Power-on Reset (POR) circuit the RESET pin may not be needed. In this case, the RESET pin may be left floating or connected to V_{CC}.

Before using the internal POR, the V_{CC} rise time condition must be met. (See Section 15.0)

2.7 V_{CC} and GND – Pins: 14 and 13

Vcc and GND are the power supply lines. The ACE1202R is designed to work with a 3.3V or a 5.0V supply voltage.

Figure 2. Receiver Block Diagram



3.0 Electrical Characteristics

Absolute Maximum Ratings

Ambient Storage Temperature	-65°C to +150°C
Input Voltage	-0.3V to V_{CC}+0.3V
Lead Temperature (10s max)	+300°C
Electrostatic Discharge on all pins	2000V

Operating Conditions

Ambient Operating Temperatures:	
ACE1202REM	-40°C to +85°C
Operating Supply Voltage:	
From -40ºC to +85ºC	2.2V to 5.5V
Relative Humidity (non-condensing)	95%
EEPROM write limits	See DC Electrical Characteristics

Preliminary ACE1202REM DC Electrical Characteristics for V_{CC} = 2.2 to 5.5V

All measurements are valid for ambient operating temperature range unless otherwise stated.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
I_{CC}[3]	Supply Current - no data EEPROM write in progress	2.2V 2.7V 3.3V 5.5V		0.4 0.7 1.3 3.6	1.0 1.2 1.5 4.5	mA mA mA mA
I_{CCH}	HALT Mode Current	3.3V @ -40°C to 25°C 5.5V @ -40°C to 25°C 3.3V @ +85°C 5.5 @ +85°C		10 60 75 400	100 1000 1000 2500	nA nA nA nA
I_{CCL}[4]	IDLE Mode Current	3.3V 5.5V		150 200		µA µA
V_{CCW}	EEPROM Write Voltage	Data EEPROM in Operating Mode	2.4		5.5	V
S_{VCC}	Power Supply Slope		1µs/V		10ms/V	
V_{IL}	Input High with Schmitt Trigger buffer	V_{CC} = 2.2 - 5.5V			0.2V_{CC}	V
V_{IH}	Input High withi Schmitt Trigger buffer	V_{CC} = 2..2 - 5.5V	0.8V_{CC}			V
I_{IP}	Input Pull-up Current	V_{CC} = 5.5V, V_{IN} = 0V	30	65	350	µA
I_{TL}	Tri-State Leakage	V_{CC} = 5.5V		2	200	nA
V_{OL}	Output Low Voltage:	V_{CC} = 2.2V				
	O1, O2, O3, ONR	2.0 mA sink			0.2V_{CC}	V
	O4	4.0 mA sink			0.2V_{CC}	V
	Output Low Voltage:	V_{CC} = 2.7V				
	O1, O2, O3, ONR	3.0 mA sink			0.2V_{CC}	V
	O4	5.0 mA sink			0.2V_{CC}	V
	Output Low Voltage:	V_{CC} = 3.3 - 5.5V				
	O1, O2, O3, ONR	5.0 mA sink			0.2V_{CC}	V
	O4	10.0 mA sink			0.2V_{CC}	V
V_{OH}	Output High Voltage:	V_{CC} = 2.2V				
	O1, O2, O3, ONR	0.4 mA source	0.8V_{CC}			V
	O4	0.8 mA source	0.8V_{CC}			V
	Output High Voltage:	V_{CC} = 2.7V				
	O1, O2, O3, ONR	0.4 mA source	0.8V_{CC}			V
	O4	0.8 mA source	0.8V_{CC}			V
	Output High Voltage:	V_{CC} = 3.3 - 5.5V				
	O1, O2, O3, ONR	0.4 mA source	0.8V_{CC}			V
	O4	1.0 mA source	0.8V_{CC}			V

[3] For I_{CC} Active data with EEPROM writes see Figure 5.

[4] IDLE current is base on a continuous looping program. The true IDLE current is dependent on the specific application and the value stored in the RXAWAKE register. See Section 9.0 for details.

Preliminary ACE1202REM AC Electrical Characteristics for V_{CC} = 2.2 to 5.5V

All measurements are valid for ambient operating temperature range unless otherwise stated.

Parameter	Conditions	MIN	TYP	MAX	Unit
Instruction cycle time from internal clock - setpoint	5.0C at + 25°C	0.9	1.0	1.1	µs
Internal cycle voltage dependent frequency variation	3.0V to 5.5V, constant temperature			±5	%
Internal clock temperature dependent frequency variation	3.0V to 5.5V, full temperature range			±10	%
Internal clock frequency deviation for 0.5V drop	3.0V to 4.5V, constant temperature			±2	%
EEPROM write time			3	10	ms
Internal clock start up time	(Note 5)			2	ms
Oscillator start up time	(Note 5)			2400	cycles

Preliminary ACE1202REM Low Battery Detect (LBD) Characteristics, V_{CC} = 2.2 to 5.5V

Parameter		Conditions	MIN	TYP	MAX	Unit
LowBattLev	Addr. 0x67	-40°C		2.45		V
		0°C		2.63		V
		+25°C		2.67		V
		+85°C		2.87		V

Preliminary ACE1202REM Brown-out Reset (BOR) Characteristics, V_{CC} = 2.2 to 5.5V

Parameter	Conditions	MIN	TYP	MAX	Unit
BOR Trigger Threshold	-40°C		1.98		V
	0°C		2.06		V
	+25°C		2.12		V
	+85°C		2.27		V

3.1 Preliminary AC & DC Electrical Characteristic Graphs

Figure 3: Internal Oscillator Frequency

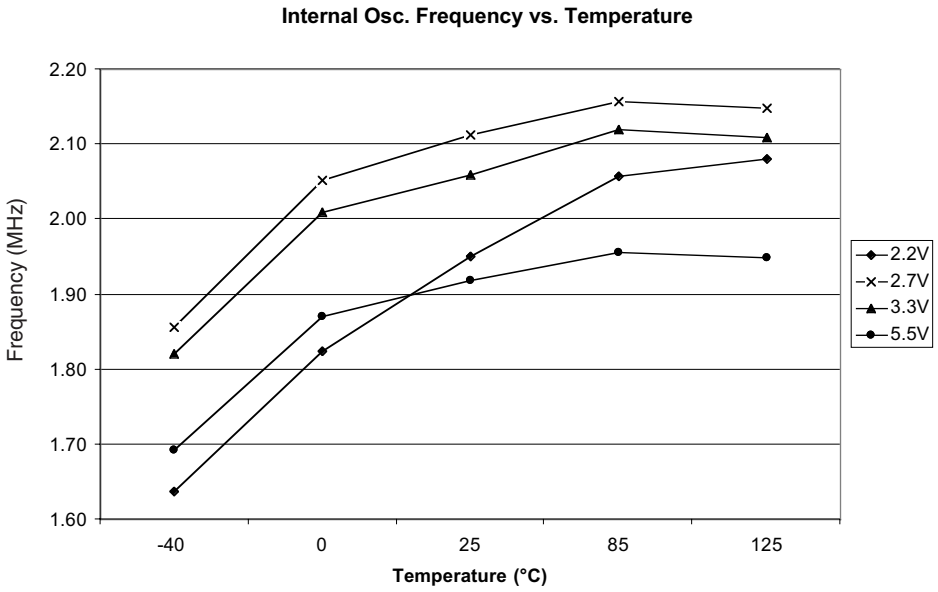
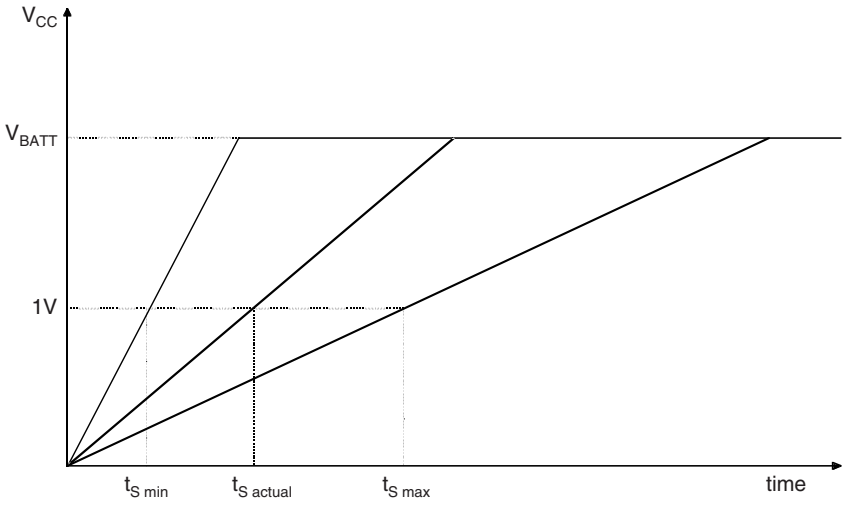
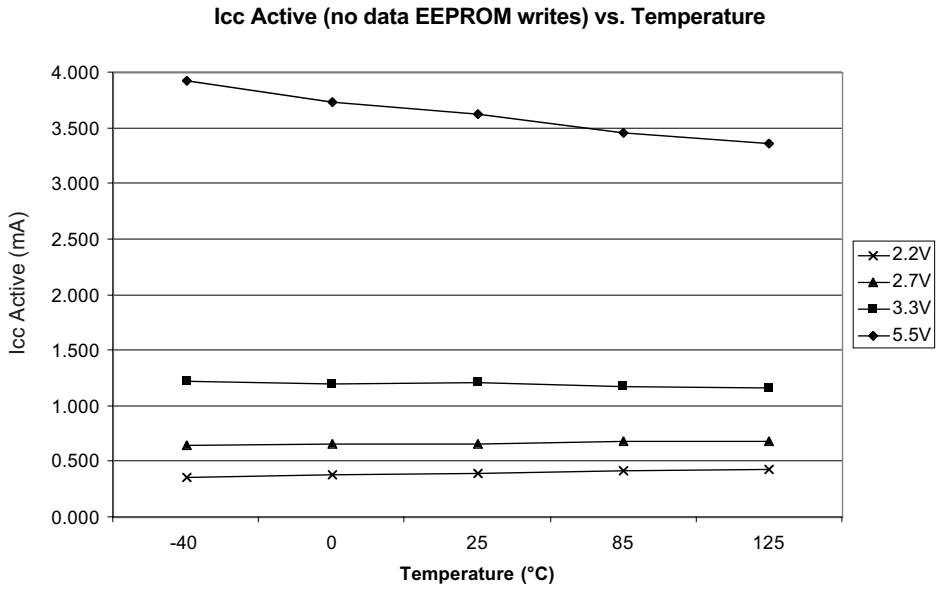


Figure 4: Power Supply Rise Time



Name	Parameter	Unit
V_{CC}	Supply Voltage	[V]
V_{BATT}	Battery Voltage (Nominal Operating Voltage)	[V]
$t_{S\ min}$	Minimum Time for V_{CC} to Rise by 1V	[ms]
$t_{S\ actual}$	Actual Time for V_{CC} to Rise by 1V	[ms]
$t_{S\ max}$	Maximum Time for V_{CC} to Rise by 1V	[ms]
S_{VCC}	Power Supply Slope	[ms/V]

Figure 5: I_{CC} Active



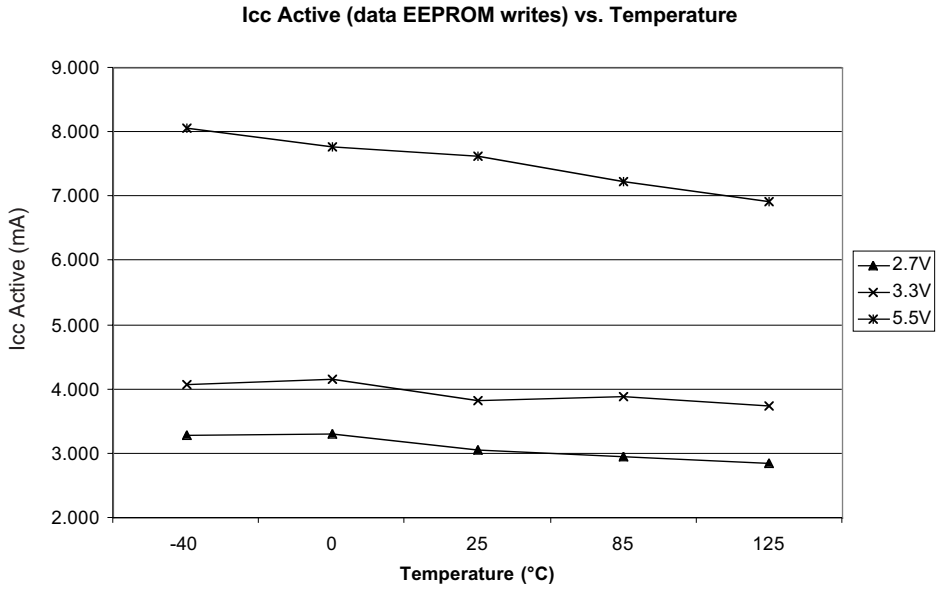
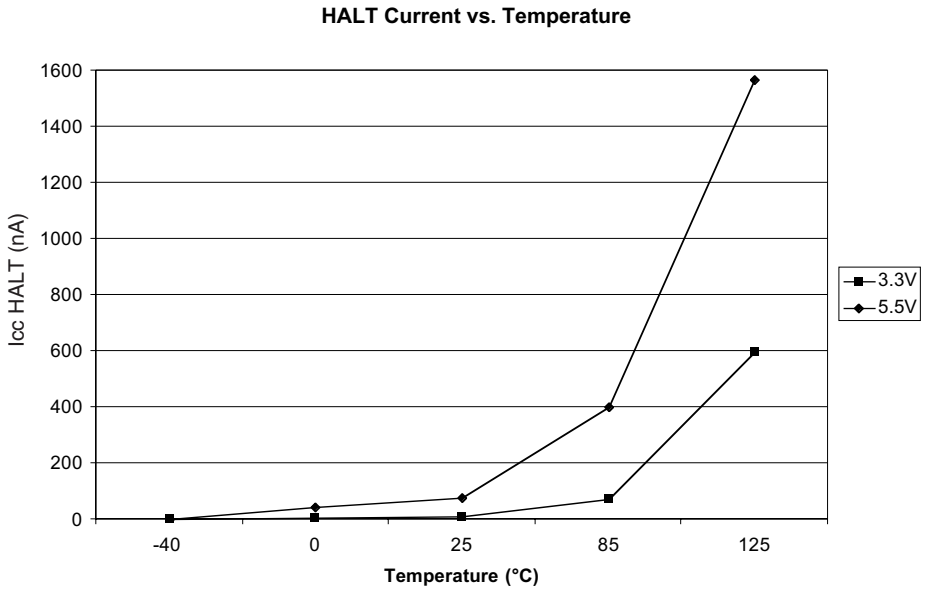


Figure 6: HALT Current



4.0 General Characteristics

ACE1202R is intended for use with the ACE1202T product. This chip-set forms a secure and inexpensive system for a variety of applications that require a high level of security such as remote keyless entry or software protection.

The basic function of the ACE1202R is to receive a DES coded message frame containing a fixed identifier (24-bit), data field (8-bit), DES code (32-bit), a sequential counter (16-bit), and a parity field. This frame is received in a PWM coded format suitable for a RF system or a NRZ format, used in a direct wire connection[5]. This frame will be compared with previously stored information in order to match the fixed and dynamic part of the code message.

4.1 Mode of Operations

ACE1202R can be programmed to work in three different modes as indicated in Table 5 and is description in later sections.

Table 5 ACE1202R Operating Modes

Operating Modes	Description
PWM Mode	Indicated to work with a RF module
NRZ Mode connection	Indicated to work with wired
Programming mode defined area	To select and program the user

[5] PWM coding is typically used in RF transmission, NRZ coding can be used as well however the bit rate tolerance is a critical aspect to consider to extract correct information. We suggest to adopt NRZ mode for wired direct connection.

5.0 DES Message Description

The DES coded message is 12-bytes wide and is divided into fields transmitted in the following order:

- **Preamble** – Sent only once as a continuous series of frames used to wake the receiver from HALT mode.
- **SYNC field** – 8 coded bits for the synchronization of the incoming data stream.
- **Data field** – Contains information about the channel selected and special transmitting modes: DES_KEY and DES_COUNTER. It is 8 bits wide.
- **Fixed field** – A unique 24-bit code that identifies the transmitter.
- **DES field** – The 32-bit DES generated code.
- **Counter field** – The lower 16 bits of the DES Counter.
- **Parity field** – Byte-wise exclusive-or from SYNC Field to DES Field.

The frame type selection bits of the Data field configures the DES field for one of three configurations. The three DES frame configurations are the NORMAL Frame, the SYNC_DES_KEY Frame, and the SYNC_DES_CNT Frame. (See Figure 7)

5.1 SYNC Field

The SYNC field is 8-bits wide and identifies the start of the DES frame.

5.2 Fixed Field

The Fixed Field is three bytes (24-bits) long and is used to identify the individual transmitter. If the Fixed Field is not found in the ACE1202R memory, the frame will be rejected. The ACE1202R must learn the Fixed Field while in a special operating mode. (See Section 7.1.)

5.3 Data field

The Data field contains the current configuration of the transmission. Bits 7 to 4 decode the binary transmitter key configuration. The least significant nibble selects the frame type. See Table 6 for details.

Table 6 Data Field Bit Definition

Bit	Value	Description
Bit 7	'1'	KEY1 has been pressed -> activate 01
Bit 6	'1'	KEY2 has been pressed -> activate 02
Bit 5	'1'	KEY3 has been pressed -> activate 03
Bit 4	'1'	KEY4 has been pressed -> activate 04
Bit 3-0	Frame Type Selection:	
	'0000'	NORMAL
	'0010'	DES KEY SYNC
	'0011'	DES COUNTER SYNC
	'1111'	Low Battery

5.4 DES Code field

The DES Code field is the 32 most significant bits of the calculated DES algorithm using the known DES KEY and COUNTER. (See Section 6.0) This field is compared with the DES CODE calculated internally by the receiver. This field is only sent in the NORMAL frame.

5.5 Counter field

The Counter field is the 16 least significant bits of the internal 64-bit DES counter. The counter is used to synchronize the DES operation on the receiver side. This field is transmitted only in the NORMAL frame. This information helps track the current DES progression held in the linear DES COUNTER. Normally, only one calculation is needed to determine the current DES CODE.

5.6 Parity field

The Parity field is present in all the frames and contains the checksum for the frame transmitted. The checksum is the exclusive-or of all bytes received in the frames starting from SYNC field.

5.7 DES KEY field

The DES KEY field is the security DES KEY used in the algorithm to calculate the current DES Code. The four least significant bits in the Data Field indicate to the receiver that a SYNC_DES_KEY frame (0x02) will be received. The receiver will store the DES KEY in the internal register for future NORMAL frame decoding.

The true length of the DES KEY is 56-bits wide. The DES KEY field is 48 bits wide (addr. 0x45 to 0x4A duplicated in addr. 0x75 to 0x7A) and the remaining 8 bits of the DES KEY is a user defined value, stored in memory (addr. 0x4B, duplicated in addr. 0x7B) during factory programming, otherwise it is defaulted to 0x00.

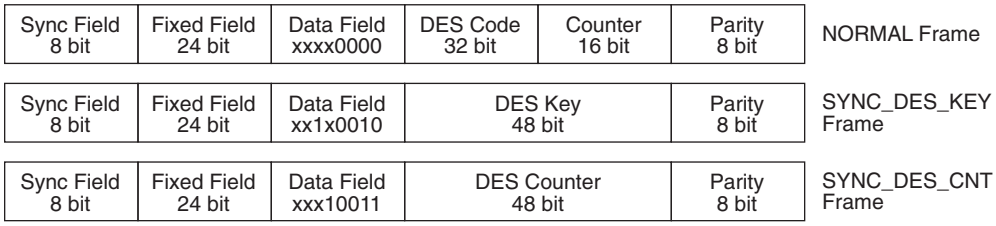
If pin 1 of the ACE1202R is set to logic '0', the receiver will ignore any SYNC Frame requests.

5.8 DES COUNTER field

The DES COUNTER field is the 48-bit DES COUNTER used in the algorithm to calculate the current DES Code. The four least significant bits in the Data Field indicate to the receiver that a SYNC_DES_CNT frame (0x03) will be received. The DES COUNTER will be stored in the internal registers for future NORMAL frame decoding.

The true length of the DES COUNTER is 64-bits long. The DES COUNTER field is 48-bits and the remaining 16 least significant bits are set to '0' every time a SYNC_DES_CNT frame is transmitted. If pin 1 of ACE1202R is set to logic '0', the receiver will ignore any SYNC Frame request.

Figure 7. NORMAL and SYNC Frames



6.0 DES Algorithm

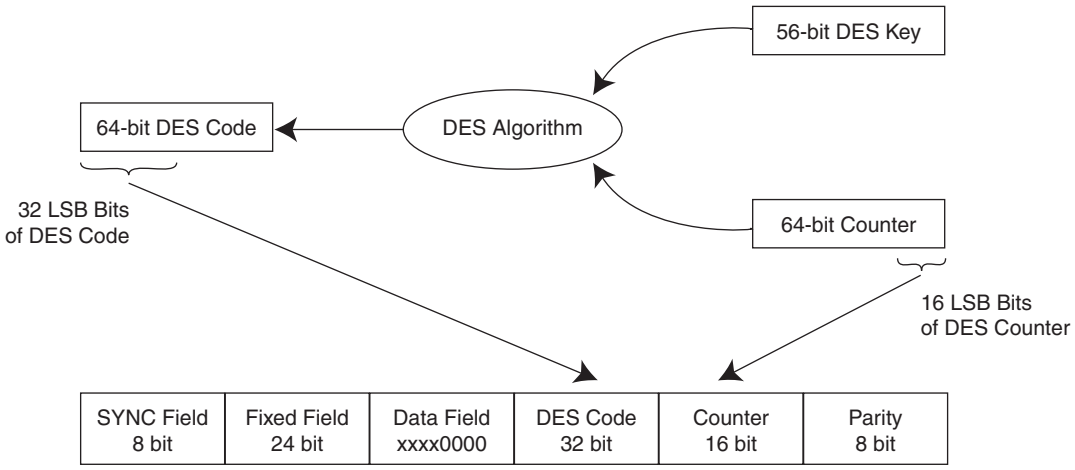
With the help of the National Security Agency the National Bureau of Standards certified the Data Encryption Standard (DES) in the1977 to be used in electronic devices for the protection of coded data during transmission and storage in a computer system or network

The DES algorithm is different from other cryptography algorithms in that it is not kept in secret like the others. The DES algorithm is public and the system security is based on a secret key (DES KEY) of 56-bits plus 8-bits of parity known only by the transmitter and receiver. The DES key must be transmitted or directly stored in the transmitter / receiver memory.

The implementation of the DES algorithm used in the ACE1202R and ACE1202T chip-set does not use the initial and final permutations normally used in DES, as there is no benefit in implementing these permutations where DES is used for authentication.

Figure 8 shows how the DES algorithm encodes a 64-bit counter using a 56-bit DES key to obtain the 64-bit DES code.

Figure 8 DES Algorithm data flow



7.0 System Operation

To validate a NORMAL frame received, the receiver must know the secret DES KEY and the 64-bit counter. The receiver determines these parameters either through the LEARNING MODE or by PRE-PROGRAMMING.

7.1 LEARNING MODE

To enter into the LEARNING MODE, the transmitter has to be enabled to send the SYNC frame[6] while pin 1 on ACE1202R is at logic level '1.'

As soon as a SYNC frame (KEY or COUNTER) has been received, the information will be stored in the ACE1202R EEPROM (See Section 8.3) replacing any previously stored information.

If a SYNC_DES_KEY frame is received and bit 0 (*AutoCntr*) in the OPTIONS register is set, the DES COUNTER will be initialized as fixed. This saves an extra operation in sending a separate SYNC_DES_CNT frame.

7.2 PRE-PROGRAMMING

If the transmitter is coupled with the receiver module after factory assembly, all the needed parameters (Fixed Code, DES KEY, and DES COUNTER) can be stored directly into ACE1202R User Area using the 2/4 wire programming interface described in Sections 8.0 and 11.0. If needed, the User Area can be protected after programming to prevent external reading or writing of the User Area.

[6] See the ACE1202T datasheet at www.fairchildsemi.com for details.

8.0 USER Area:

It is possible to read, write, or protect the user-defined area using a 2-wire programming interface. The programming interface operates as a half duplex asynchronous protocol with TxD (Pin 4) and RxD (Pin 5) dedicated lines with communications using the NRZ format. The NRZ format operates at a baud rate of 4800bps and a data frame format of 8 data bits, 1 start bit, and 1 stop bit.

In order to enter programming mode, pins 4 and 5 must be at logic '1' level during power-up. After 500ms the part is ready to accept command from an external programmer. The first message must be a character corresponding to the hex value 0x55 needed to calibrate the internal baud-rate register. Upon reception of the baud adjustment message, ACE1202R will respond with an acknowledge message to inform the external programmer to be ready to receive new messages.

The message structure is variable in length and follows the form:

a) [0x55]: Sent only from ACE1202R to external ACE1202T or Programmer

b) Nbytes: The number of bytes to send – 1

c) OpCode: Op-code field

d) Data: Variable field from 1 to 15 bytes depending on op-code

e) Checksum: Logical byte-wise exclusive-or of the previous fields b) to c)

Possible messages are:

EEPROM READ (Progr. to ACE1202R)

Nbytes + READ_USR_AREA + Addr. + Checksum (To read any location in User Area)

Nbytes = 3
READ_USR_AREA = 0x38

This message is valid only if the **RD_PROTECT** bit is zero in **OPTIONS** address (0x60). If the operation is executed correctly, the **ACE1202R** will return the message:

Nbytes + READ_USR_AREA + Addr. + Read_Value + Checksum, otherwise the message UNKNOWN will be returned.

EEPROM WRITE (Progr. to ACE1202R)

Nbytes + WRITE USR_AREA + Addr.+ Value + Checksum (To write any location in User Area)

Nbytes = 4
WRITE_USR_AREA = 0x93

This message is valid only if the **WR_PROTECT** bit is zero in **OPTIONS** address (0x60). If the operation is executed correctly, the ACE1202R will return the message:

Nbytes + WRITE_USR_AREA + Addr. + Programmed_Value + Checksum, otherwise the message UNKNOWN will be returned.

DES FRAME (ACE1202R to ACE1202T) / DES VALID (ACE1202T to ACE1202R)

[0x55] + Nbytes + DES_FRAME + FixedHigh + FixedMid + FixedLow + Data + Cnt0 + Cnt1 + DES3 + DES2 + DES1 + DES0 + Checksum (This is the DES frame to be checked by the internal algorithm)

Nbytes = 12
DES_FRAME = DES_VALID = 0x5A

If the message has correct checksum and a valid DES code, it will answer with the next DES Code generated by incrementing the DES COUNTER. If the message contains an invalid DES Code ACE1202T will re-send the same message back to ACE1202R (See Section 12.0).

The 0x55 preamble is sent only from ACE1202R to ACE1202T (DES_FRAME)

DES KEY and COUNTER info (ACE1202R to ACE1202T)

0x55 + Nbytes + DES_PAR + SyncField + FixedHigh + FixedMid + FixedLow + DES_KEY0 + DES_KEY1 + DES_KEY2 + DES_KEY3 + DES_KEY4 + DES_KEY5 + DES_CNT2 + DES_CNT3 + DES_CNT4 + DES_CNT5 + DES_CNT6 + DES_CNT7 + Checksum (DES information for ACE1202T).

Nbytes = 18
DES_PAR = 0x44

This frame is sent when the ACE1202T is not in programmed state (BLANKED) and it is used to store the DES parameters, DES Key, DES Counter and fix code into ACE1202T user area.

STATUS REQUEST (ACE1202R to ACE1202T)

0x55 + Nbytes + RX_STAT_REQ + ACERX_STATE + SW_Revision + Checksum (This message is only sent after PC connection, following the inquire (0x55) parameter.)

Nbytes = 4
RX_STAT_REQ = 0x40

ACE-R_STATE = 0x2A-> RX has no DES information stored in memory

ACE-R_STATE = 0x33 -> RX has DES information stored in memory

SW_Revision: Bit0 to 3 = Data EEPROM revision
Bit4 to 7 = Code Revision

EXIT (Progr. to ACE1202R)

Nbytes + EXIT + Checksum (To exit from 'Programming mode')

Nbytes = 2
EXIT = 0x2B

8.1 Message table

Table 7 NRZ Messages

Message	Byte Sent – 1	Op-Code	Meaning
READ_USR_AREA	3	0x38	Progr to ACE1202R - Read one location at specified address
WRITE_USR_AREA	4	0x93	Progr to ACE1202R – Write data at specified address
DES_FRAME	12	0x5A	ACE1202R to ACE1202T – Send current DES code
DES_PARAM	18	0x44	ACE1202R to ACE1202T – Send DES parameter to store
RX_STAT	3	0x40	ACE1202R to Progr. – Actual ACE1202R status
EXIT	2	0x2B	Progr to ACE1202R – Exit from Progr connection
UNKNOWN	2	0x55	ACE1202R response to invalid messages
DES_VALID	12	0x5A	ACE1202T to ACE1202R – Next calculated DES Code

8.2 Programming recommendations:

ACE1202R and ACE1202T are delivered from the factory with default values loaded into USER Area allowing the designer to perform a test on the parts without data initialization.

The programming interface is designed to allow easy in-circuit programming using the 4-wires interface. It is the responsibility of the user to load the appropriate value in the USER Area.

It is recommended always to set the Read and Write protection bits prior to terminating the programming process.

If further programming is needed, the Read protection bit should be enabled to avoid external reading of the DES information which need to remain secret to avoid system intrusion.

8.3 USER AREA Table

Table 8 USER Area Registers

Addr.	Label	Description	Note
0x40	Unused		
0x41-0x71	Sync Field	8 bit Synchronization field	Read/Write
0x42-0x72	Fixed High	24 bit fixed code – High Part	Read/Write
0x43-0x73	Fixed Mid	24 bit fixed code – Mid Part	Read/Write
0x44-0x74	Fixed Low	24 bit fixed code – Low Part	Read/Write
0x45-0x75	DES_KEY0	56 bit DES KEY – byte 0	Read/Write
0x46-0x76	DES_KEY1	56 bit DES KEY – byte 1	Read/Write
0x47-0x77	DES_KEY2	56 bit DES KEY – byte 2	Read/Write
0x48-0x78	DES_KEY3	56 bit DES KEY – byte 3	Read/Write
0x49-0x79	DES_KEY4	56 bit DES KEY – byte 4	Read/Write
0x4A-0x7A	DES_KEY5	56 bit DES KEY – byte 5	Read/Write
0x4B-0x7B	DES_KEY6	56 bit DES KEY – byte 6 – User Defined.	Read/Write
0x4C-0x7C	DES_KEY_CHECK	DES _K+ FIXED checksum value	Read/Write
0x4D	DES_CNT0_A	64 bit DES Counter – Byte 0	Bank 0 - Read/Write
0x4E	DES_CNT1_A	64 bit DES Counter – Byte 1	Bank 0 - Read/Write
0x4F	DES_CNT2_A	64 bit DES Counter – Byte 2	Bank 0 - Read/Write
0x50	DES_CNT3_A	64 bit DES Counter – Byte 3	Bank 0 - Read/Write
0x51	DES_CNT4_A	64 bit DES Counter – Byte 4	Bank 0 - Read/Write
0x52	DES_CNT5_A	64 bit DES Counter – Byte 5	Bank 0 - Read/Write
0x53	DES_CNT6_A	64 bit DES Counter – Byte 6	Bank 0 - Read/Write
0x54	DES_CNT7_A	64 bit DES Counter – Byte 7	Bank 0 - Read/Write
0x55	DES_CNTA_CHECK	Counter A Checksum	Bank 0 - Read/Write
0x5F			
0x60	OPTIONS	Operation options	Read/Write
0x61	RX_Timeout	Active time waiting for messages to be received	Read/Write Step 8.2ms
0x62	RXAWAKE	- RF Module power up cycle (PWM mode) - In NRZ mode is the ACE1202T polling time	Step 8.2ms - Read/Write Step 50ms in NRZ
0x63	PULSE_OUT	Out1 – 4 Pulse duration	Step 2.5ms - Read/Write
0x64	MASK_PORT	XOR mask for PORTG	Read/Write
0x65	BAUD_ADJ	Adjusted Baud-rate value	Read Only
0x66	ACERX_STATE	Functional receiver state	Read/Write
0x67	LowBattLev	Low Battery level - 2.6V	Read/Write[7]
0x6D	Factory Data1	Free	Read/Write
0x6E	Factory Data2	Free	Read/Write
0x6F	Data EEPROM Revision	EEPROM data revision 0 to 0xF	Read/Write[7]

[7] Though it is possible to write in this location, it is recommended not to modify the factory defined values.

8.4 OPTIONS Register (Addr. 0x60)

Bit 0 – AutoCntr

If set to '1,' the DES counter will be set to a unique secret configuration once the SYNC_DES_KEY frame is received.

Bit 1 – ForceNRZ

When this bit is set to '1,' the ACE1202R enters the NRZ mode regardless of the pin levels (after a power-on reset) on the RxD and TxD pins. This option can be used only when the requested mode is NRZ or to save external pull-ups on the RxD and TxD pins.

Bit 2 – LowPowerM

If set to '1,' a special low power mode is enabled using the internal IDLE mode (see Section 9.0.) The ONR pin is used to switch an external power supply to the external RF Receiver module. The ONR timing is defined in the RX_Timeout and RXAWAKE registers.

Bit 3 – ForceProgr

If set to '1,' a '0' on the LRN pin will force the ACE1202R to enter into programming mode. Programming mode is left as soon as the LRN pin returns to V_{CC}.

Bit 4 – EnaLearn

If the ForceProgr bit of the OPTIONS register is '1,' the EnaLearn bit becomes active (set to '1') allowing the ACE1202R to receive SYNC frames. The EnaLearn bit may be used to replace the external LRN pin feature with a programmable option through the ForceProgr bit.

Bit 5 – DESPar

If set to '0,' the ACE1202R is allowed to send the DES Parameters through the NRZ connection to the ACE1202T. If set to '1,' the DES parameters must be pre-programmed in both the ACE1202R and ACE1202T.

Bit 6 – RD_PROTECT

When programmed to '1,' the USER area registers can no longer be. Once the RD_PROTECT bit is set and the USER area is read protected, no other writes to the RD_PROTECT bit is possible. (The RD_PROTECT bit is automatically write protected.)

Bit 7 – WR_PROTECT

If set to '1,' it is no longer possible to write values into the USER area.

8.5 RX_Timeout Register (Addr. 0x61)

The RX_timeout register determines the maximum length of time for a valid PWM bit. If a PWM bit period is valid, the timeout counter is reset allowing the ACE1202R to receive the next bit of data. (The step size correction is 8.2ms.)

If the LowPowerM bit of the OPTIONS register is '0,' once the ACE1202R has timed out the receiver will enter into HALT mode. However, if the LowPowerM bit is '1,' the receiver will enter into a special low power mode using IDLE. (See Section 9.0 for details.)

8.6 RXAWAKE Register (Addr. 0x62)

When ACE1202R is connected in PWM mode, the RXAWAKE register defines the number of cycles to power down the external RF module. The ACE1202R's internal IDLE timer determines the timing (8192 us) for the power down cycles. (I.e. if a 10 decimal is written to the RXAWAKE register the ACE1202R resumes operation after 81.92 ms.) This register is valid only if the LowPowerM bit of OPTIONS register is programmed to '1.'

When ACE1202R is connected in NRZ mode, the RXAWAKE register determines the ACE1202T Status inquire timing used to poll an external ACE1202T on the communication lines. The step size in this mode is 50ms.

8.7 PulseOut Register (Addr. 0x63)

If the OutState bit of the MASK_PORT register is '1,' the Pulse_Out register defines the O1-O4 pulse duration that follows a valid received frame. The MASK_PORT register also defines the polarity (active high or low) of this pulse (see Section 8.8.) The timing step is 2.5ms.

8.8 MASK_PORT Register (Addr. 0x64)

The MASK_PORT register defines the output pin polarity of the O1 through O4 and ONR signals. If the respective bit is '0,' the output pin is active HIGH. If it is '1,' the output pin is active LOW.

Bit 3 – OutState

If the OutState bit is '0,' the O1 through O4 output pins produce a stable binary level after the DES Frame is received. If the OutState bit is '1,' the O1 through O4 output pins produce a pulse rather than a binary level with the pulse width defined by the Pulse_Out register. The MASK_PORT register bits 0, 1, 4, and 5 define the polarity (active high or low) of each output.

Upon reception of the DES Frame, the Data Field (Bit 7 to 4) information is decoded to determine which output(s) to apply the OutState condition to.

Bit 7 - Out_Toggle

If Out_Toggle is '1,' the outputs (O1 – O4) selected by the Data Field, received in the DES Frame (Bit 7 to 4), will change states every time a new frame is received. When no framed are received, the selected output(s) will maintain its state. However, if set to '0,' the O1- O4 output behavior is dictated by the OutState selection. The Out_Toggle bit feature is valid only when the OutState is '0.'

8.9 BAUD_ADJ Register (Addr. 0x65)

The BAUD_ADJ register contains the auto-adjusted baud rate value. This value is automatically adjusted and should not be changed.

8.10 ACERX_STATE Register (Addr. 0x66)

The ACERX_STATE register stores the current state of the receiver. It contains the value 0x33 if no DES parameters are stored in the USER area (blank from factory.) Once the DES information is transferred into the user area, the external programmer must take care to write the value 0x2A into this location. This information is used just to keep track of an external write access of the DES User area.

8.11 Factory Data1 to 3 (0x6D to 0x6F)

These unused locations could be programmed to hold User Factory information such production date to track lot and testing information.

8.12 Software Revision (0x6F)

Contains the EEPROM data version (0 to 0xF) and can be read through external programmer by asserting an Inquire command (0x55.)

Figure 9 OPTIONS Register Bit Definition

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WR_PROTECT	RD_PROTECT	DESPar	EnaLearn	ForceProgr	LowPowerM	ForceNRZ	AutoCntr

Figure 10 MASK_PORT Register Bit Definition

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Out_Toggle	Level_ONR	Level O4	Level O3	OutState	X	Level O2	Level O1

9.0 PWM Mode

The PWM mode is intended for use in RF transmissions. The bit coding is defined as 1/3 or 2/3 duty cycle to distinguish between coded '0' and '1' respectively. (See Figure 11)

A bit decoding algorithm will capture each single pulse transition (a rising to falling edge is 'Ph' and a falling to rising edge is 'Pl'.) The sum of the pulses will be compared to the min/max values. Ph will then be subtracted from Pl. The result is the bit to decode and will be shifted into a buffer:

If (Ph < Pl) then BitDecode = '0'
Else BitDecode = '1'

The decoding process is divided in two phases, SYNC decoding and Message Decoding. In SYNC decoding, the receiver is continuously shifting coded bit until a complete byte, which value corresponds to the SYNC field, is received. This condition is used to start the reception of the DES message (2nd phase) using a bit counter to determine the end of message. Every time an out of range timing is found the process is restarted from phase 1 waiting for a new SYNC field.

When the *LowPowerM* option is enabled, a special mode is used to minimize the total current consumption drawn by the receiving system. The pin ONR is used to switch the RF-Module power supply, as indicated in Figure 14. The receiver active time is defined by register RX_Timeout, while the power down phase is determined by register RXAWAKE.

In order to further reduce the current consumption, the ACE1202R uses the IDLE mode. In this mode, the current drawn (ACE1202R only) is typically 200µA @ 5.5V. The ACE1202R exits IDLE mode every 8192 Tcycles (whenever the IDLE timer underflows.[8]) The value contained in RXAWAKE is the number of IDLE cycles. Before entering the active phase, the ACE1202T has the possibility to add a Preamble field with programmable duration to consider the IDLE cycles in the active phase. (See Figure 12)

The example in Figure 12 shows the waveform of the signals involved when RXWAKE = 4. The PREAMBLE has to be at least 5 IDLE cycles long to receive the message at the first frame. Once exiting HALT mode, the ACE1202R waits at least RX_Timeout * 2.5 ms before HALT mode can be entered again. If a valid PWM bit is received before RX_Timeout expires, the timeout will be set to the initial counting value.

[8] See the ACE1202 Product Family datasheet at www.fairchildsemi.com for more details.

Figure 11 PWM Encoding Bits

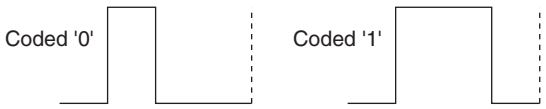
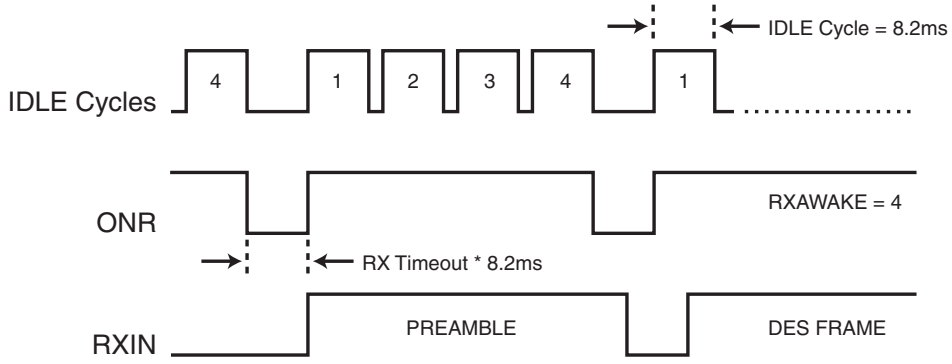


Figure 12 Receiver V_{CC} switched mode



10.0 Typical application circuit:

The schematic in Figure 13 shows a typical application where the ACE1202R is used as a standalone module. The ACE1202R takes care to switch the RF module power supply in order to minimize the power consumption. Refer to the waveforms shown in Figure 12 to see the relationship between received PREAMBLE and switching voltage. As described above, the PREAMBLE must be at least two VRF voltage cycles long, which allows the detection of an incoming signal at the very first frame. Once a preamble is detected, the RF Module is powered continuously. The incoming data stream is then decoded by the ACE1202R.

When the code has been completely received, the ACE1202R will perform the following operations on the stored buffer:

1) Checksum validation

2) Fixed Code presence

3) DES validation

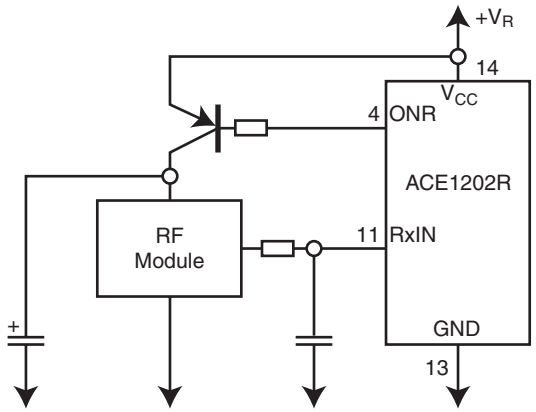
4) Output result

5) Auto-repetition Control

In cases where the current consumption is not an issue, the RF module can be powered directly from the Vcc line. For this case, the ACE1202R is in HALT mode when there is no data detected on pin 11 (RxIN), a rising edge on this pin will activate the ACE1202R to decode an incoming message or return to sleep if no valid PWM bits are received.

The *LowPowerM* bit in the OPTIONS register must be '0' to disable the Receiver Switched mode.

Figure 13 Low Power Receiver



11.0 NRZ MODE (Bidirectional)

The NRZ mode is suited for wire operating applications such as software protection where the transmitter unit (ACE1202T) can be connected through a dedicated connection to the receiver (ACE1202R).

To enable NRZ mode, Pin 4 and 5 must be high for at least 200ms following a Power-on Reset or an external Reset (pin 10.)

Upon connection, the transmitter senses a polling message coming from the ACE1202R TxD line on pin 4 (RxD). The polling message contains two bytes. The transmitter uses the first byte (0x55) of the polling message to auto-calibrate its internal baud-rate. The second byte is a request from the receiver for the transmitter's STATUS information. Once the transmitter is calibrated, the STATUS information is sent.

The status value can be:

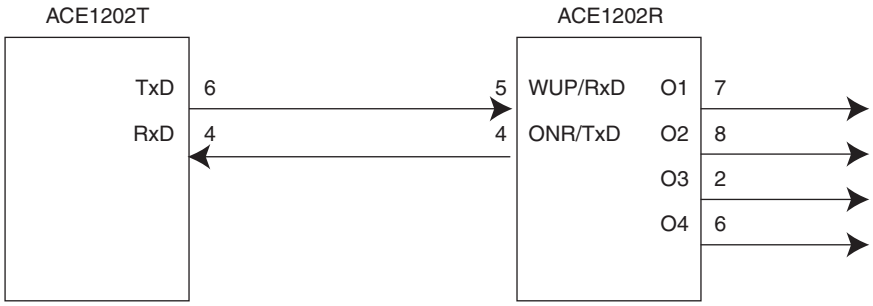
PROGRAMMED (Internal codes stored in ACE1202T)
BLANKED (Not yet coupled with ACE1202R)

If ACE1202R is connected to a BLANKED transmitter, it will automatically send a frame containing the Fixed Code, DES KEY, and DES Counter. In order to send the DES information, the bit DESPar in the OPTIONS register must be set to '1'. The ACE1202T will store this information in its user area and will reply to the ACE1202R with a new status message informing the receiver of the change to PROGRAMMED mode. Once this information is received, the ACE1202R will periodically transmit a STATUS request message (0x55 + 0x55) to the transmitter. (The timing is defined in register RXAWAKE with a 50ms step size.)

The ACE1202T will use the STATUS request message to adjust the internal baud rate and answer with its internal status. At this point, the ACE1202T responds with PROGRAMMED. The ACE1202R will then send the DES coded message [DES_FRAME] corresponding to the actual value of the DES Counter. The ACE1202T will compare the information received with its internal DES code. If a match is found, the next DES code (obtained by incrementing the internal DES Counter) will be sent back to ACE1202R for validation. If there is no match with the DES code sent from the ACE1202R, the same code will be sent back.

Once a validation cycle has completed, the value received in the Data field (bit 7 to 5) is put onto the ACE1202R output ports (O1 to O4).

Figure 14 NRZ Connection



12.0 Connection messages

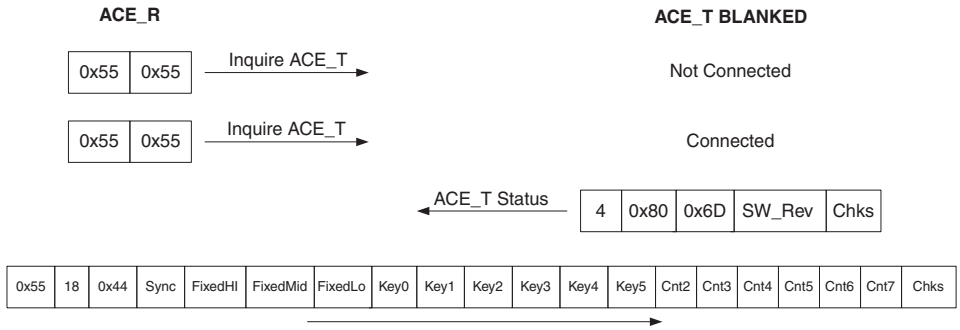
Figure 15 shows the communication protocol between the ACE1202T and the ACE1202R. The ACE1202R continuously sends an Inquire message (0x55) to the ACE1202T until the transmitter answer with its STATUS information. When a BLANKED ACE1202T is connected, the ACE1202R provides the DES Information needed to perform the DES algorithm[9]. The ACE1202T will store the DES KEY and COUNTER and change its state to PROGRAMMED.

[9] Bit DESPar in the OPTIONS register must be set to '1.'

When the next Inquire message is received by the ACE1202T, it will inform the ACE1202R that it is in the PROGRAMMED state. The ACE1202R will then send the next DES code for validation by ACE1202T. If the DES Code is acknowledge, the ACE1202T will reply with the next DES Code (DES COUNTER is incremented by one) for validation by ACE1202R. After the ACE1202R DES Code is validated, the DES COUNTER is updated. Otherwise, the old value is maintained and the Data field contents will be placed on the outputs (O1-O4.) The Data field is loaded with the contents of the DataCode register (0x6C) defined in the ACE1202T USER Area.

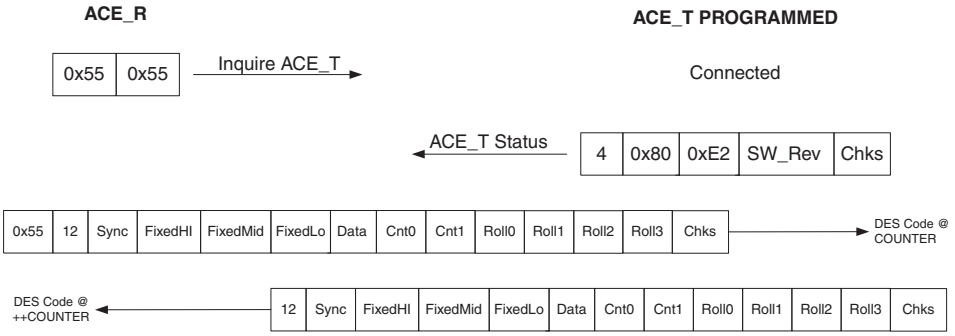
Figure 15. ACE1202T (ACE_T) with ACE1202R (ACE_R) connection

a) Communicating with a BLANKED ACE_T



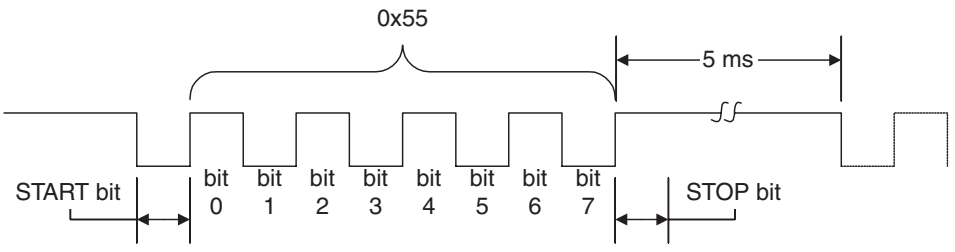
ACE_T will store the DES information changing the state to PROGRAMMED

b) Communicating with a PROGRAMMED ACE_T



Cycle is repeated sending another Inquire TX command

c) Serial data protocol



Note: All the bytes transmitted or received must be spaced at least 5ms apart.

13.0 Application Circuits

13.1 Stand Alone Receiver

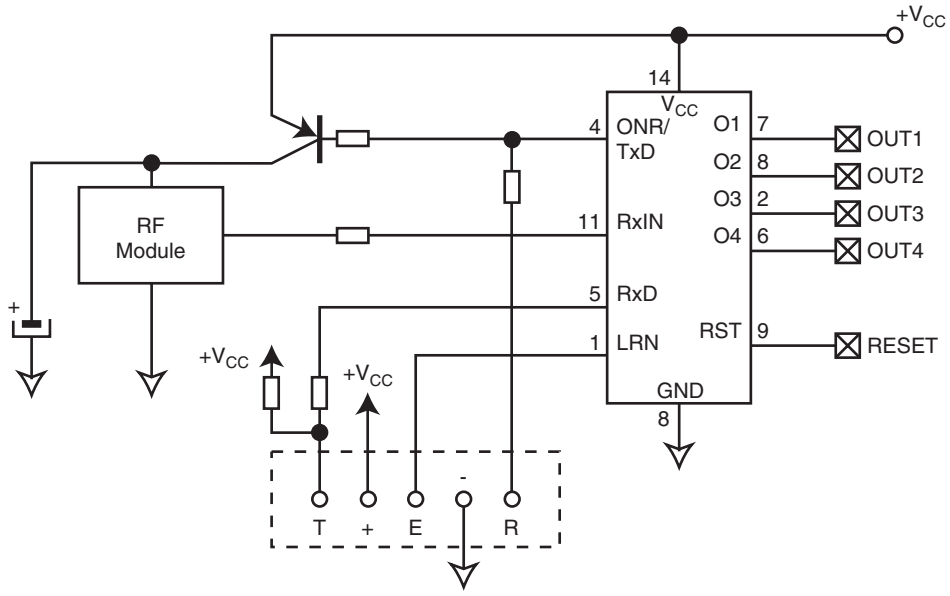
The Stand Alone Receiver application circuit shows the possibility to synchronize an ACE1202T without sending DES information on RF that can compromise security if not done in a controlled environment.

The ACE1202T will be connected through programming interface driving the line E to ground. This will assert the ACE1202R line LRN low forcing ACE1202R to enter in programming mode. At this point, the ACE1202R will send TX inquiry messages waiting for the ACE1202T's status that must be BLANKED to allow DES parameter downloading. (See Section 11.0) When ACE1202T is PROGRAMMED, no further programming is possible and the only way to alter the DES stored information is entering the Programming mode with *WR_Protect* option disabled and sending the EEPROM Write commands.

Once the ACE1202R has transferred all the DES information, it will continue to inquire the ACE1202T checking the generation of the new DES code. The process will continue as long as the pin 1 (LRN) is '0'. Once the ACE1202T is removed from programming connection, the pin 1 will go high and the Programming routine is left waiting for a message on pin 11 (RF data).

This mode is possible if bit ForceProgr in OPTIONS register is set.

Figure 16 Receiver Block with Programming Interface



13.2 2-Wire Connection[10]

The circuit in Figure 17, shows how to implement a simple 2-wire connection between the ACE1202T and the ACE1202R.

The line 'A' carries power supply and data information that is roughly one-volt modulation over the established DC voltage level. The power is delivered from the receiver unit while the transmitter acts as a passive key. If needed, the supply source can be inverted (the ACE1202T is the source and the ACE1202R is the passive element).

Capacitor C1 delivers current to ACE1202T during the message modulation, on both ACE1202T and ACE1202R, and it is the key element to demodulate information sent.

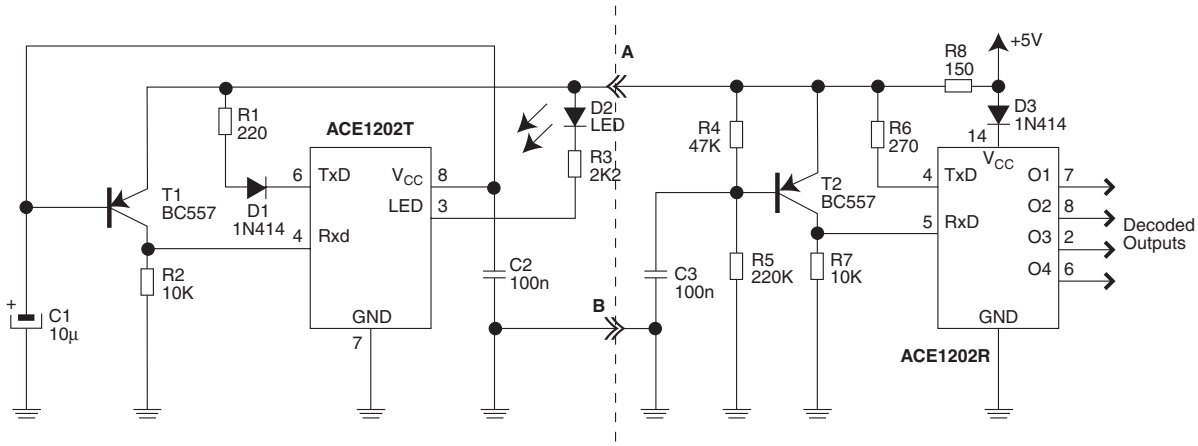
After connection, C1 is charged from R8 in a time faster than 50ms (this time required for the internal Power-on Reset circuit to operate correctly). After connection, both circuits (ACE1202T and ACE1202R) detect a NRZ connection mode reading '1' on respective RxD and TxD lines. At this moment ACE1202R starts to interrogate ACE1202T with message 0x55 until it receives a status response from ACE1202T. The process continues as indicated in Section 11.0.

The proposed circuit does not provide electrical protection in case the boards are connected to a non-compatible soure or extreme electrical noise.

The LED informs the user about the correct DES algorithm acknowledge and DES parameter stored. The use of this LED is optional.

[10]Component values and schematic not tested in a real application.

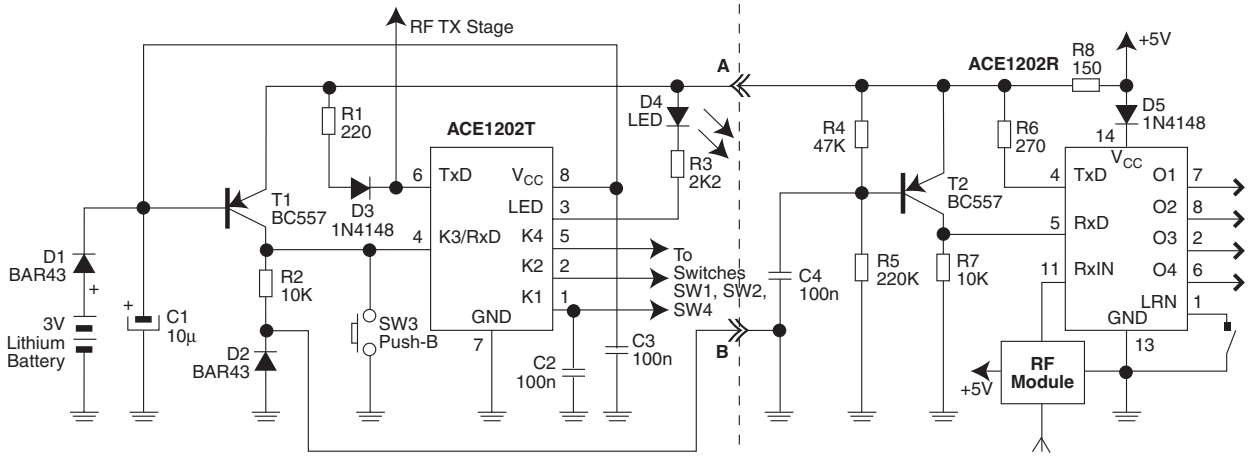
Figure 17. ACE1202T/ACE1202R 2-wire connection



13.3 RF RKE system with active/passive transmitter

Using the same 2-wire interface described in Section 13.2, it is possible to build a RKE system that allows the ACE1202T to send information in PWM mode using the RF link or act as a passive key if connected through the 2-wire connection in NRZ mode. The passive functionality could be employed as emergency enable/disable of the system or to program DES information into the ACE1202T user area. In this case, the secret information is not sent through the RF channel.To enable this possibility, pin 1 (LRN) of the ACE1202R must be connected to GND. The system can work with or without a battery on the transmitter battery-holder.

Figure 18. RKE System with 2-wire interface

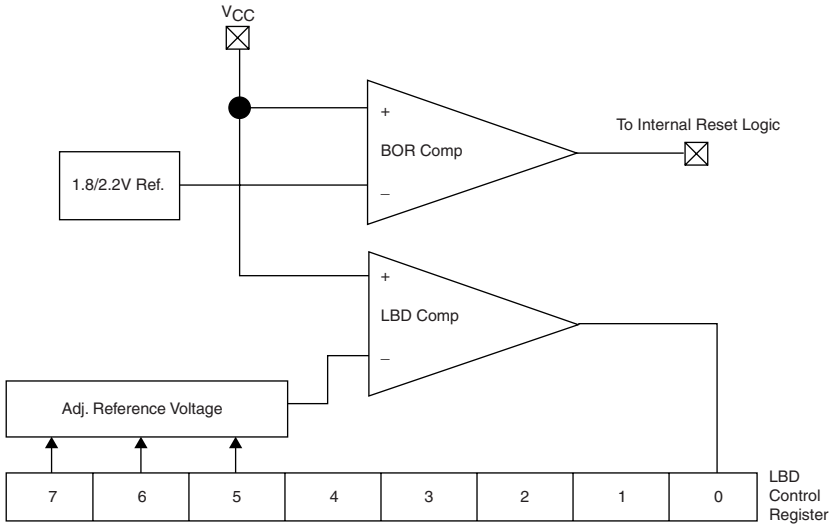


14.0 Brown-out Reset

The Brown-out Reset (BOR) function is a standard feature of the ACE1202 Product Family used to hold the device in reset when Vcc drops below a fixed threshold. (See BOR Electrical Characteristics for threshold voltage.) While in reset, the device is held in its initial condition until V_{CC} rises above the threshold value. Shortly after V_{CC} rises above the threshold value, an internal reset sequence is started. After the reset sequence, the core fetches the first instruction and starts normal operation.

The BOR should be used in situations when V_{CC} rises and falls slowly and in situations when Vcc does not fall to zero before rising back to operating range. The Brown-out Reset can be thought of as a supplement function to the Power-on Reset when V_{CC} does not fall below ~1.5V. The Power-on Reset circuit works best when V_{CC} starts from zero and rises sharply. So in applications where V_{CC} is not constant, the BOR will give added device stability.

Figure 19 BOR/LBD Block Diagram

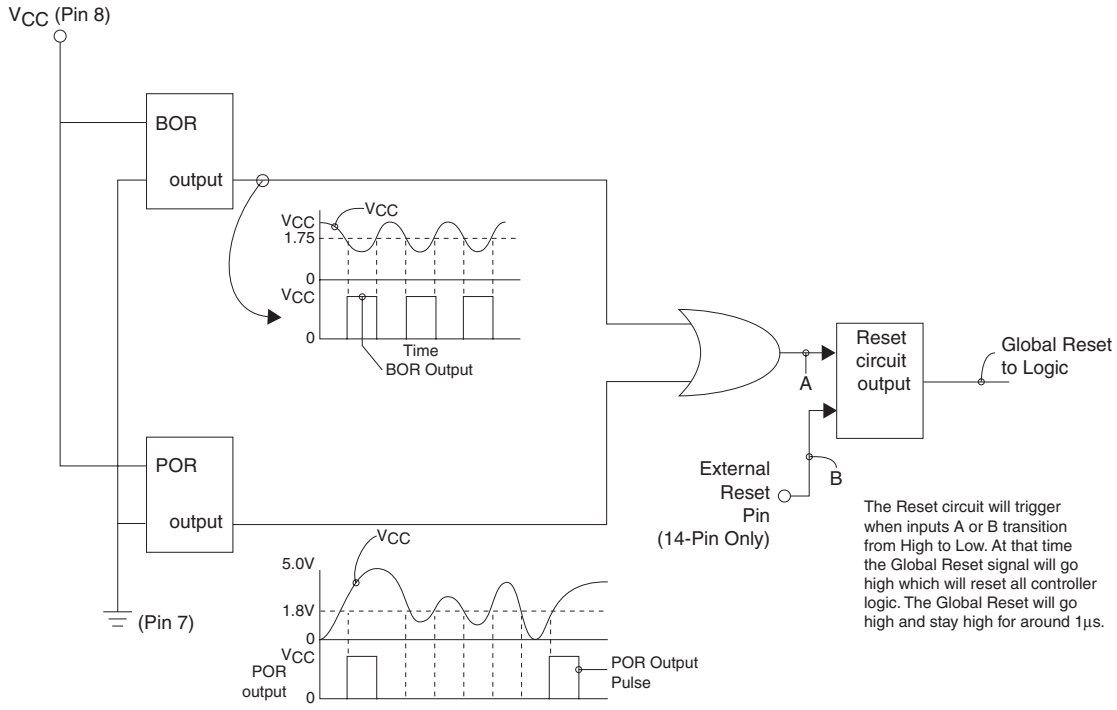


15.0 Power-on Reset

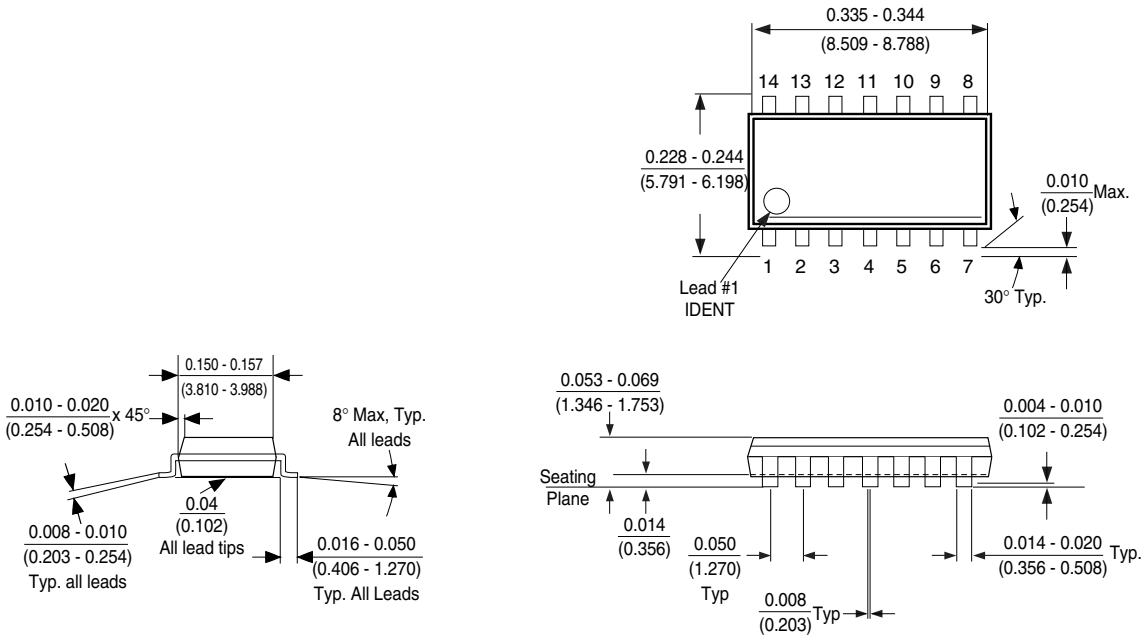
The Power-On Reset (POR) circuit is guaranteed to work if the rate of rise of V_{CC} is no slower than 10ms/1volt. The POR circuit was designed to respond to fast low to high transitions between 0V and V_{CC} . The circuit will not work if V_{CC} does not drop to 0V before the next power-up sequence. In applications where 1) the Vcc rise is slower than 10ms/1 volt or 2) V_{CC} does not drop to 0V before the next power-up sequence the external reset option should be used.

The external reset provides a way to properly reset the ACE1202R if POR cannot be used in the application. The external reset pin contains an internal pull-up resistor. Therefore, to reset the device the RESET pin should be held low for at least 2ms so that the internal clock has enough time to stabilize.

Figure 20 BOR and POR Circuit Relationship Diagram



Physical Dimensions inches (millimeters) unless otherwise noted



Molded Small Outline Package (M)
Order Number ACE1202REM
Package Number M14A

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