

#### **GENERAL DESCRIPTION**

The CMT2301 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

#### **FEATURES**

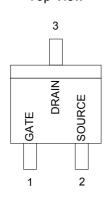
- -20V/-2.3A ,R<sub>DS(ON)</sub>=130 mΩ@VGS=-4.5V
- -20V/-1.9A ,R<sub>DS(ON)</sub>=190 mΩ@VGS=-2.5V
- Super high density cell design for extremely low R<sub>DS(ON)</sub>
- Exceptional on-resistance and maximum DC current capability
- SOT-23-3 package design

## **APPLICATIONS**

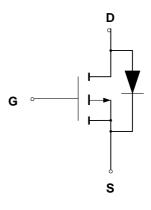
- Power Management in Notebook
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

### **PIN CONFIGURATION**





#### SYMBOL



P-Channel MOSFET

### **ORDERING INFORMATION**

Part Number	Package
CMT2301M233	SOT-23-3
CMT2301GM233*	SOT-23-3

\*Note: G : Suffix for Pb Free Product



### **ABSOLUTE MAXIMUM RATINGS**

Rating			Value	Unit	
Drain- to- Source Voltage		V <sub>DSS</sub>	-20	V	
Gate-to-Source Voltage		V <sub>GSS</sub>	±8	V	
Continuous Drain Current(Tյ=150°C)	T <sub>A</sub> =25℃		-2.5	^	
	T <b></b> , <b>=70</b> ℃	ID	-1.5	A	
Pulsed Drain Current		I <sub>DM</sub>	-10	А	
Continuous Source Current(Diode Conduction)		ls	-1.6	Α	
Power Dissipation	T <sub>A</sub> =25℃		1.25	14/	
	T <sub>A</sub> =70℃	P <sub>D</sub>	0.8	W	
Operating Junction Temperature		TJ	150	°C	
Storage Temperature Range		T <sub>STG</sub>	-55/150	°C	
Thermal Resistance-Junction to Ambient			120	°C/W	

# **ELECTRICAL CHARACTERISTICS**

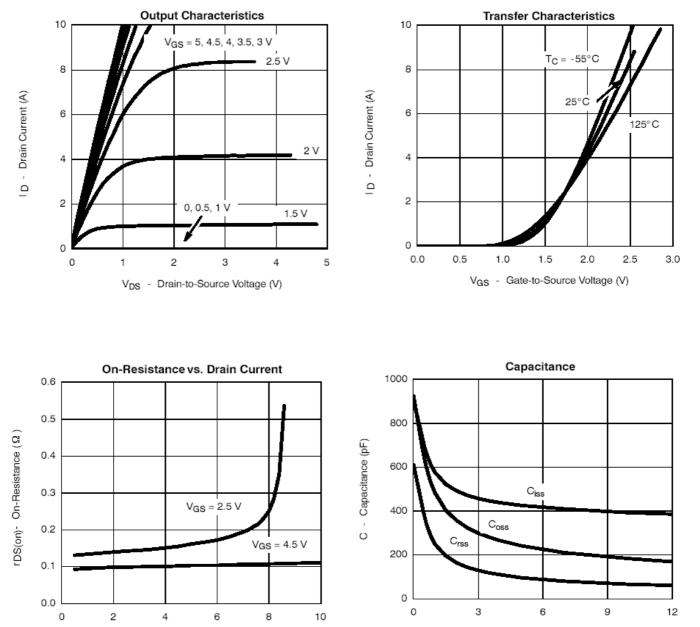
Unless otherwise specified,  $T_{\rm J}$  = 25  $^\circ\!{\rm C}$  .

			CMT2301			
Char	acteristic	Symbol	Min	Тур	Max	Units
Static						
Drain-Source Breakdown Voltage		V <sub>(BR)DSS</sub>	-20			v
$(V_{GS} = 0 \text{ V}, I_D = -250 \mu \text{ A})$		V (BR)DSS				v
Gate Threshold Voltage		$V_{GS(th)}$	-0.45		-1.5	v
$(V_{DS} = V_{GS}, I_D = -250 \mu A)$						v
Gate Leakage Current		I <sub>GSS</sub>			±100	nA
$(V_{DS} = 0 V, V_{GS} = \pm 8 V)$						
Zero Gate Voltage Drain Current						
$(V_{DS} = -20 \text{ V}, V_{GS} = 0 \text{ V})$		I <sub>DSS</sub>			-1	μΑ
$(V_{DS} = -20 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55^{\circ}C)$					-10	
On-State Drain Current						
$(V_{DS} \le -5 V, V_{GS} = -4.5V)$		I <sub>D(on)</sub>	-6			А
$(V_{DS} \le -5 V, V_{GS} = -2.5V)$			-3			
Drain-Source On-Resistance						
$(V_{GS} = -4.5 \text{ V}, I_D = -2.8\text{A})$		R <sub>DS(on)</sub>		0.105	0.13	Ω
(V <sub>GS</sub> = -2.5 V, I <sub>D</sub> = -2.0A)				0.145	0.19	52
Forward Transconductance ( $V_{DS}$ = -5 V, $I_{D}$ = -2.8V)		<b>g</b> fs		6.5		S
Diode Forward Voltage (I <sub>S</sub> =-1.6A,V <sub>GS</sub> =0V)		V <sub>SD</sub>		-0.8	-1.2	V
Dynamic						
Input Capacitance		C <sub>iss</sub>		415		pF
Output Capacitance		C <sub>oss</sub>		223		
Reverse Transfer Capacitance		C <sub>rss</sub>		87		
Turn-On Time		t <sub>d(on)</sub>		13	25	ns
	$(V_{DD} = -6 V, R_L = 6\Omega)$	tr		36	60	
Turn-Off Time	$I_{\rm D}$ = -1.0 A,V <sub>GEN</sub> = -4.5 V, R <sub>G</sub> = 6Ω)	t <sub>d(off)</sub>		42	70	
		tf		34	60	
Total Gate Charge		Qq		5.8	10	nC
Gate-Source Charge	$(V_{DS} = -6 V, I_D = -2.8 A,$	Q <sub>gs</sub>		0.85		
Gate-Drain Charge	V <sub>GS</sub> =-4.5V)	Q <sub>gd</sub>		1.7		



# TYPICAL CHARACTERISTICS

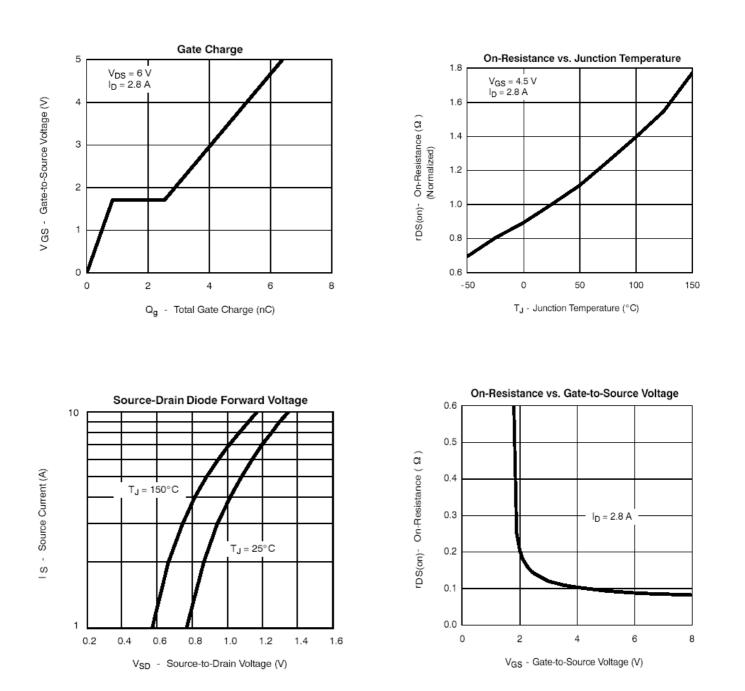
ID - Drain Current (A)



V<sub>DS</sub> - Drain-to-Source Voltage (V)

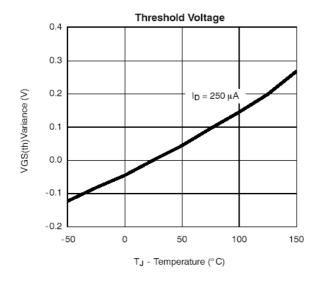


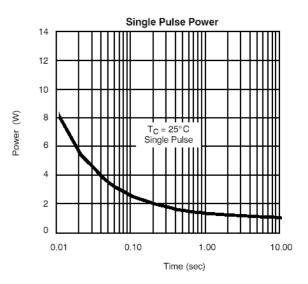
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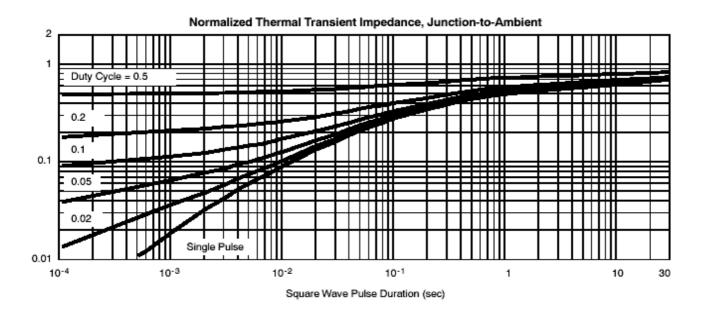




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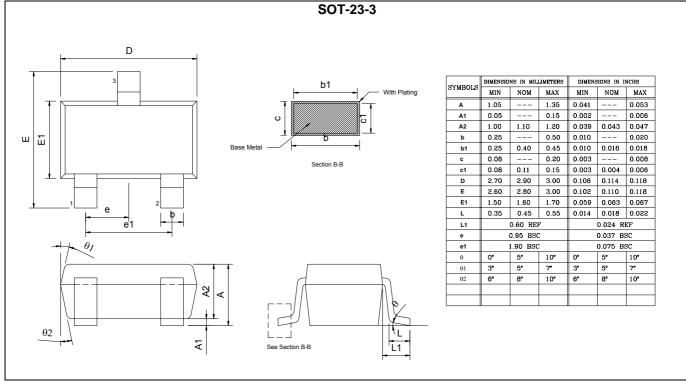








#### PACKAGE DIMENSION





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