QUAD 8 BIT DAC

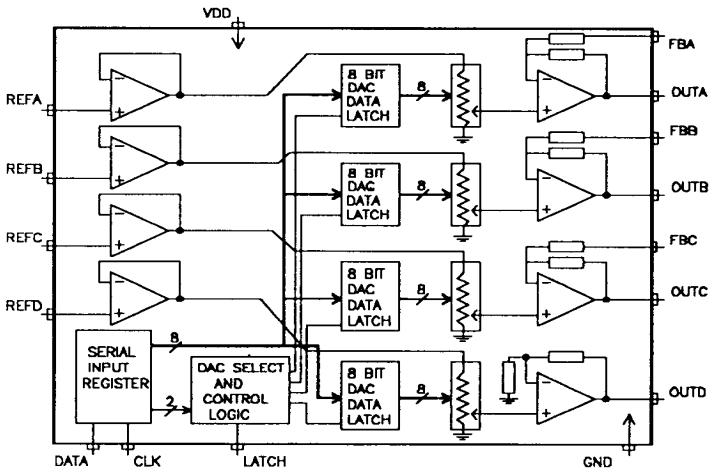
Features

- Four 8 bit D to A converters
- Guaranteed monotonicity
- 3 volt to 10 volt operation
- Microprocessor, TTL, CMOS compatible
- 4 separate voltage reference inputs
- High impedance reference inputs
- Buffered voltage outputs
- Optional x2 buffering for 3 outputs
- Fast settling time (3μs to 0.5 LSB)
- Low power consumption (5mA max)
- Small 16 pin SO (wide bodied) package

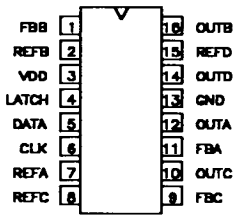
Applications

- Programmable voltage source
- Programmable amplifiers/attenuators
- Telecommunications
- Automatic test equipment
- Industrial Control
- Signal synthesis

Block Diagram



Pin Configuration



Ordering Information

Part	Package
WM8030D	16 pin Plastic DIP
WM8030S	16 pin wide bodied SO

Description

WM8030 is a quad 8 bit voltage output digital to analogue converter (DAC) with buffered reference inputs (high impedance). WM8030 is guaranteed monotonic and is simple to use, running from a single supply of 3V to 10V.

Digital interfacing to the WM8030 is via a simple 3 pin serial interface, and is CMOS/TTL and microprocessor compatible. The 10 bit command word comprises 8 bits of data and a 2 bit DAC select code. The digital inputs feature Schmitt triggers for high noise immunity.

The 16 pin wide bodied small outline (SO) package allows digital control of analogue functions in space critical applications. The WM8030 is characterised over commercial and industrial temperature ranges and does not require external trimming.

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Electrical Characteristics
(VDD = 5V, VREF = 1.25V unless otherwise stated)

Parameter		Min	Typ	Max	Units
Supply Current					
VDD supply current (outputs unloaded	@ VDD = 5V			5.0	mA
	@ VDD = 10V			6.0	mA
DAC Static Performance					
Resolution		8			bits
Monotonicity - Guaranteed					
Total Error (Integral non-linearity)				±1.0	LSB
Relative Error (differential non-linearity)				±0.5	LSB
Full Scale Error				±2.5	LSB
Full Scale Error Temperature Coefficient			30.0		ppm/ °C
Zero Code Error				±1.5	LSB
PSRR			60.0		dB
Reference Input					
Reference Input Range		GND		VDD * 0.4	V
Reference Input Capacitance			15		pF
Digital Inputs					
Input Low (VIL)				1.0	V
Input High (VIH)	(VDD = 5V to 10V)	4			V
Input High (VIH)	(VDD < 5V)	VDD			V
Input Leakage Current				±1	μA
Input Capacitance			15		pF
Dynamic Performance					
Output Slew Rate			2.0		VμS
Output Settling Time (to 0.5LSB, zero to full scale)			3.0		μS
Large Signal Bandwidth (-3dB)			100		kHz
Digital cross talk (CLK 1MHz square wave to VOUT)			-50.0		dB
Output THD (code = all 1's, Vref = 50kHz, 0.5Vpp)			-50.0		dB
Load Capacitance				100	pF
Load Resistance		10			kΩ
Switching Characteristics (see timing diagram)					
Clock Frequency				1	MHz
Data valid to CLK set-up time	(t1)	50			ns
Data valid after CLK hold time	(t2)	50			ns
CLK to LATCH setup time	(t3)	50			ns
LATCH low to CLK high	(t4)	50			ns
LATCH duration low	(t5)	250			ns

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Absolute Maximum Ratings

Supply Voltage (VDD - GND) ..... +11V
Digital Inputs..... GND - 0.3V, VDD + 0.3V
Reference Inputs..... GND - 0.3V, VDD + 0.3V
Operating Temperature..... -25 °C to +85 °C
Storage Temperature..... -50 °C to +150 °C
Lead Temperature (Soldering, 10 sec) ..... +230 °C

Pin	Name	Type	Function
1	FBB	Analogue Input	Gain Select for DACB
2	REFB	Analogue Input	Reference input to DACB
3	VDD	Supply	Positive supply voltage
4	LATCH	Digital Input	Serial Interface Latch
5	DATA	Digital Input	Serial Interface Data
6	CLK	Digital Input	Serial Interface Clock
7	REFA	Analogue Input	Reference input to DACA
8	REFC	Analogue Input	Reference input to DACC
9	FBC	Analogue Input	Gain Select for DACC
10	OUTC	Analogue Output	Buffered output of DACC
11	FBA	Analogue Input	Gain Select for DACA
12	OUTA	Analogue Output	Buffered output of DACA
13	GND	Supply	Ground pin
14	OUTD	Analogue Output	Buffered output of DACD
15	REFD	Analogue Input	Reference input to DACD
16	OUTB	Analogue Output	Buffered output of DACB

Detailed Description

The WM8030 is implemented using four resistor string digital to analogue converters (DACs). The core of each DAC is a single resistor with 256 taps, corresponding to the 256 possible codes. One end of each resistor string is connected to the GND pin and the other end is fed from the output of an input buffer amplifier. Monotonicity is guaranteed by use of the resistor strings. Linearity depends upon the matching of the resistor elements, and upon the performance of the output buffer. Because the inputs are buffered, the DACs always presents a high impedance load to the reference source.

On power-up the DAC's are reset to CODE 0.

Each output voltage is given by:

$$OUT = REF \times \frac{CODE}{256} (x2),$$

where "CODE" is in the range 0 to 255 and the x2 is optional for DACA, DACB and DACC, and always applies to DACD.

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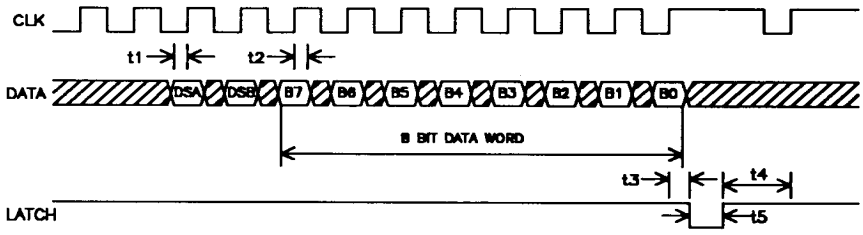
3 Pin Data Interface

With LATCH low, data is clocked into the DATA pin on each rising edge of CLK. Once all data bits have been clocked in, LATCH is pulsed high to transfer the data from the serial input register to the selected DAC. Data is entered MSB first.



DSA	DSB	Selected DAC
0	0	A
0	1	B
1	0	C
1	1	D

Timing Diagram for WM8030

DACs A, B and C feature a configurable output buffer. By leaving the feedback pin (FBA, FBB, FBC) disconnected the output amplifier acts as a unity gain buffer. Connecting the feeback pin to ground, on the other hand, configures the amplifier as a x2 gain stage. The output buffer of DACD is not programmable, and is configured as a x2 gain stage.

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