General-Purpose SDRAM Controller

SDRAM Controller Functional Description

The general-purpose SDRAM controller is designed to provide simplified control of many different sizes of SDRAMs. The controller architecture provides control for data bursts by linearly incrementing the address. The user starts a burst at a specified address and the burst continues until the user terminates it.

SDRAM Controller Signals

The SDRAM controller communicates with a user's functions and drives the control signals into the SDRAM. When the controller recognizes the start of a write cycle, the controller prepares the SDRAM to accept data and then indicates readiness by driving the WR_BE_RDY signal. When the controller recognizes the start of a read cycle, the controller prepares the SDRAM to provide data and then indicates readiness by driving the RD_BE_RDY signal.

The WR_BE_RDY and RD_BE_RDY signals are one-stage pipelined. On write cycles, the WR_BE_RDY signal is asserted one clock cycle prior to the time when data can actually be accepted by the SDRAM. On read cycles, the RD_BE_RDY signal is asserted one clock cycle prior to the time when SDRAM data is valid. In general, the *_RDY signals indicate that the SDRAM and controller will ready for data transfer on the next cycle.

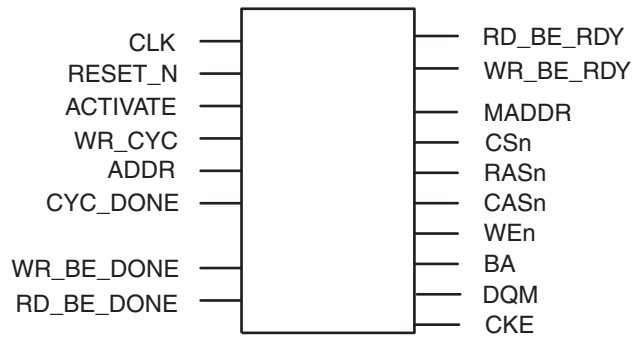

Figure 1 • *SDRAM Controller*

The user provides a WR_BE_NOW and RD_BE_NOW signal to the controller. When WR_BE_RDY and WR_BE_NOW are both asserted at the same time, or when RD_BE_RDY and RD_BE_NOW are both asserted at the same time, data is transferred. If the WR_BE_NOW signal is not asserted, the controller will retain its current address until the WR_BE_NOW signal asserts at which time data is transferred. Because of the pipelined nature of the SDRAM and the assumption that burst addresses are incremented linearly, a deassertion of RD_BE_NOW causes delay while the controller backs up and refills the pipeline.

At the conclusion of a cycle, the user asserts the CYCLE_DONE signal for one cycle.

Table 1 • *SDRAM Controller Signals*

Name	Description
Inputs from the User's System	
Clk	This is the system clock. The controller can transfer data at this rate during bursts.
RESETn	This is a reset signal. Assertion of this signal causes the SDRAM to be initialized.
ACTIVATE	A pulse on this signal causes the Controller to prepare the SDRAM for a cycle.
WR_CYC	This signal defines the type of cycle started when the ACTIVE (ACTIVATE?) signal is asserted.
ADDR(M:0)	This is the beginning address of the burst.
CYC_DONE	This signal causes the cycle to be terminated.
WR_BE_NOW	This signal indicates that the user wants the currently valid data to be written.
RD_BE_NOW	This signal indicates that the user will accept the data on this cycle.
Outputs to the User's System	

Table 1 • SDRAM Controller Signals

Name	Description
WR_BE_RDY	This signal indicates that the controller has readied the SDRAM for (to receive/accept?) data on the following cycle. These signals are pipelined to give the user 1 clock cycle advanced warning of the SDRAM's readiness to accept data.
RD_BE_RDY	This signal indicates that the controller has readied the SDRAM to deliver data to the system on the following cycle. These signals are pipelined to give the user 1 clock cycle advanced warning of the SDRAM's readiness to deliver data.
Outputs to the SDRAM	
CS0n	Chip Select for low bank.
CS1n	Chip Select for upper (optional) bank.
RASn	This is the Ras signal.
CASn	This is the Cas signal.
WEn	This is the We signal.
BA0	This is the Bank 0 bit signal.
BA1	This is the Bank 1 (if used) signal.
MADDR(N:0)	This is the multiplexed RAS / CAS address bus.
DQM	This is the Data mask signal.
CKE	This is the Clock enable signal.

SDRAM Controller SDRAM Signal Function

The Controller connects to the SDRAM as expected. The CASn, RASn, and WEn signals connect as expected. The DQM signal from the controller may need to be connected to multiple DQM lines depending on the width of SDRAM being used. There are two CSn lines: CS0N and CS1n. The assumption is that a user may want two banks (twice as much address space) of SDRAMs. The CS0n then drives the lower bank and the CS1n signal drives the upper bank of SDRAMs. If only one bank is desired, connect the CS0n line and leave the CS1n line unconnected. Some SDRAMS have only two banks and require only one BA line. Most SDRAMS have four banks and require two BA lines. When using a small SDRAM, leave the BA1 line disconnected.

SDRAM Configurations for Various Sizes of SDRAMS

Inside the SDRAM Controller HDL code file are constants or generic statements that allow the use of various sizes of SDRAMs. The following constants or generics are included - COL_WIDTH, ROW_WIDTH, BANK BITS AND CHIP BITS. These constants configure the controller to fit a particular SDRAM. COL_WIDTH defines the number of address bits required to address all of the columns in the SDRAM. ROW_WIDTH defines the number of address bits required to address all of the rows in the SDRAM. The bank bits are the address bits required to address the banks in the SDRAM. The CHIP_BITS are the bits required to address the number of banks in the SDRAM.

A typical application would be interfacing with one bank of MT48??? SDRAMs. This is a 2Mx32x4banks SDRAM and the settings are as follows:

- ROW_WIDTH = 11
- COL_WIDTH = 8
- BANK BITS = 2
- CHIP_BITS = 0

Testbench

The test bench is defined in the system.vhd file and is comprised of the following elements:

- The SDRAM controller
- A model of a Micron SDRAM
- A test vector generator

The testbench causes the SDRAM controller to write and then read/verify linear bursts of ten addresses to/from various places in memory. During the first read write burst (from time 100 us to 108 us), three bursts are written and then read/verified. During these first bursts, RD/WR_BE_NOW are always asserted.

From time 116us to 118us, a read burst and a write burst are executed with minimal deassertion of RD/WR_BE_NOW. These bursts are designed to demonstrate the operation of

the SDRAM controller when simple deassertion of RD/WR_BE_NOW occurs.

From time 120us to 148us, the RD/WR_BE_NOW signals are driven by a pseudo-random bit stream and vectors are targeted to cause page crossings for a very complete testing of the MiniCore.

To run the simulation:

1. Unzip the SDRAM MiniCore zip file,
2. Start MTI,
3. In MTI, File->change directory "designs/SDRAM/testbench/mti"
4. In MTI, macro->execute macro "comp.do"

Functional Waveforms

Figure 2 and Figure 3 are functional waveforms for read and write. They represent key events. For more detailed events, run the testbench and view simulation signals. Figure 2 is a write cycle. Significant events are as follows:

1. At clock 2, ACTIVE, ADDR and WR_CYC from the user ask the SDRAM controller to prepare the SDRAM for a write.
2. At clock 4, the SDRAM controller asserts WR_BE_NOW indicating that at cycle 5, the SDRAM will be ready to accept data.
3. The user is not ready to transfer data until clock 8.
4. Data is written into the SDRAM on clocks 8 through 15 except 12 (WR_BE_NOW not asserted during that cycle).
5. The cycle ends at clock16.

Figure 3, the Read cycle is much like the write cycle except because of the pipelined nature of an SDRAM. Any time the user de-asserts the WR_BE_NOW as shown in cycle 5, the SDRAM controller will become not ready for several clocks while it reloads the SDRAM data output pipeline.

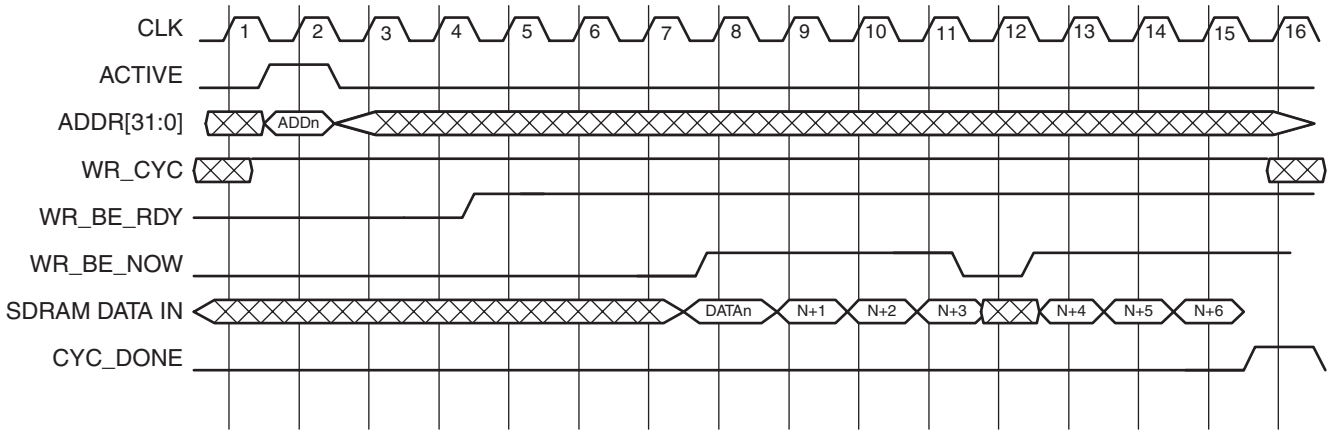

***Figure 2** • Write Cycle*

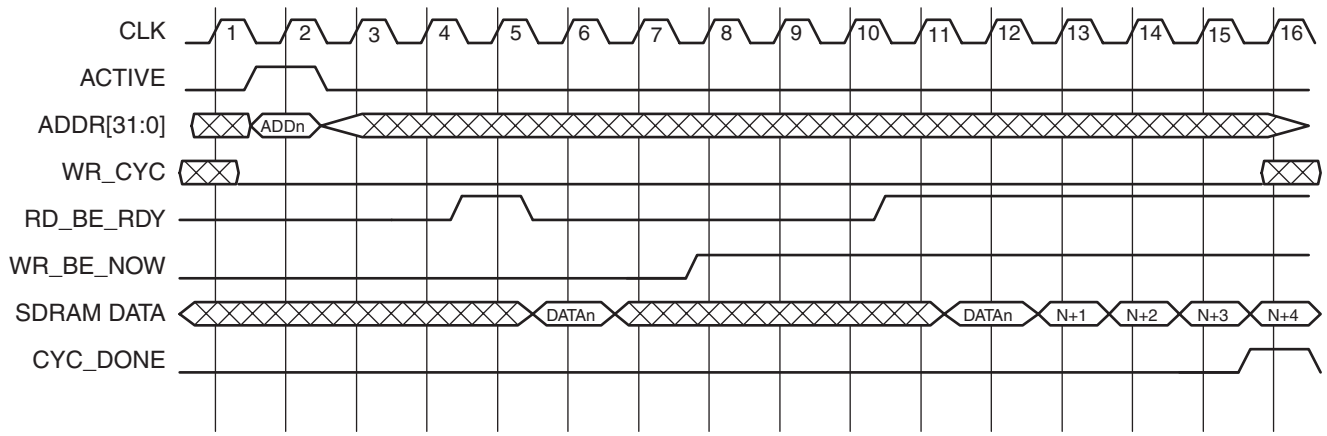

***Figure 3** • Read Cycle*

Timing and Utilization

The SDRAM controller will function at over 100 Mhz when synthesized into SX –3 silicon. Table 2 and Table 3 are some tables for several parts. Other more-specific timing information can be derived by using the DirecTime analysis tools or by looking at the .adf file in the SDRAM controller files.

Table 2 •

Part	Tsu	Treg-reg	Tco	Seq count	Comb count
54SX08A-3	6.3	6.9	5.7	90/256 34%	204/512 40%
54SX08-std	9.5	10.5	9.0	90	211

Table 3 •

Tsu	SX-3
ACTIVATE	5.2
WR_CYC	6.4
AD	2.8
CYC_DONE	6.3
WR_BE_NOW	4.8
RD_BE_NOW	5.9
CS0N	3.3
CS1N	4.0
RASN	2.8
CASN	2.8
WEN	3.0
MADDR	5.6
DQM	4.5
WR_BE_RDY	5.7
RD_BE_RDY	5.6

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