T-52-19-00

GA1210E

Low-Skew TTL Clock Doubler Two-Phase Clock Generator

gazelle

General Description

Gazelle's GA1210E is a low-skew TTL-level clock doubler chip. It produces multiple clock outputs, at precisely 2X the input frequency, which are all phase-aligned to a periodic clock input signal. The GA1210E can generate clocks up to 100 MHz, making it an ideal solution for high-speed clock generation and routing.

The GA1210E guarantees precise clock control. The delay through the part is typically ±250 ps. Skew at all six outputs is maintained to ± 250 ps., typically. When used with Gazelle's GA1110E multi-phase low-skew buffer, a complete system clocking solution can be achieved.

The capability to double clock signals while maintaining tight control over the phase and frequency of the output clocks is accomplished with the use of a 500 MHz internal phase-locked loop (PLL). By feeding back one of the 1X frequency output clocks (to FBIN), the on-chip PLL can continuously maintain synchronization between the input clock (CLKIN) and all six outputs. Any drift or variation in the system clock will be matched and tracked at the six outputs of the GA1210E.

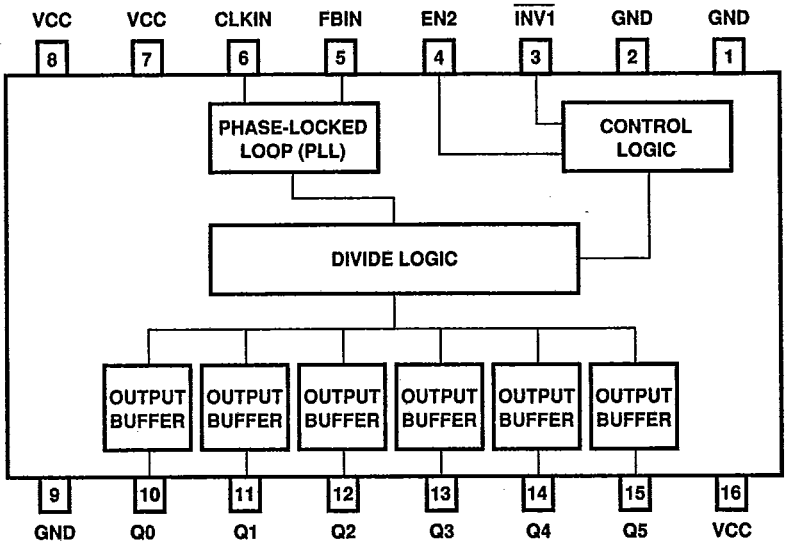
The GA1210E offers several different configurations to accommodate the designer's high-speed clocking requirements. In addition to providing 2X outputs at 50-100 MHz frequencies, the GA1210E can also be configured to generate non-overlapping two-phase clocks. The combination of high speed and a selectable two-phase capability makes it ideal for clocking state machine and pipeline logic.

The GA1110E is fabricated using Gazelle's One-Up™ gallium arsenide technology to achieve precise timing control and guarantee 100% TTL-compatibility. The 25, 33, 40 and 50 MHz input frequencies make them ideal for high-speed clock generation and skew control in high-performance RISC- and CISC-based systems.

Features

- 2X Clock Multiple Generator
  - — Generates high-frequency clocks
  - — Allows backplane clock routing at 1/2 or 1/4 frequencies
  - — Phase control synchronizes all frequencies in phase
- Two-Phase Clock Generator
  - — Ideal for pipelined or two-phase logic structures
  - — Runs at double the input frequency
- Zero-propagation delay
  - — Delay from input to output ±250 ps. (typ), ±1 ns (max)
- Output skew controlled to ± 250 ps. (typ), ± 500 ps. (max)
  - — Allows precisely-controlled system clocking
  - — Ideal for low-skew clock fanout
- Available in 25, 33, 40 and 50 MHz versions
  - — Compatible with high-performance microprocessors
  - — System speed upgrades can use the same clock scheme
- High-drive, symmetric TTL-compatible outputs
  - — Ioh = -24 mA, Iol = 24 mA
  - — Outputs may be combined for even greater drive
- Fully TTL-compatible inputs and outputs
  - — Reduced voltage swing minimizes noise and skew
  - — No ECL voltage translators needed
- Self-contained on-board 500 MHz phase-locked loop (PLL)
  - — No external filter components required
  - — Digitally guaranteed timing control
- Single (+5V) power supply
- Commercially proven gallium arsenide technology
  - — Allows for precise phase adjustment and control
- 120 mA operating current (typ.), 160 mA (max)
- Standard 16-pin DIP package
  - — Call factory for surface mount availability

Block Diagram



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Functional Description

The GA1210E TTL-level clock doubler and two-phase generator chip is capable of generating multiple 2X outputs from a periodic clock input. Two control pins, EN2 and INV1, provide additional flexibility by selecting two-phase and inverted clocks, respectively.

Table 1 below enumerates the four available sets of output clock configurations generated by the GA1210E. The first two columns represent the signal levels for the two control signals. EN2 is an active-HIGH signal which enables the two-phase clocking on outputs Q4 and Q5. INV1 is an active-LOW signal which inverts the Q1 output to provide a $\overline{1X}$ clock output. The following six columns specify the resulting waveforms on each output; they are pictured in detail on the following page. Specifications for the phase and skew parameters associated with the output clocks are listed in the AC Specifications on page 7.

The GA1210E's primary function is to offer precisely phase-aligned, low-skew 2X versions of the CLKIN input. Since the 2X clocks are all synchronous to the input, high-frequency clocks can be generated locally. This relieves the difficulty of routing high-frequency clocks on a board or across a backplane. They can also be cascaded with other GA1210E devices to generate synchronous 4X clocks.

The GA1210E also has the capability to generate non-overlapping two-phase clocks. By setting the EN2 pin HIGH, two-phase clocks are generated at outputs Q4 and Q5. This is ideal for state machines and other logic structures which can be optimized through two-phase clocking. The two-phase clocks are synchronous to the remaining outputs at 1X and 2X frequencies, providing maximum flexibility in board and system level clocking solutions.

In all configurations, the 1X clock must be fed back, either directly or indirectly, to the FBIN input enabling the on-chip PLL to maintain phase and frequency synchronization.

Multiple-Chip Applications

Because of the tight input-output phase control, the GA1210E can be easily cascaded to build low-skew clock chains and clock trees. The generation and distribution of high-speed clocks can be accomplished with minimal skew allowance, permitting the system designer to obtain maximum performance from the microprocessor and other high-speed circuits in their designs. When combined with Gazelle's GA1110E low-skew, multi-phase clock buffer, a complete system clocking solution can be achieved.

(Note the applications examples on pages 4 and 5).

Breaking the Feedback Loop

There is no requirement that the external feedback connection be a direct hardwire from an output pin to the FBIN pin. So long as the signal at FBIN is derived directly from the Q0 output pin and maintains its frequency, additional logic incorporating any delay whatsoever can be accommodated. The internal phase-locked loop will adjust the output clocks on the GA1210E to ensure continuous phase alignment between the FBIN and CLKIN signals.

This feature is extremely valuable in synchronizing ASICs to the system clock.

Caution:

The signal at FBIN must be continuous (i.e. not a gated or conditional signal), and must be derived directly from one of the GA1210E's 1X outputs.

Power-Up/Reset Synchronization

The GA1210E utilizes on-chip phase-locked loop technology to maintain synchronization between inputs and outputs. Whenever the device is powered up, or the system clock (CLKIN) is reset, the phase-locked loop requires a synchronization time (t_{SYNC}) before lock is achieved. The maximum time required is specified in the AC specification table on page 7.

For lock to occur, the Q0 output must always be connected (either directly or through additional ICs) to the FBIN input.

Configuration Table

EN2	$\overline{INV1}$	Q0	Q1	Q2	Q3	Q4	Q5
0	0	1X	$\overline{1X}$	2X	2X	2X	2X
0	1	1X	1X	2X	2X	2X	2X
1	0	1X	$\overline{1X}$	2X	2X	ϕ1	ϕ2
1	1	1X	1X	2X	2X	ϕ1	ϕ2

Notes:
1. 1X: The output clock is a phase-aligned 1X copy of the CLKIN signal
2. $\overline{1X}$: The output clock is a 1X copy of CLKIN, 180° out pf phase (i.e., inverted).
3. 2X: The output clock is a phase-aligned, 2X frequency of the CLKIN signal.
4. ϕ1,ϕ2: The outputs are the first and second of two phases, synchronous to CLKIN.
5. See the configuration waveforms on page 3.

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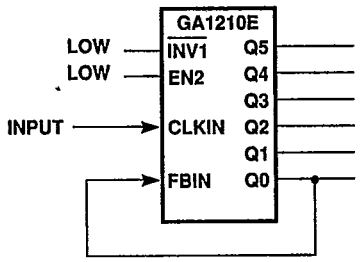
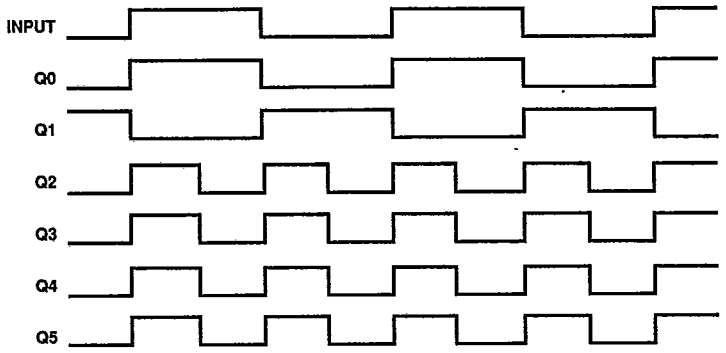
Configuration Examples

1

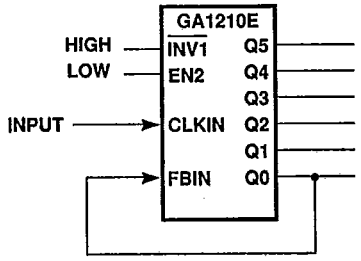
EN2 = 0 $\overline{INV1}$ = 0
FBIN = Q0

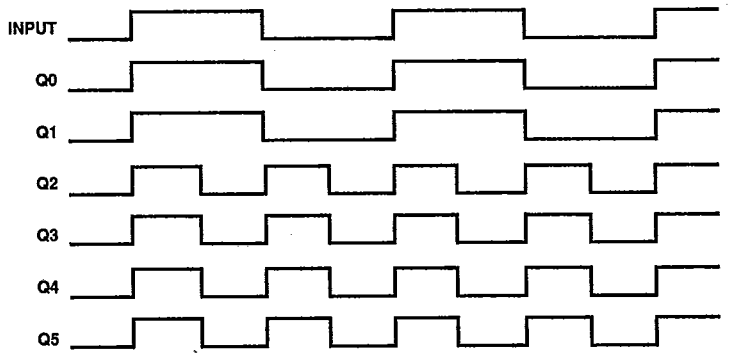




2

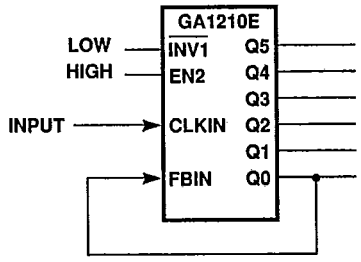
EN2 = 0 $\overline{INV1}$ = 1
FBIN = Q0

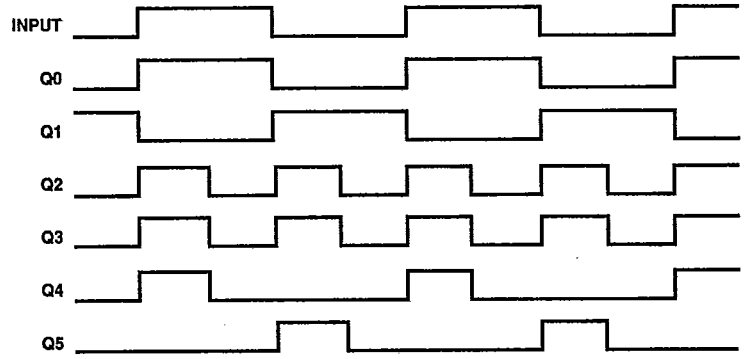




3

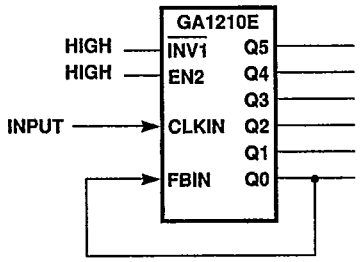
EN2 = 1 $\overline{INV1}$ = 0
FBIN = Q0

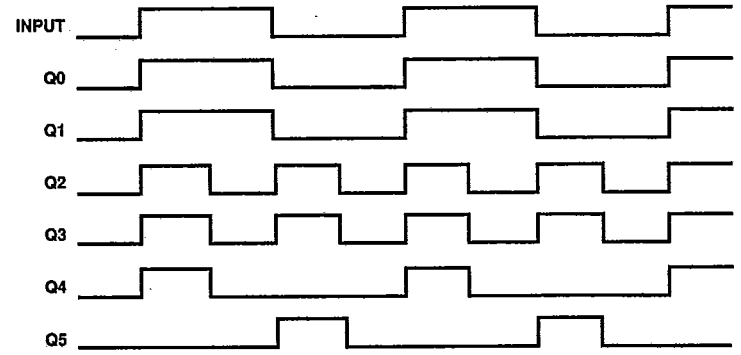




4

EN2 = 1 $\overline{INV1}$ = 1
FBIN = Q0





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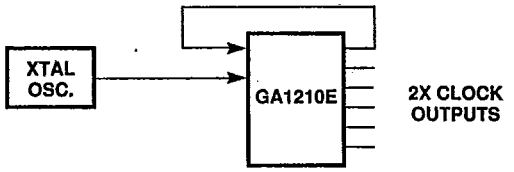
Typical Applications

The GA1210E is designed to satisfy a wide range of system clocking requirements. It provides an ideal companion to the GA1110E multi-phase clock generator. Several application examples are illustrated below.

1) High-Frequency Low-Skew Clock Generation

The GA1210E's basic capability is the generation of multiple, phase-aligned, low-skew clocks at 2X the input frequency.

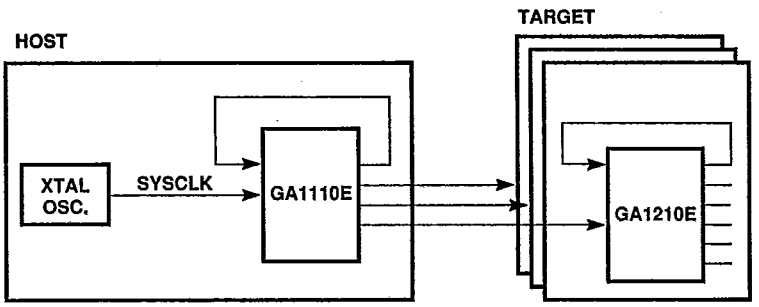
- The GA1210E guarantees low skew among all clocks in the system by controlling both the input-to-output delay, as well as the skew among all six clock outputs.



2) Board-to-Board Clock Synchronization

Many computing systems today consist of multiple boards and cards designed to run synchronously. The skew associated with routing clocks across a backplane presents a major hurdle to maximizing system performance.

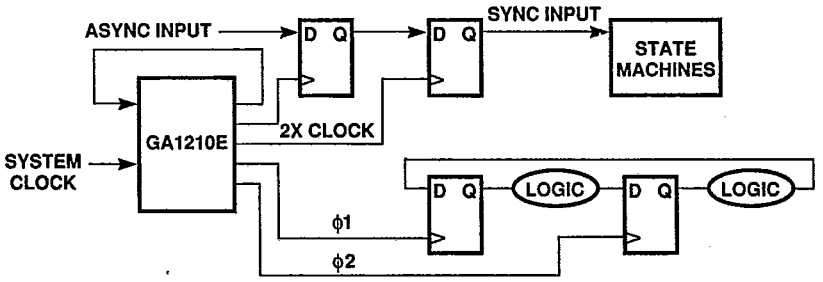
- The tightly-controlled input/output delay of the GA1210E ensures all boards in the system are running synchronously.
- The GA1210E can be used with the GA1110E low-skew buffer to route lower-frequency clocks across a backplane; the low-frequency signal is then doubled on the target boards, enabling them to run synchronously with the host board.



3) Two-Phase Clocking

The GA1210E can be configured to generate synchronous two-phase clocks.

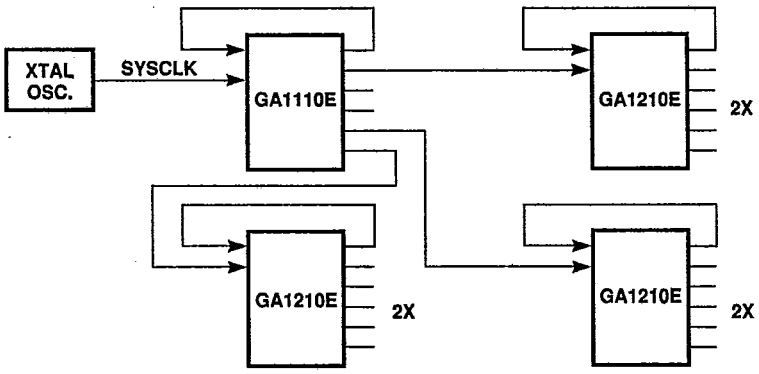
- The two-phase clocks can be used for pipelined logic forms.
- Synchronous two-phase clocks can be used to eliminate metastability concerns by synchronizing asynchronous system inputs to the system clock.



4) Clock Trees and Clock Chains

Used alone or with the GA1110E, the GA1210E is an integral part of distributing multiple copies of high-frequency clocks to the various blocks of a system. All of the clock signals at all of the destinations will run synchronously.

- The controlled input-to-output delay allows long clock chains and trees to be built for clock fanout, with minimal skew among all destinations.



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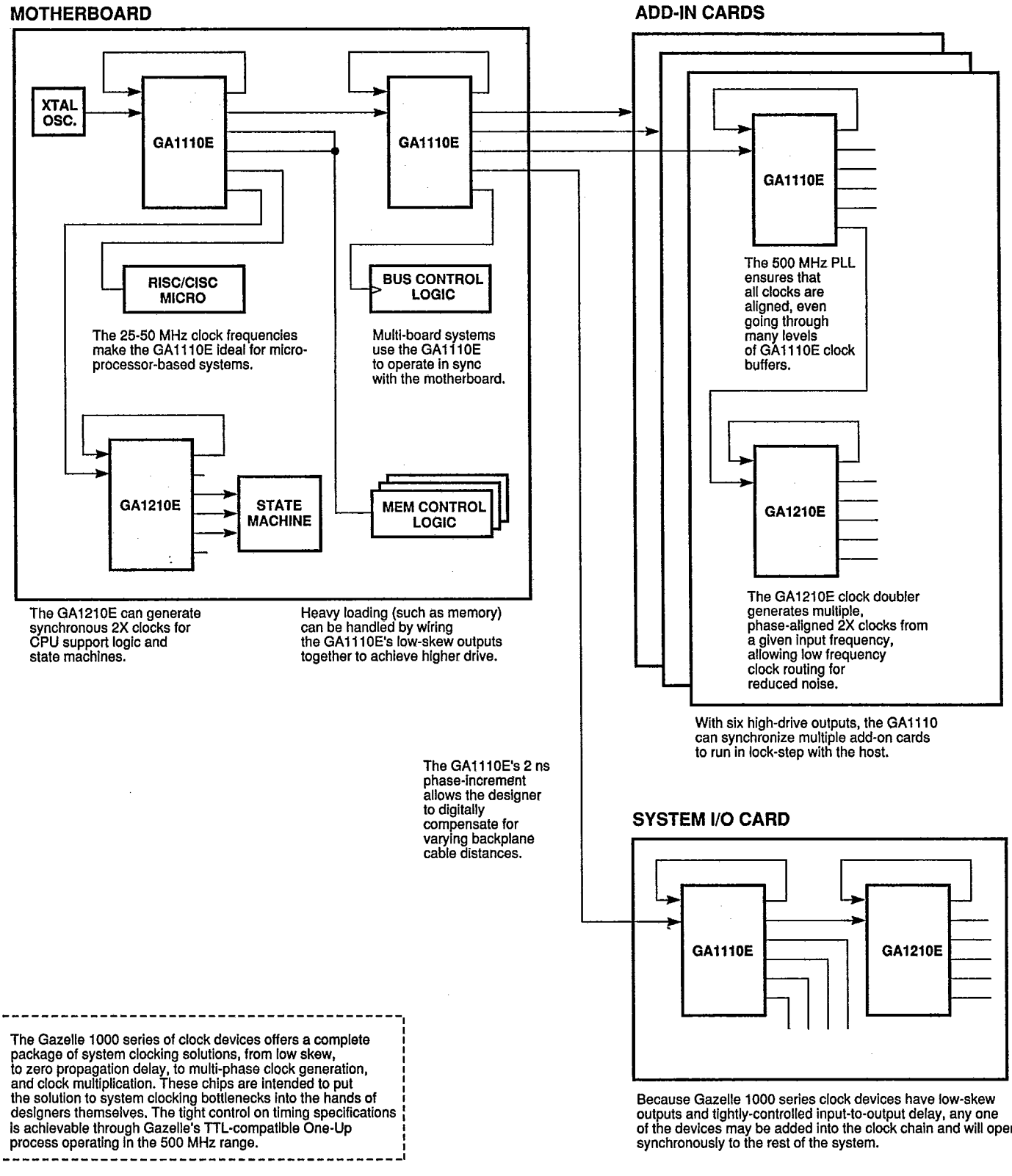
System Clocking Solution



The 25-50 MHz clock frequencies make the GA1110E ideal for micro-processor-based systems.

Multi-board systems use the GA1110E to operate in sync with the motherboard.

The 500 MHz PLL ensures that all clocks are aligned, even going through many levels of GA1110E clock buffers.

The GA1210E can generate synchronous 2X clocks for CPU support logic and state machines.

Heavy loading (such as memory) can be handled by wiring the GA1110E's low-skew outputs together to achieve higher drive.

The GA1210E clock doubler generates multiple, phase-aligned 2X clocks from a given input frequency, allowing low frequency clock routing for reduced noise.

With six high-drive outputs, the GA1110 can synchronize multiple add-on cards to run in lock-step with the host.

The GA1110E's 2 ns phase-increment allows the designer to digitally compensate for varying backplane cable distances.

Because Gazelle 1000 series clock devices have low-skew outputs and tightly-controlled input-to-output delay, any one of the devices may be added into the clock chain and will operate synchronously to the rest of the system.

The Gazelle 1000 series of clock devices offers a complete package of system clocking solutions, from low skew, to zero propagation delay, to multi-phase clock generation, and clock multiplication. These chips are intended to put the solution to system clocking bottlenecks into the hands of designers themselves. The tight control on timing specifications is achievable through Gazelle's TTL-compatible One-Up process operating in the 500 MHz range.

Absolute Maximum Ratings

Storage temperature	-65°C to +150°C
Ambient temperature with power applied	-55°C to +125°C
Supply voltage to ground potential	-0.5 V to +7.0 V
DC input voltage	-0.5 V to +(V_{CC} + 0.5)
DC input current	-30 mA to +5 mA

Operating Range

Ambient temperature (at thermal equilibrium) ..... 0°C to +70°C

Supply voltage ..... +4.75 to +5.25V

The operating range defines those limits within which the functionality of the device to specification is guaranteed.

DC Characteristics over operating range unless otherwise specified

SYMBOL	DESCRIPTION	TEST CONDITIONS	LIMITS[1] MIN	TYP	MAX	UNIT
V_{OH}	Output HIGH voltage	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}, I_{OH} = -24 mA	2.4	3.2		V
V_{OL}	Output LOW voltage	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}, I_{OL} = 24 mA		0.3	0.5	V
V_{IH}[2]	Input HIGH level	Guaranteed input logical HIGH Voltage for all Inputs	2.0			V
V_{IL}[2]	Input LOW level	Guaranteed input logical LOW Voltage for all inputs			0.8	V
I_{IL}	Input LOW current	V_{CC} = Max, V_{IN} = 0.40 V		-150	-400	µA
I_{IH}	Input HIGH current	V_{CC} = Max, V_{IN} = 2.7 V			25	µA
I_I	Input HIGH current	V_{CC} = Max, V_{IN} = 5.5 V			1	mA
I_{SC}[3]	Output short-circuit current	V_{CC} = Max, V_{OUT} = 0.5 V		-110		mA
I_{CC}	Power supply current	V_{CC} = Max		120	160	mA
V_I	Input clamp voltage	V_{CC} = Min, I_{IN} = -18mA			-1.2	V
I_{OLD}	Dynamic switching current	V_{CC} = Max, V_{OLD} = 1.5 V		100		µA
I_{OHD}		V_{CC} = Max, V_{OHD} = 1.5 V		-100		µA

Capacitance[4]

SYMBOL	DESCRIPTION	TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{IN}	Input capacitance	V_{IN} = 2.0 V at f = 1 MHz		6		pF
C_{OUT}	Output capacitance	V_{OUT} = 2.0 V at f = 1 MHz		9		pF

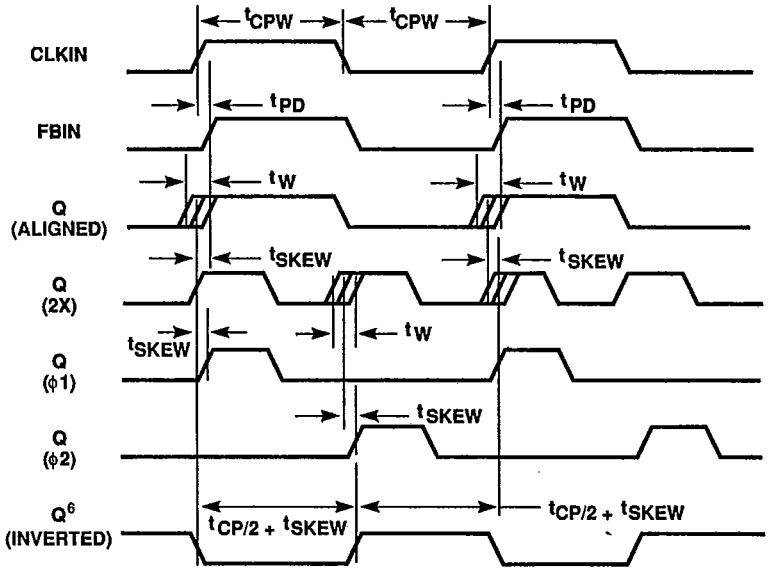
Notes: 1. Typical limits are at V_{CC} = 5.0 V and T_A = 25°C.
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3. No more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} has been chosen to avoid test problems caused by tester ground degradation.
4. These parameters are not 100% tested, but are periodically sampled.

AC Specifications across the operating range

		-50			-40			-33			-25			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
F_{IN}	CLKIN frequency	49	50	51	39	40	41	32	33	34	24	25	26	MHz
t_{CP}	CLKIN period	—	20	—	—	25	—	—	30	—	—	40	—	ns
t_{CPW}	CLKIN pulse width	5	10	—	6.25	12.5	—	7.5	15	—	10	20	—	ns
	Input rise/fall time	—	1.5	3	—	1.5	3	—	1.5	3	—	1.5	3	ns
	Output rise/fall time	—	1.5	—	—	1.5	—	—	1.5	—	—	1.5	—	ns
t_{PD}	CLKIN ↑ to FBIN ↑[1]	—	±250	±1000	—	±250	±1000	—	±250	±1000	—	±250	±1000	ps
t_{SKEW}	Output skew[2]	—	±250	±500	—	±250	±500	—	±250	±500	—	±250	±500	ps
t_W	Output window[3]	—	0.5	1.0	—	0.5	1.0	—	0.5	1.0	—	0.5	1.0	ns
t_{CYC}	Duty-cycle variation[4]	—	1.0	—	—	1.0	—	—	1.0	—	—	1.0	—	ns
t_{SYNC}	Synchronization time[5]	—	200	500	—	200	500	—	200	500	—	200	500	µs

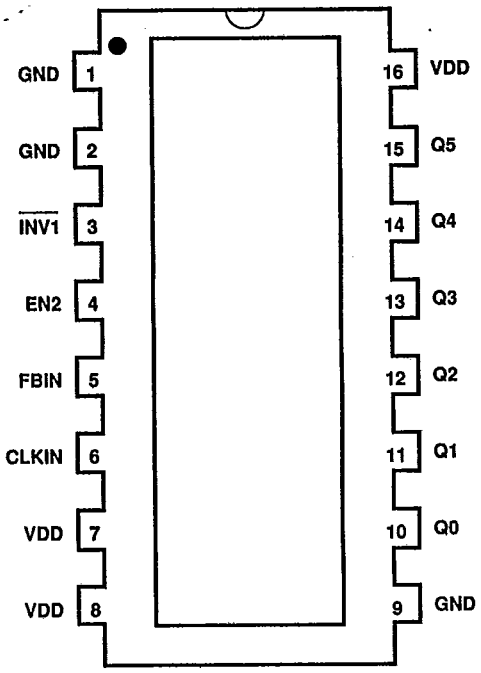
Note: All AC specifications are measured with a 75Ω transmission line load terminated with 75Ω to 1.5 V. The skew specifications are guaranteed for equal loading at each output.

Switching Waveforms



Notes:
1. The PLL maintains alignment of CLKIN and FBIN at all times. This specification applies to the rising edge only because the input duty-cycle can vary while the output duty cycle is typically 50/50.
2. The output skew is measured from the middle of the output window (see Note 3). The maximum skew is guaranteed across all parts, voltages, and temperatures.
3. t_W specifies the width of the window in which all outputs will switch.
4. This specification represents the deviation from 50/50 on the outputs; it is sampled periodically but is not guaranteed.
5. t_{SYNC} is the time required for the PLL to synchronize; this assumes the presence of a CLKIN signal and a connection from one of the outputs to FBIN.
6. All specifications for inverted outputs apply to the rising edges only.

Pinout



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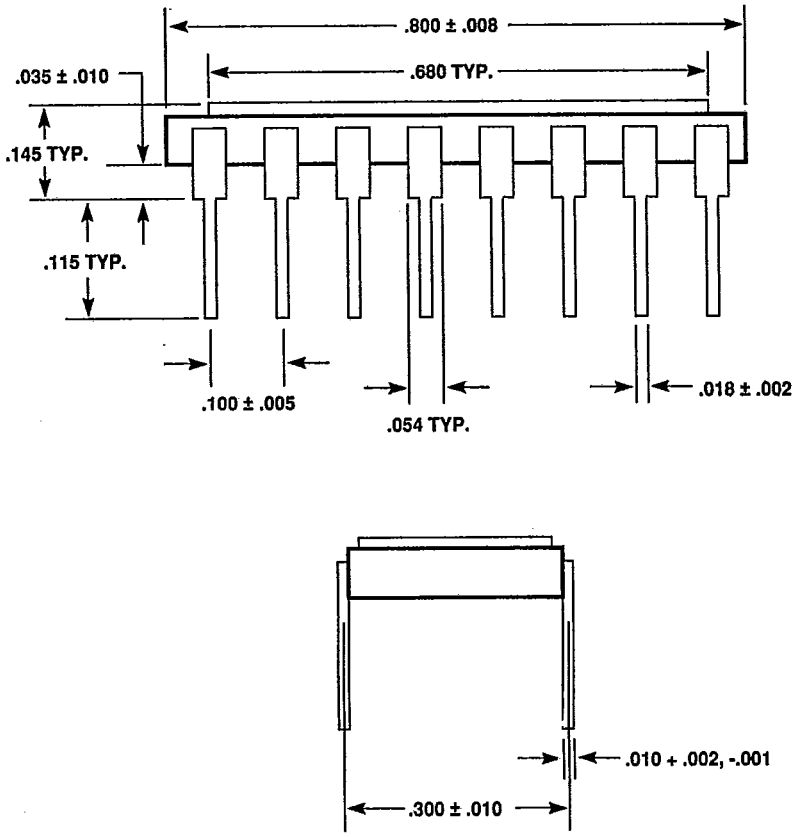
Mechanical Specifications



(All dimensions are in inches)

Ordering Information

GA1210E -

Input Frequency
- -25 - 25 MHz input
- -33 - 33 MHz input
- -40 - 40 MHz input
- -50 - 50 MHz input

Package
- S - 16-pin DIP (side-brazed)
- (Consult factory for surface mount availability)

Temperature
- C - Commercial

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