1 to 4 Demultiplexer GaAs IC for Optical Transmission

The PHS6903 is a 1 to 4 Demultiplexer GaAs IC for Optical Transmission systems.

Features

- 1 to 4 Demultiplexer with on-chip clock synchronization circuitry
- Clock input 2.4 GHz
- ECL compatible I/O's
- Single Power Supply of –5.2 V
- 32 pin package containing internal decoupling capacitors

Absolute Maximum Ratings

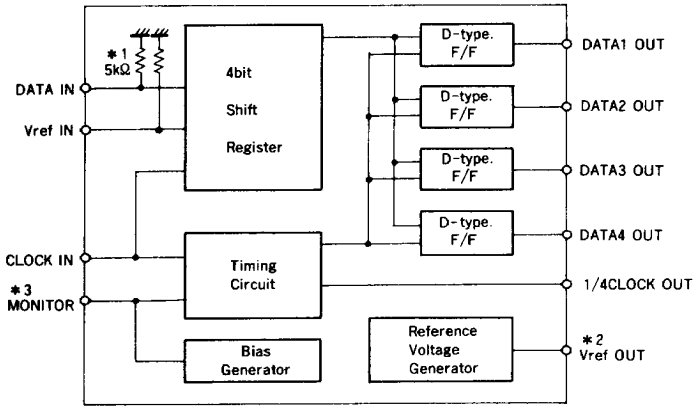
Item	Symbol	Ratings	Unit	Remarks
Supply Voltage	Vss (+)	+0.5	V	
	Vss (–)	–7.0		
Input Voltage	V_{IH}	0	V	
	V_{IL}	Vss		
Supply Current	Iss	500	mA	
Output Current	Io	50	mA	
Power Dissipation	P_D	2.5	W	
Operating Tenparature	Ta	–10 to +80	°C	
Storage Temparature	Tstg	–65 to +150	°C	

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

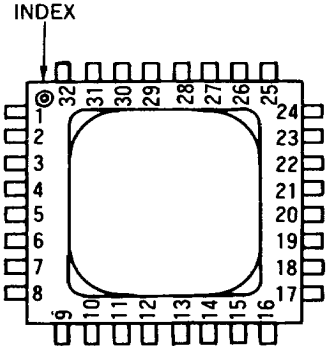
Recommended Operational Conditions

Item	Symbol	Min	Typ	Max	Unit	Remarks
Supply Voltage	Vss	–5.46	–5.20	–4.94	V	
Input Voltage	V_{IH}	–1.1		–0.8	V	
	V_{IL}	–1.8		–1.6		
Output termination voltage	V_{TT}		–2.0		V	
Input reference voltage	Vref	–1.386	–1.320	–1.254	V	
Input clock	CKp-p	0.6	0.8	1.2	Vp-p	

Block Diagram



Pin Description



Pin No	Pin Name	Function
1	DATA 4 OUT	DATA 4 OUTPUT
2	GND	GND
3	DATA 3 OUT	DATA 3 OUTPUT
4	GND	GND
5	DATA 2 OUT	DATA 2 OUTPUT
6	GND	GND
7	DATA 1 OUT	DATA 1 OUTPUT
8	GND	GND
9		
10		
11	1/4 clock out	1/4 clock out of input clock
12	GND	GND
13	Vss	–5.2 V voltage source input
14	GND	GND
15		
16		
17	Monitor	Gate bias control Pin, Normaly Open
18	GND	GND
19	Clock in	Clock input
20	GND	GND
21	Vref Out	Output Pin of ECL reference level voltage
22	Vref In	–1.32 V voltage source input
23	GND	GND
24	Data In	Data Input

25	GND	GND
26		
27		
28		
29		
30		
31		
32		
33		
34		

Electrical Characteristics

DC Characteristics

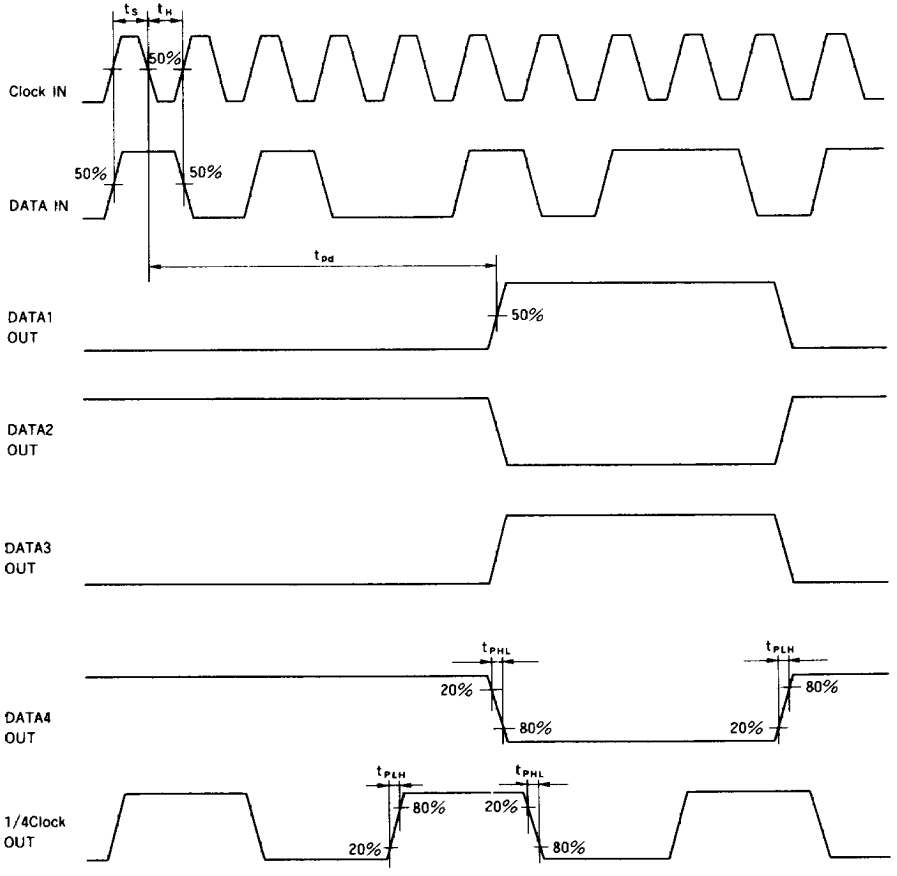
Item	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_{OH}	$V_{IN} = V_{IH}$ max, $R_T = 50\ \Omega$	−1.1		−0.8	V
	V_{OL}	$V_{IN} = V_{IL}$ min, $V_{TT} = -2$ V	−1.8		−1.6	
Input Voltage	V_{IH}		−1.1			V
	V_{IL}				−1.5	
Input Current	I_{IM}	$V_{IN} = V_{IH}$ max		160		μA
	I_{IL}	$V_{IN} = V_{IL}$ min		360		
Output Current	I_{OH}	$R_T = 50\Omega$			24	mA
	I_{OL}	$V_{TT} = -2$ V			8	
Supply Current	Iss			300		mA

AC Characteristics

Item	Symbol	Test Condition	Min	Typ	Max	Unit
Propagation delay time between data input and output	tpd	50% to 50%		*		ns
Input data setup time	ts		0.1			ns
Input data hold time	th		0.1			ns
Clock inter rate	fc max		2.4	3.6		GHz
	fc min				0.5	
Output Signal transition time	t_{TLH}	20% to 80%		0.25		ns
	t_{THL}	$R_T = 50\ \Omega$		0.25		

* tpd = (4T + 1.0) ns, T: Input Clock Sycle

Time Chart



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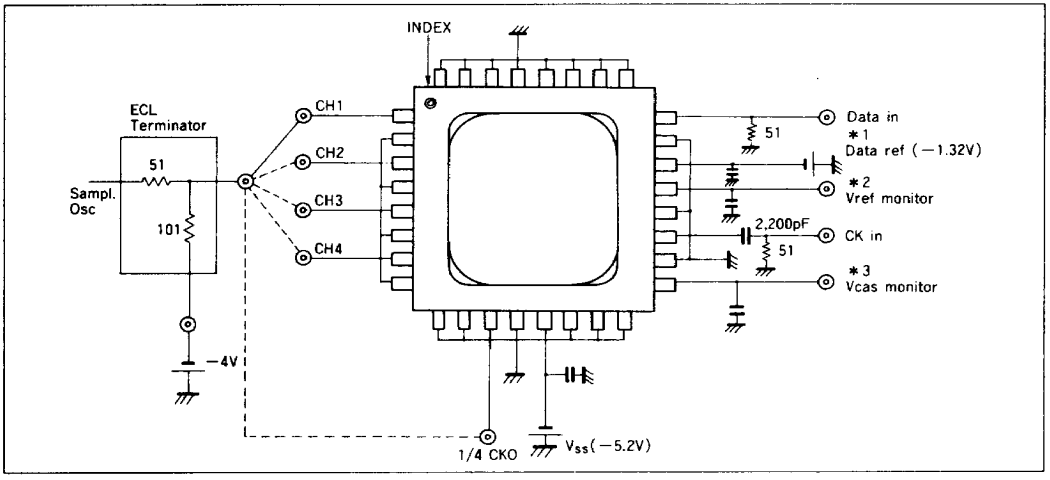
Test Circuit



Mechanical Drawings

Item	Content
Outward Form	12 x 12 x 3.35 t(mm) quad leaded chip carrier
Pin Count	32
Pin Pitch	1.27 (mm)
Characteristic Impedance of Signal Line	50 ± 5 (Ω)
Noise Decoupling Chip Capacitors	located in package
Thermal Registance	20 (°C/W) with Fin at natural convection