HY51C1000

1M×1-Bit CMOS DRAM

M131202B-APR91

DESCRIPTION

The HY51C1000 is a high speed, low power 1,048,576×1 bit CMOS dynamic random access memory. Fabricated with the HYUNDAI CMOS process, the HY51C1000 offers a fast page mode for high bandwidth and clock-free page operation, fast usable speed, CMOS standby current and inherently high CMOS reliability.

All inputs and outputs are TTL compatible. Input and output capacitances are significantly lowered to allow increased system performance.

Fast page mode operation allows random or sequential access of up to 1,024 bits within a row with cycle times as fast as 45ns. Because of static circuitry, the $\overline{CAS}$ clock is no longer in the critical timing path. The flow-through column latch allows address pipelining while relaxing many critical system timing requirements for fast usable speed. These features make the HY51C1000 ideally suited for cache based mainframe and mini computers, graphics, digital signal processing, and high performance microprocessor systems.

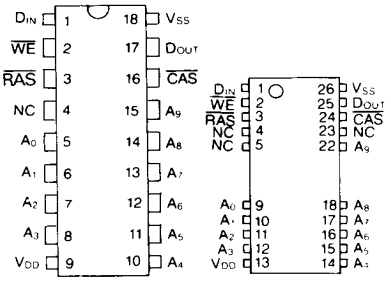
When $\overline{RAS}$ is $\geq V_{DD}-0.2V$, CMOS standby operation mode is active, and power drops to 1.5 mW (typically).

FEATURES

- **Low power dissipation**
  - **Operating current, 100ns : 75mA (max.)**
  - **TTL standby current : 2.5mA (max.)**
  - **CMOS standby current : 1.5mA (max.)**
- **Read-Modify-Write capability**
- **$\overline{RAS}$-only, Hidden, $\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **Common I/O capability**
- **Fast Page mode operation for a sustained data rate up to 22 MHz**
- **512 refresh cycles/8 ms**
- **High reliability 18 pin 300 mil P-DIP and 20/26 pin SOJ**
- **Fast access time and cycle time (ns)**

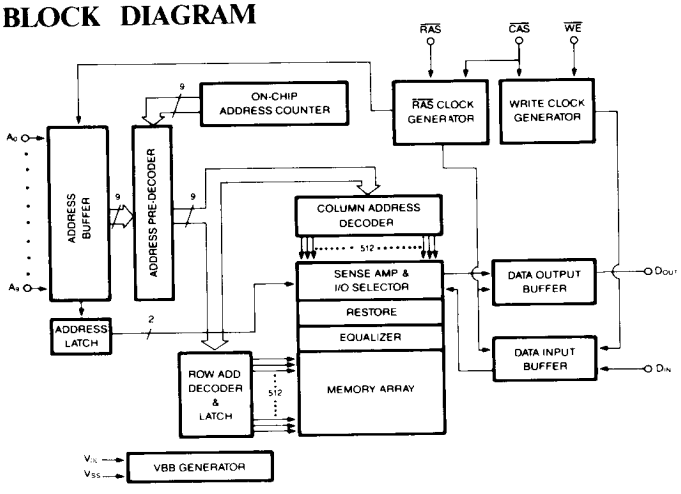
	HY51C1000-80	HY51C1000-10	HY51C1000-12
Max $\overline{RAS}$ Access Time, t_{RAC}	80	100	120
Max $\overline{CAS}$ Access Time, t_{CAC}	20	25	30
Min Fast Page Mode Cycle Time, t_{PC}	45	55	65
Min Cycle Time, t_{RC}	160	190	220

PIN CONNECTIONS



P-DIP SOJ

BLOCK DIAGRAM



PIN NAMES

$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{WE}$	WRITE ENABLE
A_0–A_9	ADDRESS INPUT
D_{IN}	DATA INPUT
D_{OUT}	DATA OUTPUT
V_{DD}	POWER (+5V)
V_{SS}	GROUND

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	°C
T_{STG}	Storage Temperature (Plastic)	−55 to 125	°C
V_{TERM}	Voltage on Any Pin Except V_{DD} Relative to V_{SS}	−1.0 to 7.0	V
V_{DD}	Voltage on V_{DD} Relative to V_{SS}	−1.0 to 7.0	V
I_{OUT}	Data Out Current	50	mA
P_T	Power Dissipation	1.0	W

NOTE: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

DC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED	HY51C1000		UNIT	NOTE
				MIN.	MAX.		
$\|I_{LI}\|$	Input Leakage Current (any input pin)	$V_{SS} \le V_{IN} \le V_{DD}$			10	μA	
$\|I_{LO}\|$	Output Leakage Current for High Impedance State	$V_{SS} \le D_{OUT} \le V_{DD}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}			10	μA	
I_{DD1}	V_{DD} Supply Current, Operating	$t_{RC}=t_{RC}$ (min.)	−80		95	mA	1,2
			−10		75		
			−12		70		
I_{DD2}	V_{DD} Supply Current, TTL Standby	$\overline{RAS}$, $\overline{CAS}$ at V_{IH}, other inputs $\ge V_{SS}$			2.5	mA	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-only Refresh	$t_{RC}=t_{RC}$ (min.)	−80		95	mA	2
			−10		75		
			−12		70		
I_{DD4}	V_{DD} Supply Current, Fast page mode	Minimum Cycle	−80		50	mA	1,2
			−10		40		
			−12		35		
I_{DD5}	V_{DD} Supply Current, CMOS Standby	$\overline{RAS} \ge V_{DD}-0.2V$, $\overline{CAS}=V_{IH}$, other inputs $\ge V_{SS}$			1.5	mA	
I_{DD6}	V_{DD} Supply Current, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh	$t_{RC}=t_{RC}$ (min.)	−80		95	mA	2
			−10		75		
			−12		70		
V_{IL}	Input Low Voltage (all inputs)			−0.5	0.8	V	3
V_{IH}	Input High Voltage (all inputs)			2.4	$V_{DD}+1$	V	3
V_{OL}	Output Low Voltage	$I_{OL}=4.2mA$			0.4	V	
V_{OH}	Output High Voltage	$I_{OH}=-5mA$		2.4		V	

NOTES :
1. I_{DD1} is dependent on output loading when the device output is selected. Specified I_{DD} (max.) is measured with output open.
2. I_{DD} is dependent upon the number of address transitions. Specified I_{DD} (max.) is measured with a maximum of two transitions per address cycle in Fast page mode.
3. Specified V_{IL} (min.) is steady state operation. During transitions, V_{IL} may undershoot to −1.0V for a period not to exceed 20ns. All AC parameters are measured with V_{IL} (min.) ≥ V_{SS} and V_{IH} (max.) ≤ V_{DD}.

AC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

#	SYMBOL	PARAMETER	HY51C1000						UNIT	NOTES
			80		10		12			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t_{RAS}	$\overline{RAS}$ Pulse Width	80	85K	100	85K	120	85K	ns	
2	t_{RC}	Random Read or Write Cycle Time	160		190		220		ns	
3	t_{RP}	$\overline{RAS}$ Precharge Time	70		80		90		ns	
4	t_{ASR}	Row Address Set-up Time	0		0		0		ns	
5	t_{RAH}	Row Address Hold Time	15		15		15		ns	
6	t_{CAR}	Column Address to $\overline{RAS}$ Set-up Time	40		45		55		ns	
7	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	40	20	55	20	65	ns	1
8	t_{ASC}	Column Address Set-up Time	0		0		0		ns	
9	t_{CAH}	Column Address Hold Time	15		20		25		ns	
10	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	25	60	25	75	25	90	ns	2
11	t_{RAC}	Access Time From $\overline{RAS}$		80		100		120	ns	3,4,5
12	t_{CAA}	Access Time From Column Address		40		45		55	ns	5,6,12
13	t_{CAC}	Access Time From $\overline{CAS}$		20		25		30	ns	6,12
14	$t_{CAS(R)}$	$\overline{CAS}$ Pulse Width in Read Cycle	20		25		30		ns	
15	$t_{RSH(R)}$	$\overline{RAS}$ Hold Time in Read Cycle	20		25		30		ns	
16	t_{RCS}	Read Command Set-up Time	0		0		0		ns	
17	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	5		5		5		ns	7
18	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	5		5		5		ns	7
19	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5		5		10		ns	
20	t_{OFF}	Output Buffer Turn Off Delay	0	20	0	25	0	30	ns	8
21	t_{OH}	Output Data Hold Time From $\overline{CAS}$	0		0		0		ns	8
22	t_{WP}	Write Pulse Width	10		10		15		ns	
23	t_{CP}	$\overline{CAS}$ Precharge Time	10		10		15		ns	
24	t_{AR}	Column Address Hold Time From $\overline{RAS}$	60		70		80		ns	
25	$t_{CAS(W)}$	$\overline{CAS}$ Pulse Width in Write Cycle	25		30		35		ns	
26	$t_{RSH(W)}$	$\overline{RAS}$ Hold Time in Write Cycle	25		30		35		ns	
27	t_{WCR}	Write Command Hold Time From $\overline{RAS}$	60		70		80		ns	
28	t_{WCS}	Write Command Set-up Time	0		0		0		ns	9,10
29	t_{WCH}	Write Command Hold Time	15		20		25		ns	
30	t_{DS}	Data-In Set-up Time	0		0		0		ns	11
31	t_{DH}	Data-In Hold Time	15		20		25		ns	11
32	t_{DHR}	Data-In Hold Time Reference to $\overline{RAS}$	60		70		80		ns	
33	t_{RWC}	RMW Cycle Time	190		220		255		ns	
34	t_{RRW}	RMW Cycle $\overline{RAS}$ Pulse Width	110		130		155		ns	
35	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay in RMW Cycle	80		100		120		ns	9
36	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	20		25		30		ns	9
37	t_{AWD}	Column Address to $\overline{WE}$ Delay	40		45		55		ns	9
38	t_{CAP}	Access Time From Column Precharge		40		50		60	ns	12

#	SYMBOL	PARAMETER	HY51C1000						UNIT	NOTES
			80		10		12			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
39	t_{PC}	Fast page mode Read or Write Cycle time	45		55		65		ns	
40	t_{PCM}	Fast page mode Read-Modify-Write Cycle	70		85		100		ns	
41	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	25		25		30		ns	
42	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	25		25		30		ns	
43	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0		0		0		ns	
44	t_{CSR}	$\overline{CAS}$ Set-up Time ($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	10		10		10		ns	
45	t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	20		30		30		ns	
46	t_{CSH}	$\overline{CAS}$ Hold Time	80		100		120		ns	
47	t_T	Transition Time (Rise and Fall)	3	25	3	25	3	25	ns	13,14
48	t_{RI}	Refresh Interval (512 Cycle)		8		8		8	ms	15

NOTES:

1. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a referenced point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then the access time is controlled by t_{CAA} and t_{CAC}.
2. t_{RCD} (max.) is specified for reference only. Operation within t_{RCD} (max.) and t_{RAD} (max.) limit insure that t_{RAC} (max.) and t_{CAA} (max.) can be met. If t_{RCD} is greater than the specified t_{RCD} (max.) then the access time is controlled by t_{CAA} and t_{CAC}.
3. Assume $t_{RAD} \leq t_{RAD}$ (max.). If t_{RAD} is greater than t_{RAD} (max.) then t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD} (max.)
4. Assume $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than t_{RCD} (max.) then t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max.)
5. Measured with a load equivalent to two TTL loads and 100 pF.
6. Assume $t_{RAD} \geq t_{RAD}$ (max.)
7. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
8. t_{OFF} and t_{OH} define the time at which the data output achieves the open circuit condition and is not referenced to the output voltage levels.
9. t_{WCS}, t_{WHC}, t_{WHR}, t_{RWD}, t_{AWD}, t_{CWD}, are not restrictive operating parameters.
10. t_{WCS} (min.) must be satisfied in the early write cycle.
11. t_{DS} and t_{DH} are referenced to the latter occurence of $\overline{CAS}$ or $\overline{WE}$.
12. Access time is determined by the longer of t_{CAA}, t_{CAC} or t_{CAP}.
13. t_T is measured between V_{IH} (min.) and V_{IL} (max.)
14. AC measurements assume t_T = 5ns.
15. An initial pause of 200μs is required after power-up and followed by a minimum of 8 initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh). 8 initialization cycles are required after extended period of bias without clocks.

CAPACITANCE

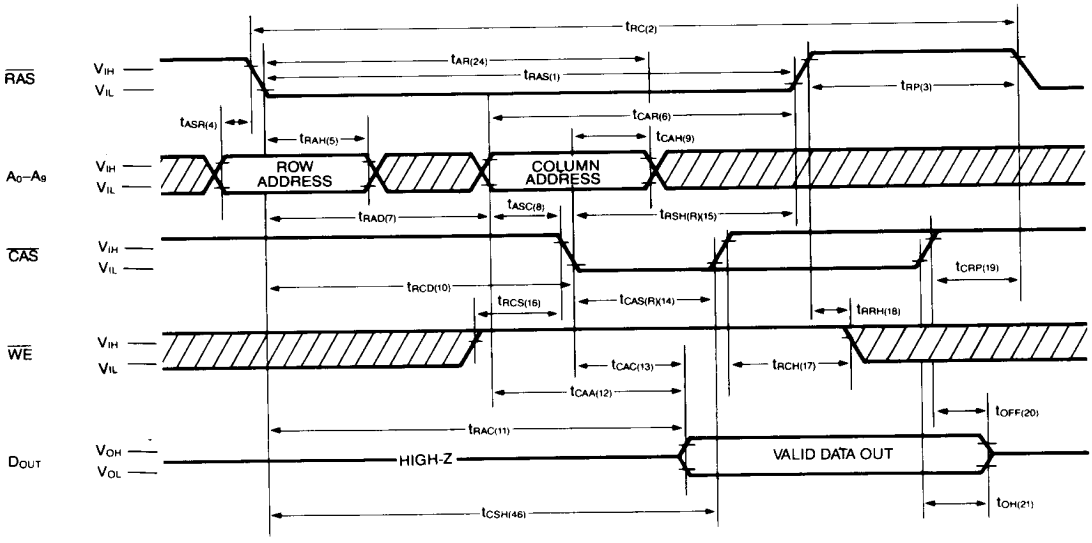
(T_A=25°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Address, D_{IN}	—	6	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	—	8	pF
C_{OUT}	D_{OUT}	—	8	pF

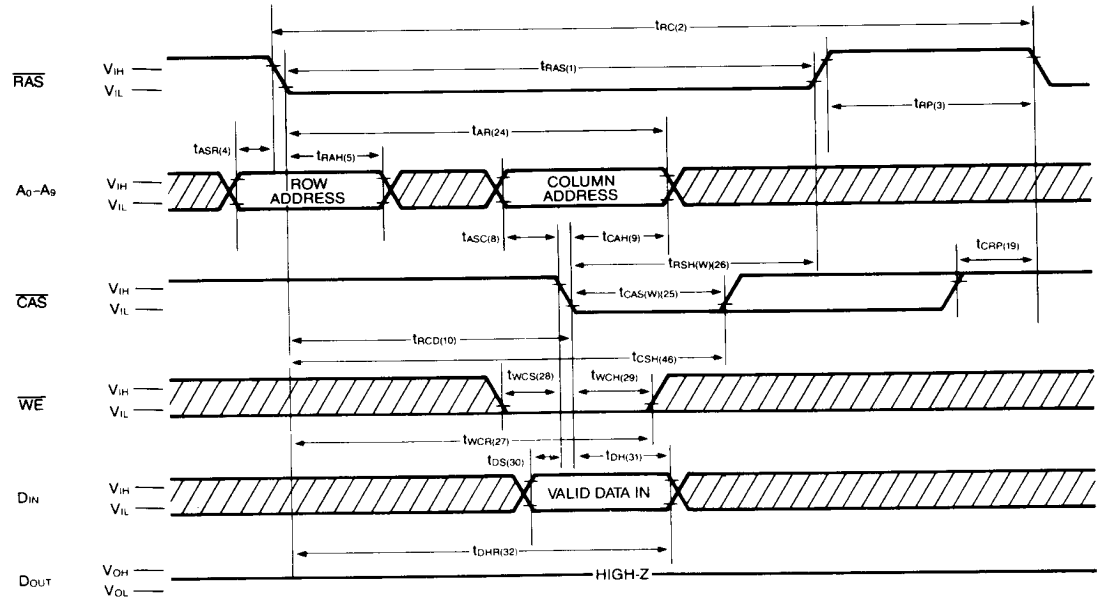
NOTE: Capacitance is measured at the worst case of voltage levels with a programmable capacitance meter.

TIMING DIAGRAM

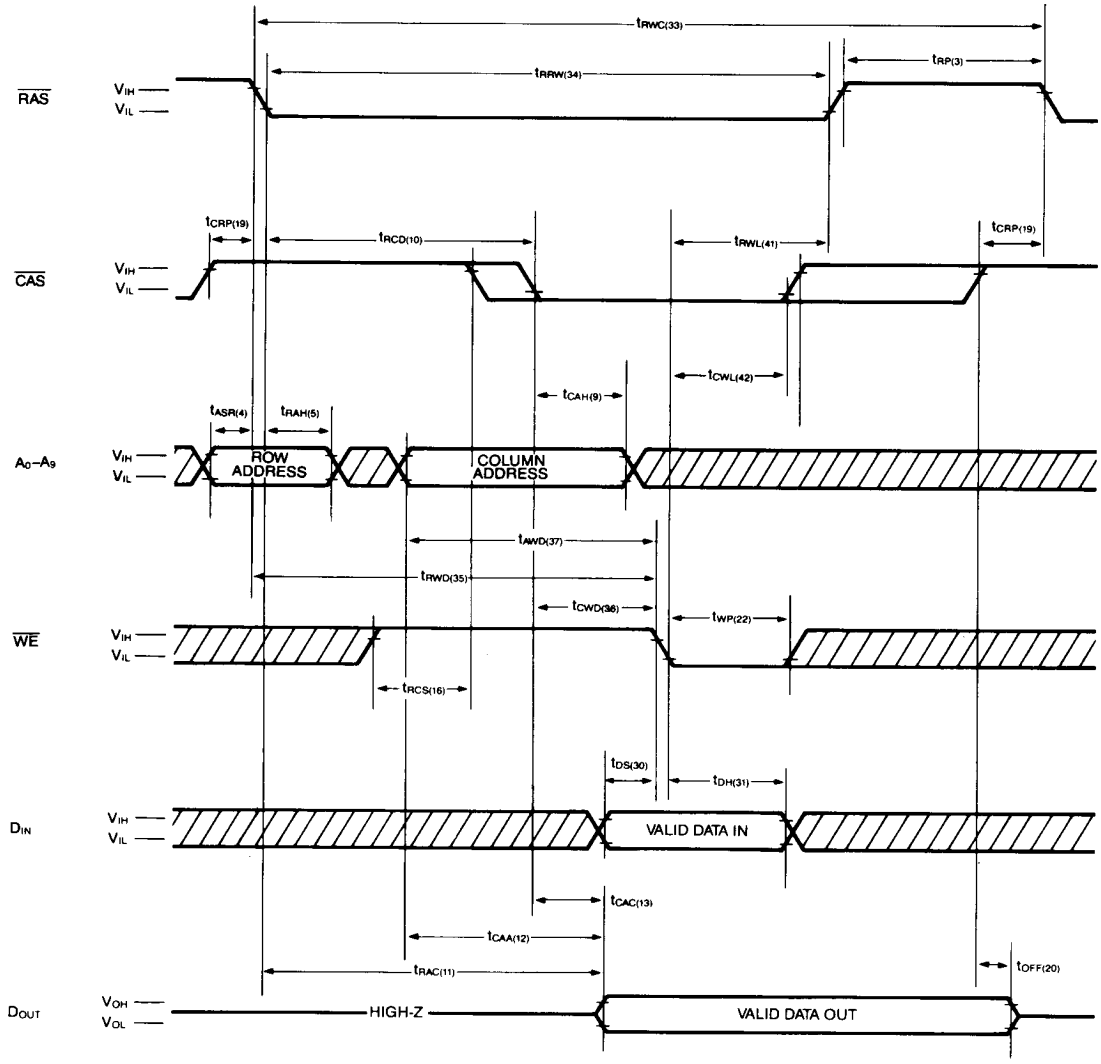
READ CYCLE



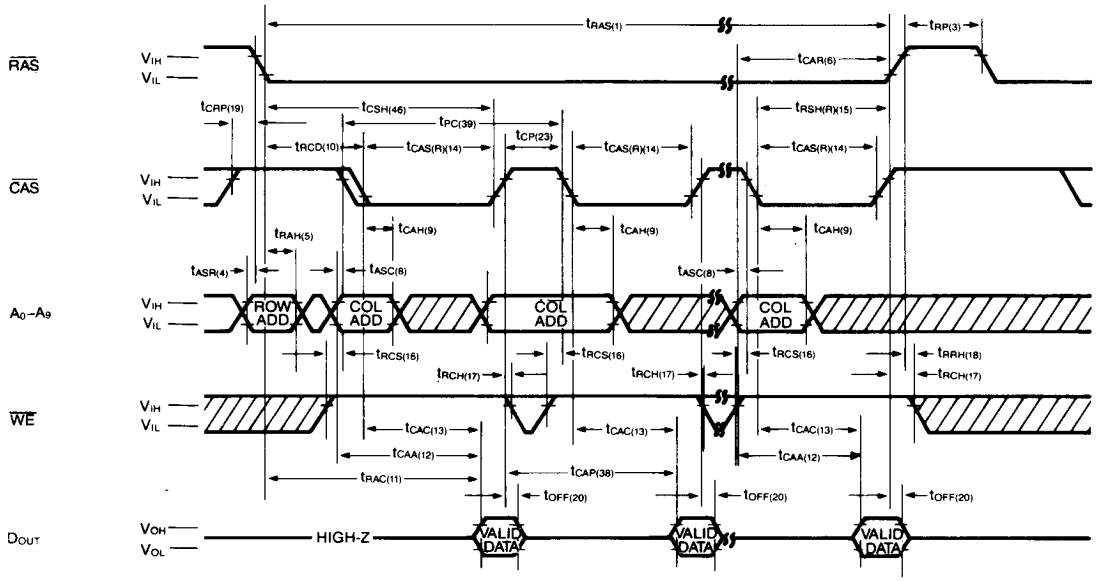
EARLY WRITE CYCLE



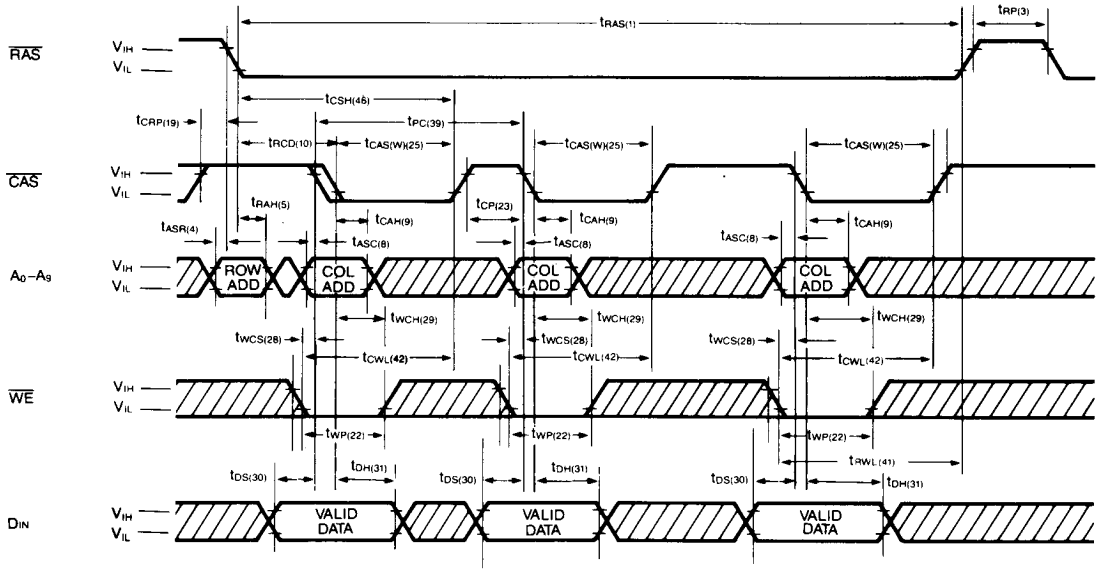
READ-MODIFY-WRITE CYCLE



FAST PAGE MODE READ CYCLE



FAST PAGE MODE EARLY WRITE CYCLE



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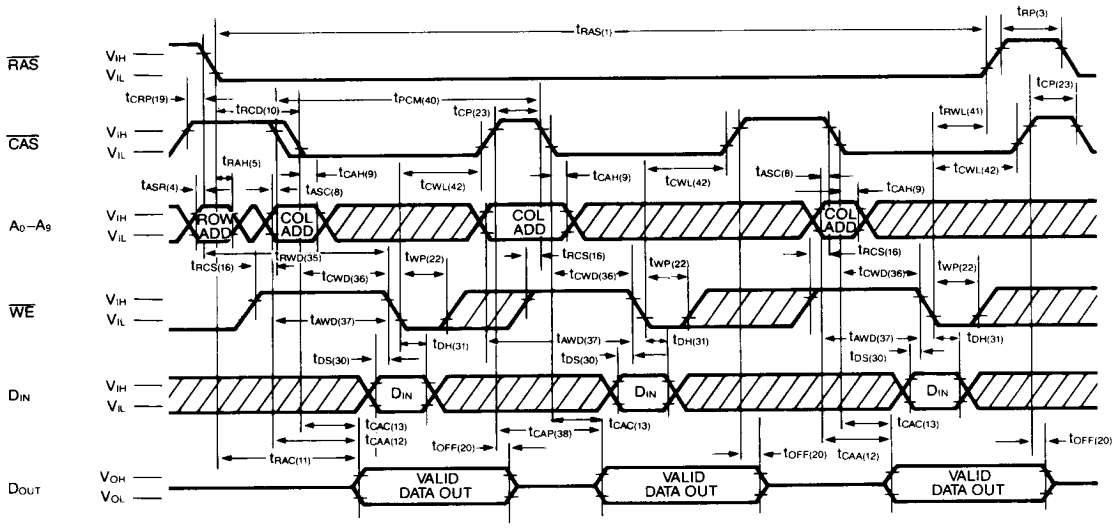
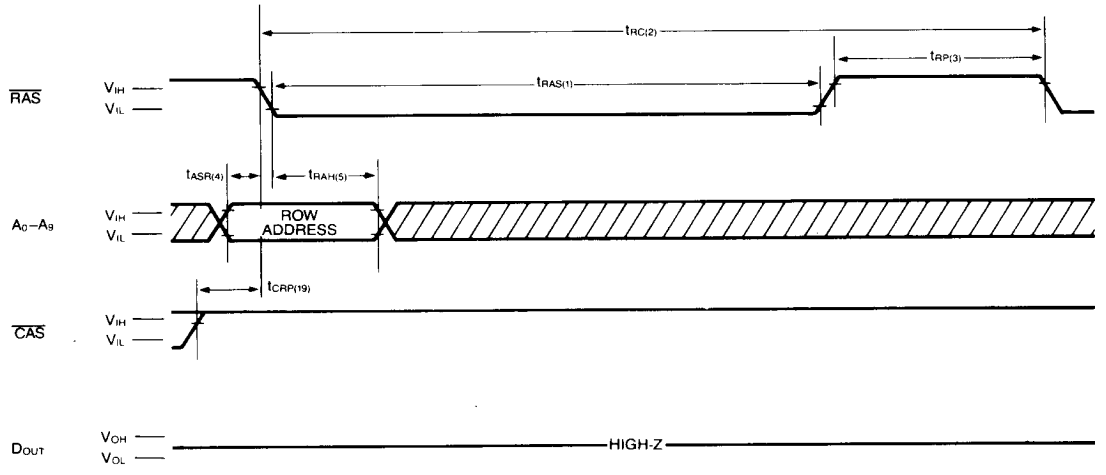
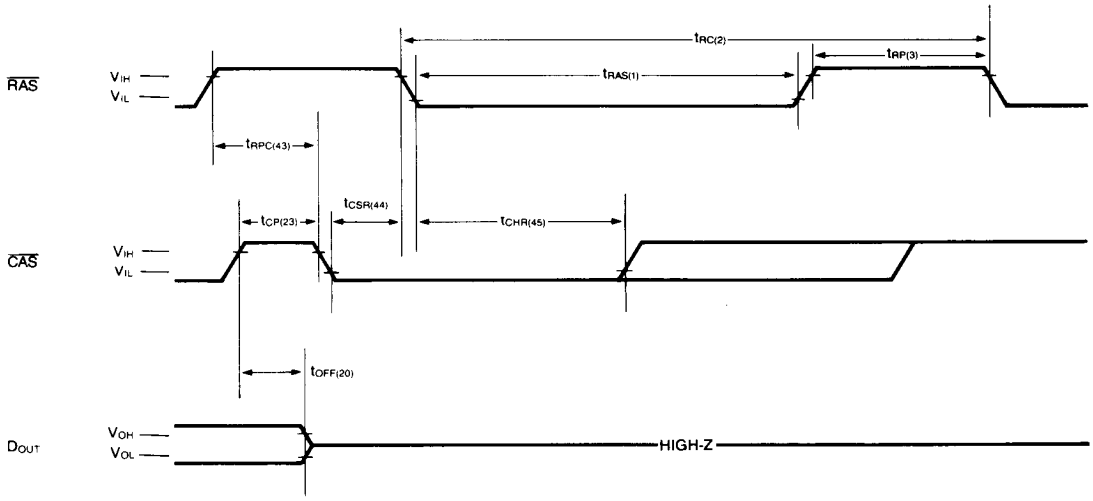
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



RAS-ONLY REFRESH CYCLE

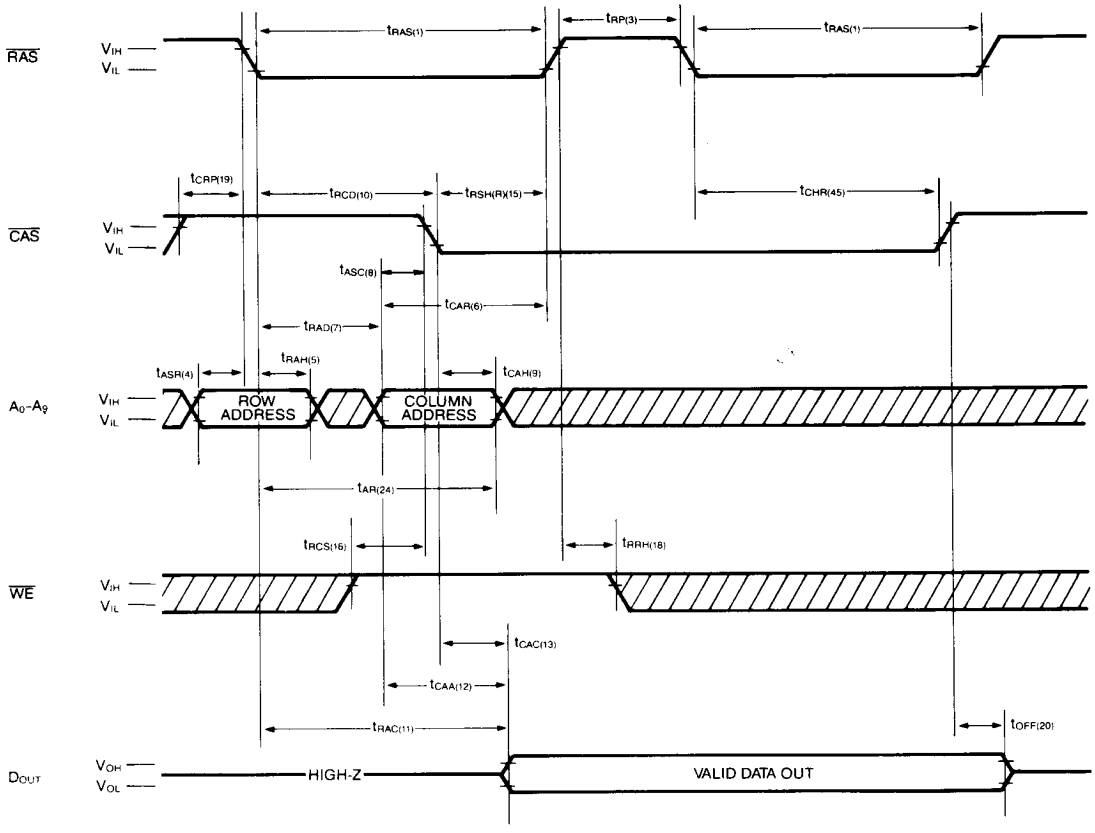


$\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH CYCLE

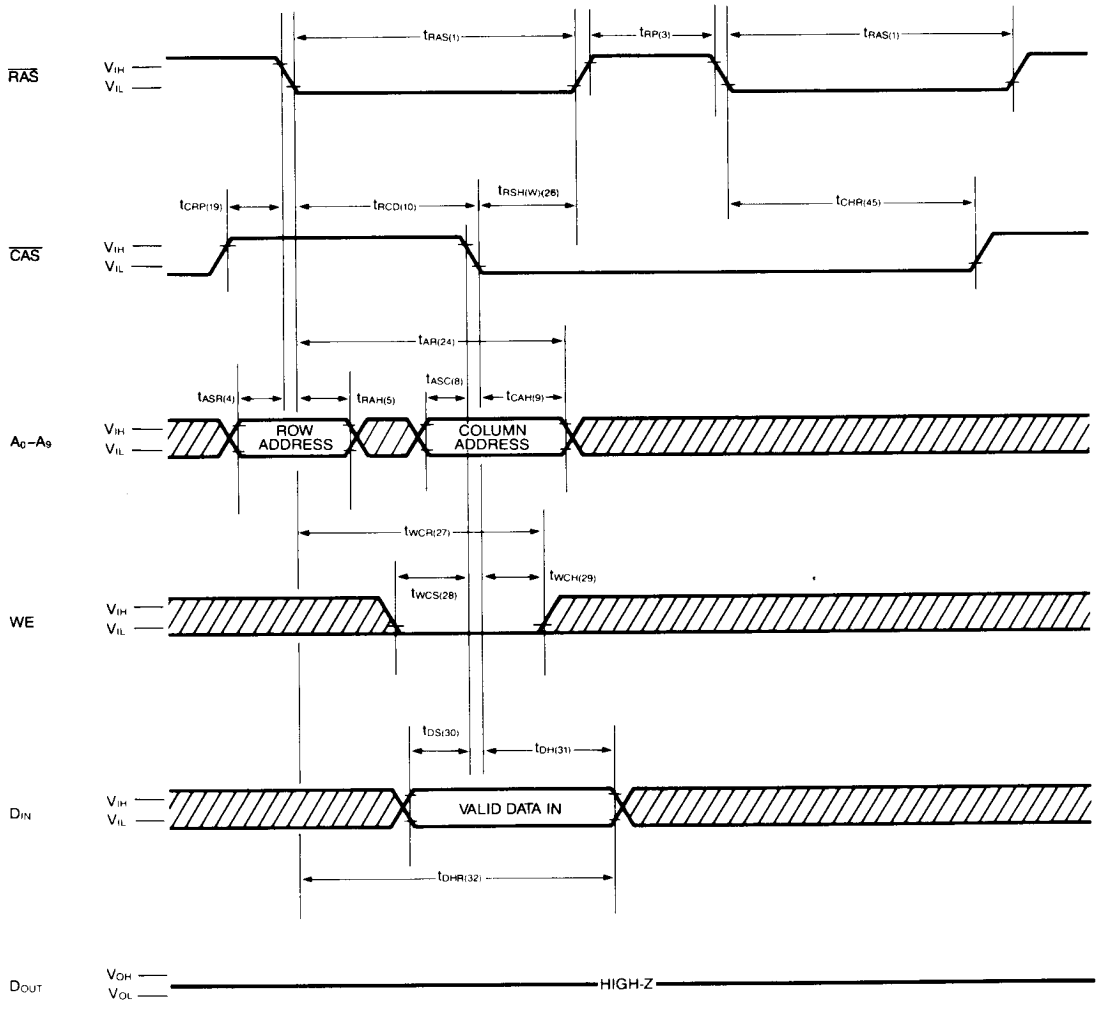


Note: $\overline{\text{WE}}$, A_0-A_9=Don't care

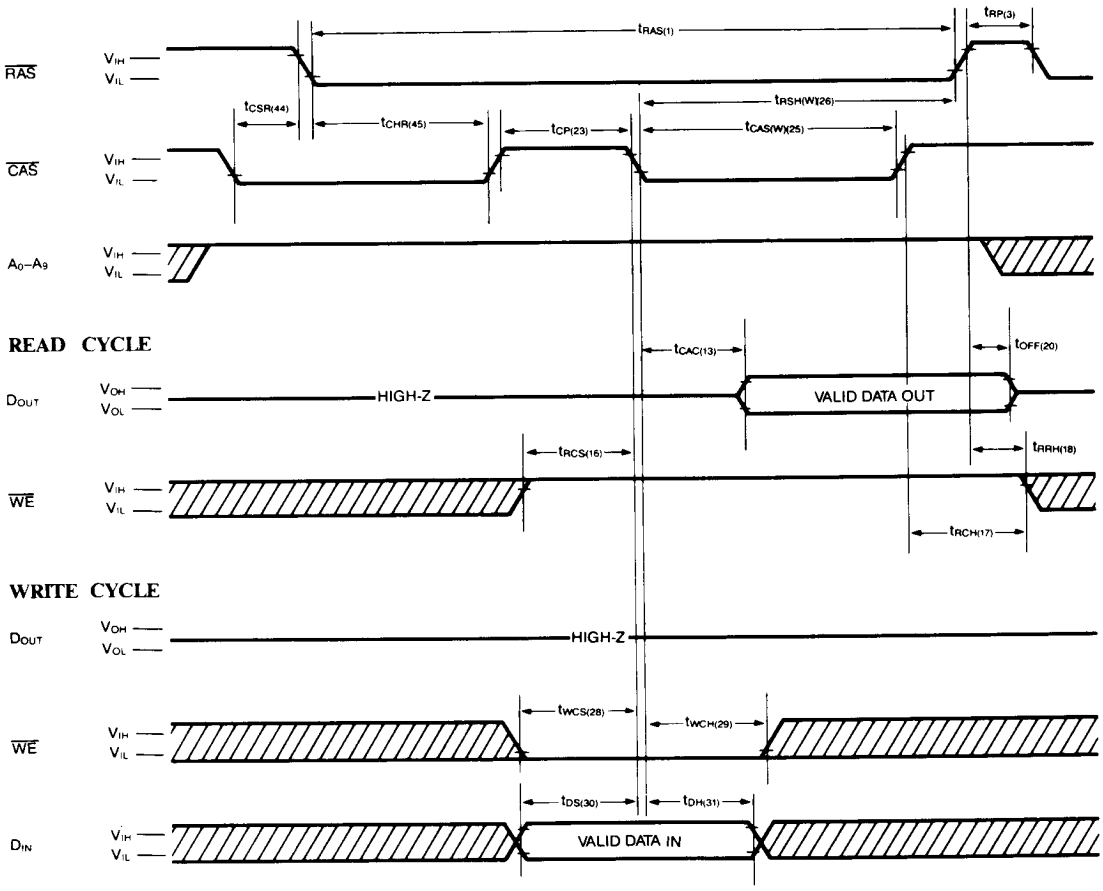
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



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FUNCTIONAL DESCRIPTION

The HY51C1000 is a CMOS dynamic RAM optimized for high data bandwidth and low power applications. The functionality is similar to a traditional dynamic RAM. The HY51C1000 reads and writes one bit of data by multiplexing 20 bit address into 10 bit row and 10 bit column address. The row address is latched by Row Address Strobe($\overline{RAS}$). The column address, however, flows through the internal address buffer and is latched by the Column Address Strobe ($\overline{CAS}$). Because access time is primarily dependent on a valid column address, the delay time between $\overline{RAS}$ and $\overline{CAS}$ can be long without affecting the access time.

MEMORY CYCLE

The memory cycle is initiated by bringing $\overline{RAS}$ low. Any memory cycle once initiated must not be ended or aborted prior to fulfilling the minimum t_{RAS} timing specification. This ensures proper device operation and data integrity. Additionally, a new cycle can not be initiated until the minimum precharge time t_{RP}/t_{CP} has elapsed.

READ CYCLE

A read cycle is performed by holding the Write Enable ($\overline{WE}$) signal high during a $\overline{RAS}/\overline{CAS}$ operation. The column address must be held for a minimum time specified by t_{AR}. Data output becomes valid only when t_{RAC}, t_{CAC} and t_{CAA} are all satisfied. Consequently, the access time is dependent upon the timing relationship among the t_{RAC}, t_{CAC} and t_{CAA}. For example, the access time is limited by t_{CAA} when t_{RAC} and t_{CAC} are both satisfied.

WRITE CYCLE

A write cycle is performed by taking $\overline{WE}$ and $\overline{CAS}$ low during a $\overline{RAS}$ operation. The column address is latched by $\overline{CAS}$. The write can be $\overline{WE}$ controlled or $\overline{CAS}$ controlled depending upon the latter of $\overline{WE}$ or $\overline{CAS}$ low transition. Consequently, the input data must be valid at or before the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. In a $\overline{CAS}$ controlled write cycle (the leading edge or $\overline{WE}$ occurs priors to or coincident with the $\overline{CAS}$ low transition) the output(D_{OUT}) pin will be in the high impedance state at the beginning of the write function. Terminating the write action with $\overline{RAS}$ or $\overline{CAS}$ going high will maintain the data output (D_{OUT}) in the high impedance state.

REFRESH CYCLE

To retain data, 512 $\overline{RAS}$ refresh cycle are required in an 8 ms period. The refresh operation can be performed two ways :

1. Clocking each of 512 row address(A_0 through A_8) with $\overline{RAS}$ at least every 8 ms period. Any combination of $\overline{RAS}$ cycle such as read, write, read-modify-write, or $\overline{RAS}$-Only refresh cycle will perform a refresh on the selected row.
2. $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle : IF $\overline{CAS}$ go low prior to $\overline{RAS}$ go low, the chip enters a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle. In $\overline{CAS}$ before-$\overline{RAS}$-refresh cycle the HY51C1000 will use an internal nine-bit counter output as the source of the row address and will ignore the external address input.

This $\overline{CAS}$-before-$\overline{RAS}$ refresh mode is a refresh only mode and no data access is allowed. Also, the $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle does not cause device selection and the state of the data output pin will remain in a high impedance state.

In order to guarantee the reliable operation of the $\overline{CAS}$-before-$\overline{RAS}$ refresh mode, a internal counter test mode is provided. The user can use the counter test mode to write in a data pattern consecutively (512 write cycles) and then verify the data which has been written by 512 consecutive read cycles.

DATA RETENTION MODE

The HY51C1000 offers a CMOS standby mode that is entered by causing the $\overline{RAS}$ clock

to swing between a valid V_{IL} and an "extra high" V_{IH} within 0.2V of V_{DD}. While the $\overline{RAS}$ clock is at the "extra high" level, the HY51C1000 power consumption is reduced to the low I_{DDS} level. Overall I_{DD} consumption when operating in this mode can be calculated as follows :

$$I=\frac{(t_{RC})\times(I\ active)+(t_{RX}-t_{RC})\times(I_{DDS})}{t_{RX}}$$

Where t_{RC}=Refresh Cycle Time
t_{RX}=Refresh Interval/512

FAST PAGE MODE OPERATION

Fast page mode operation permits all 1024 columns within a selected row of the device to be randomly accessed at a high data rate. Maintaining $\overline{RAS}$ low while successive $\overline{CAS}$ cycles are performed retains the row address internally, eliminating the need to reapply it. The column address buffer acts as a transparent or flow through latch while $\overline{CAS}$ is high. Access begins from the valid column address rather than from $\overline{CAS}$, eliminating t_{ASC} and t_T from the critical timing path. $\overline{CAS}$ latch the address into column address buffer and acts as an output enable.

During this operation, read, write, and read-modify-write, or read-write-read cycles are possible at random or sequential address within a row. Following the entry cycle into fast page mode, access time is t_{CAA} or t_{CAP} dependent. If the column adderess is valid prior to or coincident by t_{CAP} as shown in figure 1. If the column address is valid after the rising edge of $\overline{CAS}$, then the access time is determined by the valid column address specified by t_{CAA}. For both cases, the falling edge of $\overline{CAS}$ latches the address and enable the output.

Fast page mode provides a sustanined data rate over 22 MH_Z for applications that require high data rates, such as bit mapped graphics or high speed signal processing. The following equation can be used to calculate the data rate :

$$\text{Data Rate}=\frac{1024}{t_{RC}+1023\times t_{PC}}$$

DATA OUT OPERATION

The HY51C1000 data output(D_{OUT}), which has tri-state capability, is controlled by $\overline{CAS}$. During a $\overline{CAS}$ the high state ($\overline{CAS}$ at V_{IH}), the data output is in the high impedance state. The following table summarize the D_{OUT} state for various types of cycles.

CYCLE	D_{OUT} STATE
Read Cycle	Data from Addressed Memory Cell
$\overline{CAS}$ Controlled Write Cycle (Early Write)	High Impedance
$\overline{WE}$ Controlled Write Cycle (Late Write)	Active, Not Valid
Read-Modify-Write Cycle	Data from Addressed Memory Cell
Fast Page Mode Read Cycle	Data from Addressed Memory Cell
Fast Page Mode Write Cycle (Early Write)	High Impedance
Fast Page Mode Read-Modify-Write Cycle	Data from Addressed Memory Cell
$\overline{RAS}$-Only Refresh Cycle	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle	Data remain the previous cycle's state (high Impedance or low Impedance
$\overline{CAS}$-Only Cycle	High Impedance

POWER ON

An initial pause of 200 μs is required after the application of the V_{DD} power supply, followed by a minimum of eight initialization cycles(any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh cycle). Eight initialization cycles are required after extended periods of bias without clocks(greater than the refresh interval).

The V_{DD} current (I_{DD}) requirement of the HY51C1000 during power on is dependent upon the input levels of $\overline{RAS}$ and $\overline{CAS}$. If $\overline{RAS}=V_{SS}$ during power on, the device will go into an active cycle and I_{DD} will exhibit large current transients. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{DD} or be held at a valid V_{IH} level during power on.

FIGURE 1. FAST PAGE MODE ACCESS TIME DETERMINATION