Circuit and Application Options

Digital Inputs

FS0 (2), FS1 (1), FS2 (20),FS3(19), and **FS4 (18),** are the TTL compatible frequency select inputs for the binary code corresponding to the frequency desired. **STROBE (3)** when high, allows new data into the frequency select latches; and

Applications

Layout Considerations

Utilizing the **ICS1560** in video graphics applications is simple, but does require precautions in board layout if satisfactory jitter-free performance is to be realized. A low series inductance bypass capacitor of .047 μF should be utilized

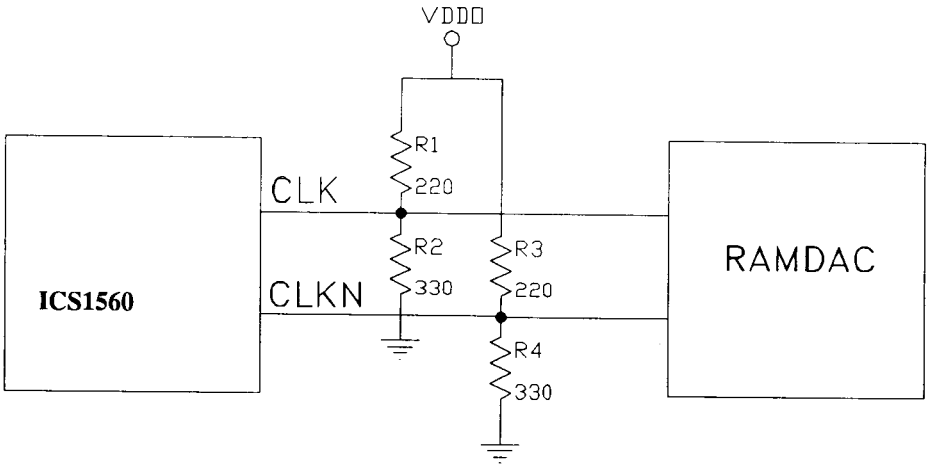
Frequency Reference

The internal reference oscillator contains all of the passive components required. An appropriate series resonant crystal should be connected between **XTAL1 (5)** and **XTAL2 (6)**. In IBM™ compatible applications this will typically be a 14.31818 MHz crystal, but crystals between 5MHz and 25MHz may be used. Maintain short lead lengths between the crystal and the **ICS1560**. In some applications, it may be desirable to utilize the bus clock. To do this, connect the clock through a .047μF capacitor to **XTAL1 (5)**, and keep the lead length of the capacitor to **XTAL1 (5)** to a minimum to reduce noise susceptibility. This input is internally biased at $V_{DD/2}$ since TTL compatible clocks typically exhibit a V_{OH} of 3.5V. Capacitively coupling the input restores noise immunity. The **ICS1560** is not sensitive to the duty cycle of the bus clock; however, the quality of this signal varies considerably with different motherboard designs. As the quality of the bus clock is typically outside of the control of the graphics adapter card manufacturer, it is suggested that this signal be buffered on the graphics adapter board. **XTAL2 (6)** must be left open in this configuration.

Output Circuit Considerations

The **CLK** and **CLKN** outputs are each connected to the drains of P- Channel MOSFET devices. The source of each of these devices is connected to V_{DDO}. Typical on resistance of each device is 15Ω. Typically these outputs will drive the clock and clock* inputs of a RAMDAC™ device. The inputs of the RAMDAC™ should have a 220Ω resistor connected to +5V and a 330Ω resistor connected to ground as physically close to the RAMDAC™ as practical.

Typical Output Configuration



NOTE: RAMDAC is a trademark of Brooktree Corporation.

Absolute Maximum Ratings

Ambient Temperature under bias	T_O	0 °C to 70 °C
Supply Voltage	V_{DD}	-0.5V to +7V
Input Voltage	V_{IN}	-0.5V to V_{DD} +0.5V
Output Voltage	V_{OUT}	-0.5V to V_{DD} +0.5V
Clamp Diode Current	V_{IK} & I_{OK}	+/-30mA
Output Current per Pin	I_{OUT}	+/-50mA
Storage Temperature	T_S	-85 °C to +150 °C
Power Dissipation	P_D	500mW

Values beyond these ratings may damage the device. This device contains circuitry to protect the inputs and outputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than the maximum rated voltages. For proper operation it is recommended that V_{IN} and V_{OUT} be constrained to $>= V_{SS}$ and $<= V_{DD}$.

Typical Operating Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	DV_{DD},AV_{DD}	4.5	5.0	5.5	Volts
Digital Supply Current (Fout = 50 MHz, internal xtal oscillator used for Fref.)	DI_{DD}		11		Milliamps
Digital Supply Current (Fout = 50 MHz, Ext. clock used for Fref.)	DI_{DD}		10		Milliamps
Analog Supply Current (F_{out} = 50 MHz)	AI_{DD}		3.2		Milliamps
Digital Supply Current (F_{out} = 120 MHz)	DI_{DD}		20		Milliamps
Analog Supply Current (F_{out} = 120 MHz)	AI_{DD}		9.6		Milliamps
Output Impedance CLK, CLKN	Z_{OUT}		15		Ohms
Output Drive Current	I_{SOURCE}, I_{SINK}		4		Milliamps
Phase Comparator Characteristics					
Gain Constant	$K\phi$		0.4		Volts/Radian
Bus TIming					
Setup Timing FS0-FS4 relative to STROBE	T_{SETUP}		10		ns
Hold Time FS0-FS4 relative to STROBE	T_{HOLD}		10		ns