LH540205

ADVANCE INFORMATION

CMOS 8192 × 9 Asynchronous FIFO

FEATURES

- Fast Access Times: 20/25/35/50 ns
- Fast-Fall-Through Time Architecture Based on CMOS Dual-Port SRAM Technology
- Input Port and Output Port Have Entirely Independent Timing
- Expandable in Width and Depth
- Full, Half-Full, and Empty Status Flags
- Data Retransmission Capability
- TTL-Compatible I/O
- Pin and Functionally Compatible with Am/IDT7205
- Pin and Functionally Compatible, Except for Depth, With Smaller Industry-Standard ×9 FIFOs, Such as IDT7201 Series, and Sharp LH5496 and LH540201 Series
- Control Signals Assertive-LOW for Noise Immunity
- Packages:
  28-Pin, 300-mil PDIP
  28-Pin, 600-mil PDIP *

FUNCTIONAL DESCRIPTION

The LH540205 is a FIFO (First-In, First-Out) memory device, based on fully-static CMOS dual-port SRAM technology, capable of storing up to 8192 nine-bit words. It follows the industry-standard architecture and package pinouts for nine-bit asynchronous FIFOs. Each nine-bit LH540205 word may consist of a standard eight-bit byte, together with a parity bit or a block-marking/framing bit.

The input and output ports operate entirely independently of each other, unless the LH540205 becomes either totally full or else totally empty. Data flow at a port is initiated by asserting either of two asynchronous, assertive-LOW control inputs: Write ($\overline{W}$) for data entry at the input port, or Read ($\overline{R}$) for data retrieval at the output port.

Full, Half-Full, and Empty status flags monitor the extent to which the internal memory has been filled. The system may make use of these status outputs to avoid the risk of data loss, which otherwise might occur either by attempting to write additional words into an already-full LH540205, or by attempting to read additional words from an already-empty LH540205. When an LH540205 is operating in a depth-cascaded configuration, the Half-Full Flag is not available.

Data words are read out from the LH540205's output port in precisely the same order that they were written in at its input port; that is, according to a First-In, First Out (FIFO) queue discipline. Since the addressing sequence for a FIFO device's memory is internally predefined, no external addressing information is required for the operation of the LH540205 device.

Drop-in-replacement compatibility is maintained with both larger sizes and smaller sizes of industry-standard nine-bit asynchronous FIFOs. The only change is in the number of internally-stored data words implied by the states of the Full Flag and the Half-Full Flag.

The Retransmit ($\overline{RT}$) control signal causes the internal FIFO-memory-array read-address pointer to be set back to zero, to point to the LH540205's first physical memory location, without affecting the internal FIFO-memory-array write-address pointer. Thus, the Retransmit control signal provides a mechanism whereby a block of data, delimited by the zero physical address and the current write-address-pointer value, may be read out *repeatedly* an arbitrary number of times. The only restrictions are that neither the read-address pointer nor the write-address

PIN CONNECTIONS

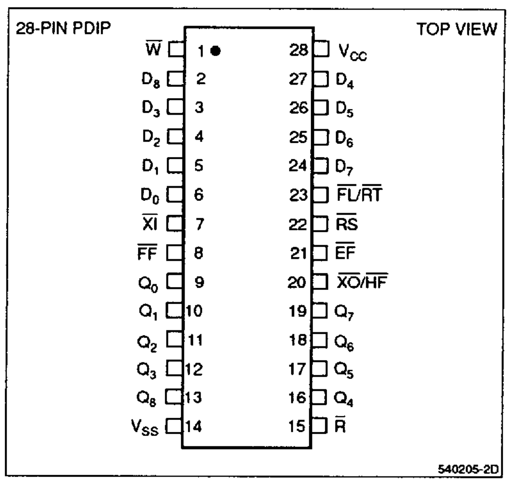

Figure 1. Pin Connections for PDIP Packages

* This is an Advance Information data sheet; except that all references to the 600-mil PDIP still have Product Preview status.

FUNCTIONAL DESCRIPTION (cont'd)

pointer may 'wrap around' during this entire process, i.e., advance past physical location zero after traversing the entire memory. The retransmit facility is not available when an LH540205 is operating in a depth-expanded configuration.

The Reset ($\overline{RS}$) control signal returns the LH540205 to an initial state, empty and ready to be filled. An LH540205 should be reset during every system power-up sequence. A reset operation causes the internal FIFO-memory-array write-address pointer, as well as the read-address pointer, to be set back to zero, to point to the LH540205's first physical memory location. Any information which previously had been stored within the LH540205 is not recoverable after a reset operation.

A cascading (depth-expansion) scheme may be implemented by using the Expansion In ($\overline{XI}$) input signal and the Expansion Out ($\overline{XO}/\overline{HF}$) output signal. This scheme allows a deeper 'effective FIFO' to be implemented by using two or more individual LH540205 devices, without incurring additional latency ('fallthrough' or 'bubblethrough') delays, and without the necessity of storing and retrieving any given data word more than once. In this cascaded operating mode, one LH540205 device must be designated as the 'first-load' or 'master' device, by grounding its First-Load ($\overline{FL}/\overline{RT}$) control input; the remaining LH540205 devices are designated as 'slaves,' by tying their $\overline{FL}/\overline{RT}$ inputs HIGH. Because of the need to share control signals on pins, the Half-Full Flag and the retransmission capability are not available for either 'master' or 'slave' LH540205 devices operating in cascaded mode.

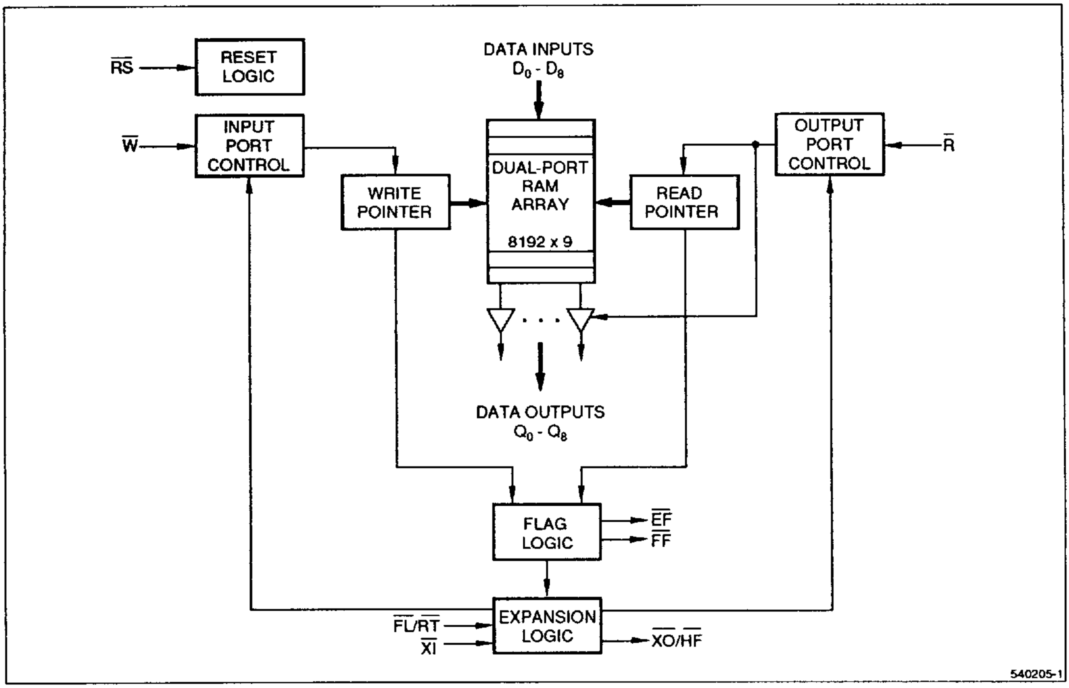

Figure 2. LH540205 Block Diagram

PIN DESCRIPTIONS

PIN	PIN TYPE *	DESCRIPTION
$D_0 - D_8$	I	Input Data Bus
$Q_0 - Q_8$	O/Z	Output Data Bus
$\overline{W}$	I	Write Request
$\overline{R}$	I	Read Request
$\overline{EF}$	O	Empty Flag
$\overline{FF}$	O	Full Flag

PIN	PIN TYPE *	DESCRIPTION
$\overline{XO}/\overline{HF}$	O	Expansion Out/Half-Full Flag
$\overline{XI}$	I	Expansion In
$\overline{FL}/\overline{RT}$	I	First Load/Retransmit
$\overline{RS}$	I	Reset
V_{CC}	V	Positive Power Supply
V_{SS}	V	Ground

* I = Input, O = Output, Z = High-Impedance, V = Power Voltage Level

OPERATIONAL DESCRIPTION

Reset

The LH540205 is reset whenever the Reset input ($\overline{RS}$) is taken LOW. A reset operation initializes both the read-address pointer and the write-address pointer to point to location zero, the first physical memory location. During a reset operation, the state of the $\overline{XI}$ and $\overline{FL}/\overline{RT}$ inputs determines whether the device is in standalone mode or in depth-cascaded mode. (See Tables 1 and 2.)

A reset operation is required whenever the LH540205 first is powered up. The Read ($\overline{R}$) and Write ($\overline{W}$) inputs may be in any state when the reset operation is initiated; but they must be HIGH, before the reset operation is terminated by a rising edge of $\overline{RS}$, by a time t_{RRSS} (for Read) or t_{WRSS} (for Write) respectively. (See Figure 9.)

Write

A write cycle is initiated by a falling edge of the Write ($\overline{W}$) control input. Data setup times and hold times must be observed for the data inputs ($D_0 - D_8$). Write operations may occur independently of any ongoing read operations. However, a write operation is possible only if the FIFO is not full, (i.e., if the Full Flag $\overline{FF}$ is HIGH).

At the falling edge of $\overline{W}$ for the first write operation after the memory is half filled, the Half-Full Flag is asserted ($\overline{HF}$ = LOW). It remains asserted until the difference between the write pointer and the read pointer indicates that the data words remaining in the LH540205 are filling the FIFO memory to less than or equal to one-half of its total capacity. The Half-Full Flag is deasserted ($\overline{HF}$ = HIGH) by the appropriate rising edge of $\overline{R}$. (See Table 3.)

The Full Flag is asserted ($\overline{FF}$ = LOW) at the falling edge of $\overline{W}$ for the write operation which fills the last available location in the FIFO memory array. $\overline{FF}$ = LOW inhibits further write operations until $\overline{FF}$ is cleared by a valid read operation. The Full Flag is deasserted ($\overline{FF}$ = HIGH) after the next rising edge of $\overline{R}$ releases another memory location. (See Table 3.)

Read

A read cycle is initiated by a falling edge of the Read ($\overline{R}$) control input. Read data becomes valid at the data outputs ($Q_0 - Q_8$) after a time t_A from the falling edge of $\overline{R}$. After $\overline{R}$ goes HIGH, the data outputs return to a high-impedance state. Read operations may occur independently of any ongoing write operations. However, a read operation is possible only if the FIFO is not empty (i.e., if the Empty Flag $\overline{EF}$ is HIGH).

The LH540205's internal read-address and write-address pointers operate in such a way that consecutive read operations always access data words in the same order that they were written. The Empty Flag is asserted ($\overline{EF}$ = LOW) after that falling edge of $\overline{R}$ which accesses the last available data word in the FIFO memory. $\overline{EF}$ is deasserted ($\overline{EF}$ = HIGH) after the next rising edge of $\overline{W}$ loads another valid data word. (See Table 3.)

Data Flow-Through

Read-data flow-through mode occurs when the Read ($\overline{R}$) control input is brought LOW while the FIFO is empty, and is held LOW in anticipation of a write cycle. At the end of the next write cycle, the Empty Flag $\overline{EF}$ momentarily is deasserted, and the data word just written becomes available at the data outputs ($Q_0 - Q_8$) after a maximum time of $t_{WEF} + t_A$. Additional write operations may occur while the $\overline{R}$ input remains LOW; but only data from the first write operation flows through to the data outputs. Additional data words, if any, may be accessed only by toggling $\overline{R}$.

Write-data flow-through mode occurs when the Write ($\overline{W}$) input is brought LOW while the FIFO is full, and is held LOW in anticipation of a read cycle. At the end of the read cycle, the Full Flag momentarily is deasserted, but then immediately is reasserted in response to $\overline{W}$ being held LOW. A data word is written into the FIFO on the rising edge of $\overline{W}$, which may occur no sooner than $t_{RFF} + t_{WPW}$ after the read operation.

OPERATIONAL DESCRIPTION (cont'd)

Retransmit

The FIFO can be made to reread previously-read data by means of the Retransmit function. A retransmit operation is initiated by pulsing the $\overline{RT}$ input LOW. Both $\overline{R}$ and $\overline{W}$ must be deasserted (HIGH) for the duration of the retransmit pulse. The FIFO's internal read-address pointer is reset to point to location zero, the first physical memory location, while the internal write-address pointer remains unchanged.

After a retransmit operation, those data words in the region in between the read-address pointer and the write-address pointer may be reaccessed by subsequent read operations. A retransmit operation may affect the state of the status flags $\overline{FF}$, $\overline{HF}$, and $\overline{EF}$, depending on the relocation of the read-address pointer. There is no restriction on the number of times that a block of data within an LH540205 may be read out, by repeating the retransmit operation and the subsequent read operations.

The maximum length of a data block which may be retransmitted is 8192 words. Note that if the write-address pointer ever 'wraps around' (i.e., passes location zero more than once) during a sequence of retransmit operations, some data words will be lost.

The Retransmit function is not available when the LH540205 is operating in depth-cascaded mode, because the $\overline{FL}/\overline{RT}$ control pin must be used for first-load selection rather than for retransmission control.

Table 1. Grouping-Mode Determination During a Reset Operation

$\overline{XI}$	$\overline{FL}/\overline{RT}$	MODE	$\overline{XO}/\overline{HF}$ USAGE	$\overline{XI}$ USAGE	$\overline{FL}/\overline{RT}$ USAGE
H [1]	H	Cascaded Slave [2]	$\overline{XO}$	$\overline{XI}$	$\overline{FL}$
H [1]	L	Cascaded Master [2]	$\overline{XO}$	$\overline{XI}$	$\overline{FL}$
L	X	Standalone	$\overline{HF}$	(none)	$\overline{RT}$

NOTES:
1. A reset operation forces $\overline{XO}$ HIGH for the nth FIFO, thus forcing $\overline{XI}$ HIGH for the n+1st FIFO.
2. The terms 'master' and 'slave' refer to operation in depth-cascaded grouping mode.
3. H = HIGH; L = LOW; X = Don't Care.

Table 2. Expansion-Pin Usage According to Grouping Mode

I/O	PIN	STANDALONE	CASCADED MASTER	CASCADED SLAVE
I	$\overline{XI}$	Grounded	From $\overline{XO}$ (n-1st FIFO)	From $\overline{XO}$ (n-1st FIFO)
O	$\overline{XO}/\overline{HF}$	Becomes $\overline{HF}$	To $\overline{XI}$ (n+1st FIFO)	To $\overline{XI}$ (n+1st FIFO)
I	$\overline{FL}/\overline{RT}$	Becomes $\overline{RT}$	Grounded (Logic LOW)	Logic HIGH

Table 3. Status Flags

NUMBER OF UNREAD DATA WORDS PRESENT WITHIN 8192 × 9 FIFO	$\overline{FF}$	$\overline{HF}$	$\overline{EF}$
0	H	H	L
1 to 4096	H	H	H
4097 to 8191	H	L	H
8192	L	L	H

OPERATIONAL MODES

Standalone Configuration

When depth cascading is not required for a given application, the LH540205 is placed in standalone mode by tying the Expansion In input ($\overline{XI}$) to ground. This input is internally sampled during a reset operation. (See Table 1.)

Width Expansion

Word-width expansion is implemented by placing multiple LH540205 devices in parallel. Each LH540205 should be configured for standalone mode. In this arrangement, the behavior of the status flags is identical for all devices; so, in principle, a representative value for each of these flags could be derived from any one device. In practice, it is better to derive 'composite' flag values using external logic, since there may be minor speed variations between different actual devices. (See Figures 3 and 4.)

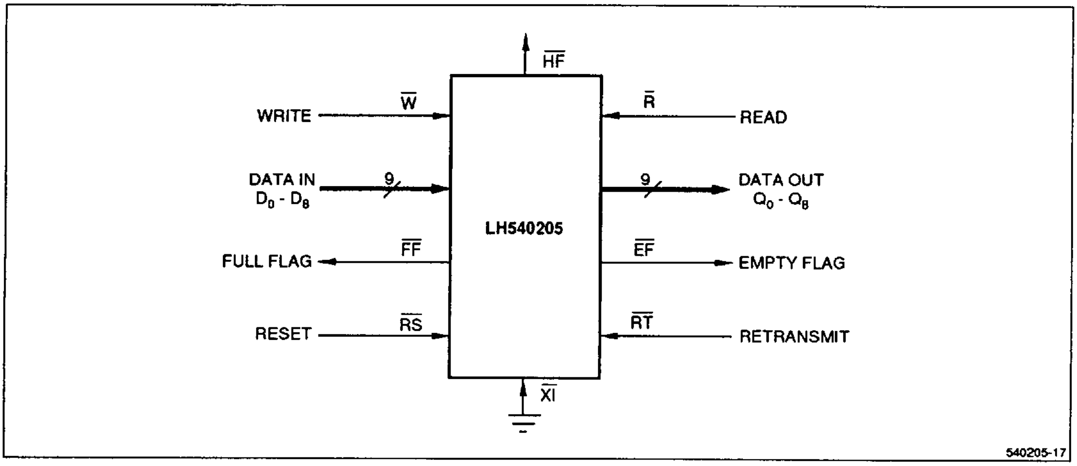

Figure 3. Standalone FIFO (8192 × 9)

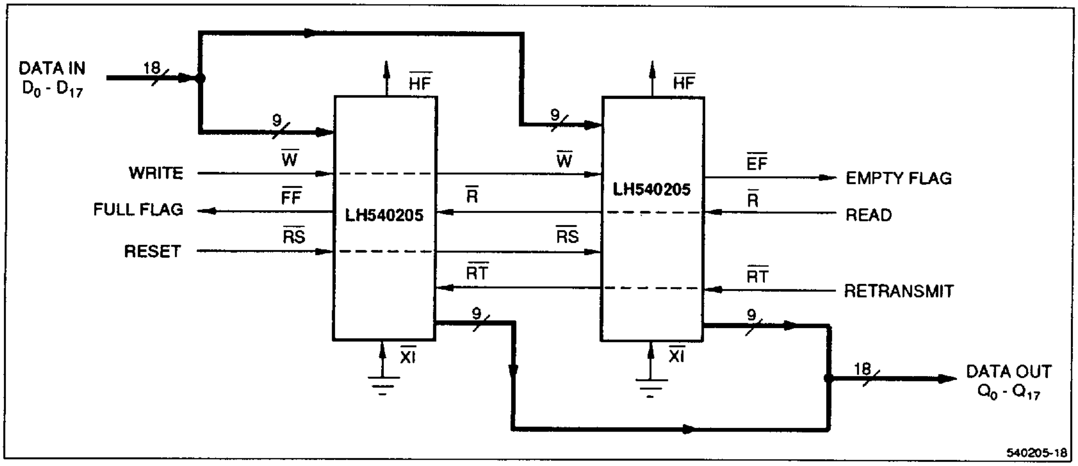

Figure 4. FIFO Word-Width Expansion (8192 × 18)

OPERATIONAL MODES (cont'd)

Depth Cascading

Depth cascading is implemented by configuring the required number of LH540205s in depth-cascaded mode. In this arrangement, the FIFOs are connected in a circular fashion, with the Expansion Out output ($\overline{XO}$) of each device tied to the Expansion In input ($\overline{XI}$) of the next device. One FIFO in the cascade must be designated as the 'first-load' device, by tying its First Load input ($\overline{FL}/\overline{RT}$) to ground. All other devices must have their $\overline{FL}/\overline{RT}$ inputs tied HIGH. In this mode, $\overline{W}$ and $\overline{R}$ signals are shared by all devices, while logic within each LH540205 controls the steering of data. Only one LH540205 is enabled during any given write cycle; thus, the common Data In inputs of all devices are tied together. Likewise, only one LH540205 is enabled during any given read cycle; thus, the common Data Out outputs of all devices are wire-ORed together

In depth-cascaded mode, external logic should be used to generate a composite Full Flag and a composite Empty Flag, by ANDing the $\overline{FF}$ outputs of all LH540205 devices together and ANDing the $\overline{EF}$ outputs of all devices together. Since $\overline{FF}$ and $\overline{EF}$ are assertive-LOW signals, this 'ANDing' actually is implemented using an assertive-HIGH physical OR gate. The Half-Full Flag and the Retransmit function are not available in depth-cascaded mode.

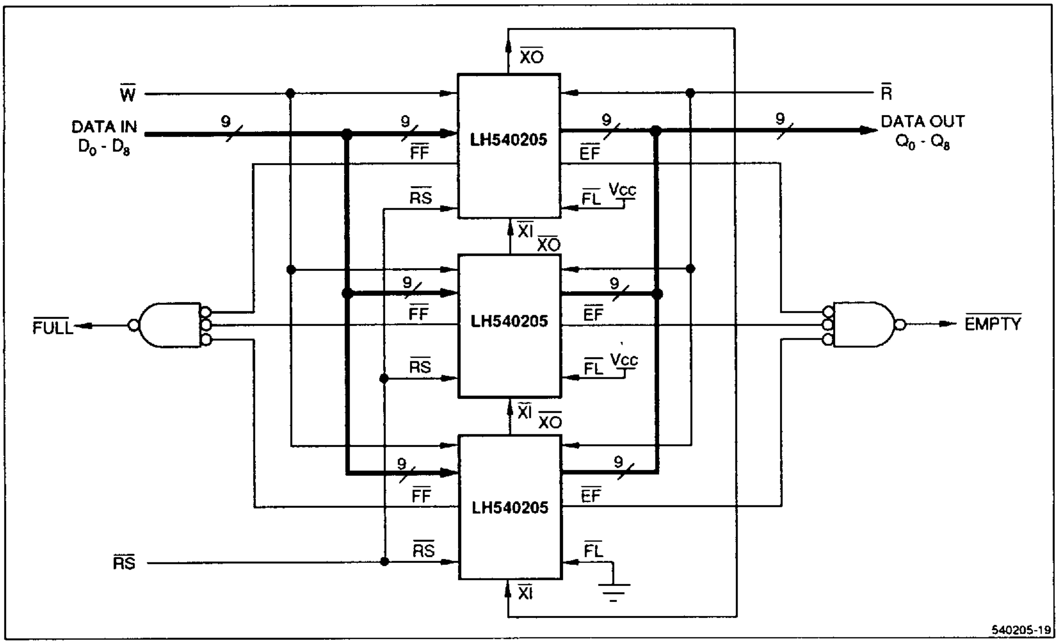

Figure 5. FIFO Depth Cascading (24576 × 9)

OPERATIONAL MODES (cont'd)

Compound FIFO Expansion

A combination of word-width expansion and depth cascading may be implemented easily by operating groups of depth-cascaded FIFOs in parallel.

Bidirectional FIFO Operation

Bidirectional data buffering between two systems may be implemented by operating LH540205 devices in parallel, but in opposite directions. The Data In inputs of each LH540205 are tied to the corresponding Data Out outputs of another LH540205, which is operating in the opposite direction, to form a single bidirectional bus interface. Care must be taken to assure that the appropriate read, write, and flag signals are routed to each system. Both word-width expansion and depth cascading may be used in bidirectional applications.

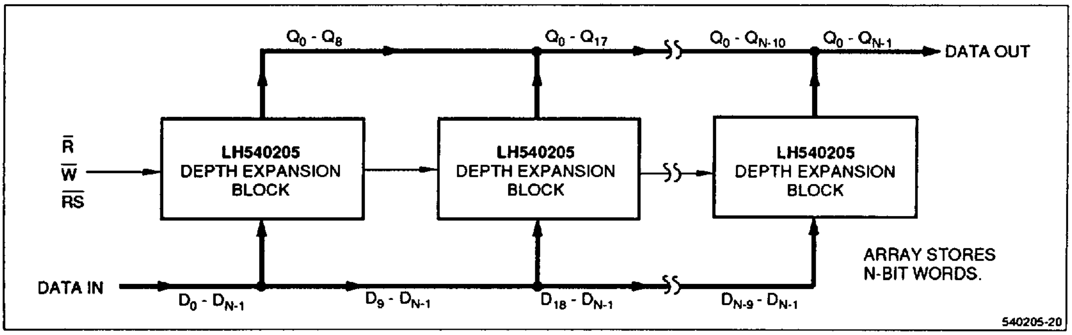

Figure 6. Compound FIFO Expansion

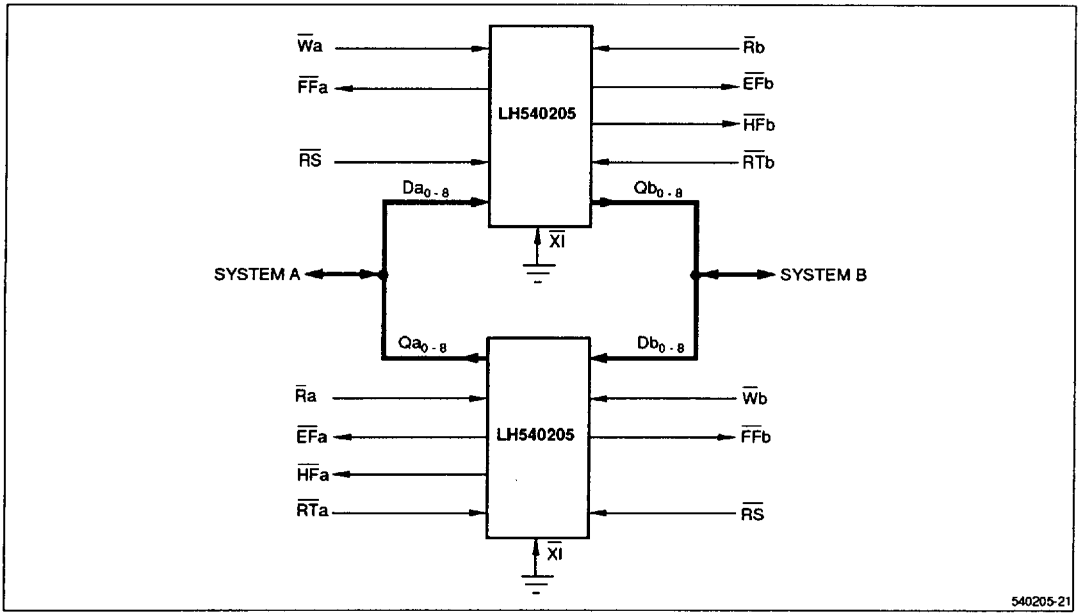

Figure 7. Bidirectional FIFO Operation
(8192 × 9 × 2)

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
Supply Voltage to V_{SS} Potential	–0.5 V to 7 V
Signal Pin Voltage to V_{SS} Potential [2]	–0.5 V to V_{CC} + 0.5 V (not to exceed 7 V)
DC Output Current [3]	± 50 mA
Storage Temperature Range	–65°C to 150°C
Power Dissipation (Package Limit)	1.0 W
DC Voltage Applied to Outputs In High-Z State	–0.5 V to V_{CC} + 0.5 V (not to exceed 7 V)

NOTES:

1. Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions outside of those indicated in the 'Operating Range' of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Negative undershoots of 1.5 V in amplitude are permitted for up to 10 ns once per cycle.
3. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.

OPERATING RANGE

SYMBOL	PARAMETER	MIN	MAX	UNIT
T_A	Temperature, Ambient	0	70	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{SS}	Supply Voltage	0	0	V
V_{IL}	Logic LOW Input Voltage [1]	–0.5	0.8	V
V_{IH}	Logic HIGH Input Voltage	2.0	V_{CC} + 0.5	V

NOTE:

1. Negative undershoots of 1.5 V in amplitude are permitted for up to 10 ns once per cycle.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
I_{LI}	Input Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	–10	10	µA
I_{LO}	Output Leakage Current	$\overline{R} \geq V_{IH}$, 0 V ≤ V_{OUT} ≤ V_{CC}	–10	10	µA
V_{OH}	Output HIGH Voltage	I_{OH} = –2.0 mA	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 8.0 mA		0.4	V
I_{CC}	Average Supply Current [1]	Measured at f = 33 MHz		110	mA
I_{CC2}	Average Standby Current [1]	All Inputs = V_{IH}		15	mA
I_{CC3}	Power Down Current [1]	All Inputs = V_{CC} – 0.2V		8	mA

NOTE:

1. I_{CC}, I_{CC2}, and I_{CC3} are dependent upon actual output loading and cycle rates. Specified values are with outputs open.

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AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	V_{SS} to 3 V
Input Rise and Fall Times (10% to 90%)	5 ns
Input Timing Reference Levels	1.5 V
Output Reference Levels	1.5 V
Output Load, Timing Tests	Figure 8

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} MAX (Input Capacitance)	5 pF
C_{O} MAX (Output Capacitance)	7 pF

NOTES:
1. Sample tested only.
2. Capacitances are maximum values at 25°C, measured at 1.0MHz, with V_{IN} = 0 V.

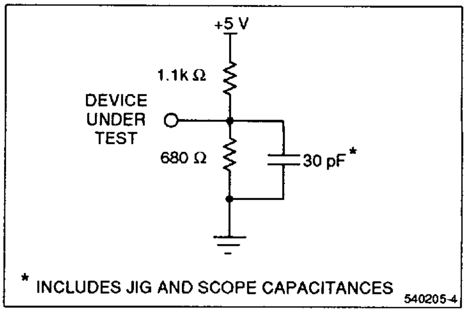


Figure 8. Output Load Circuit

SHARP CORP

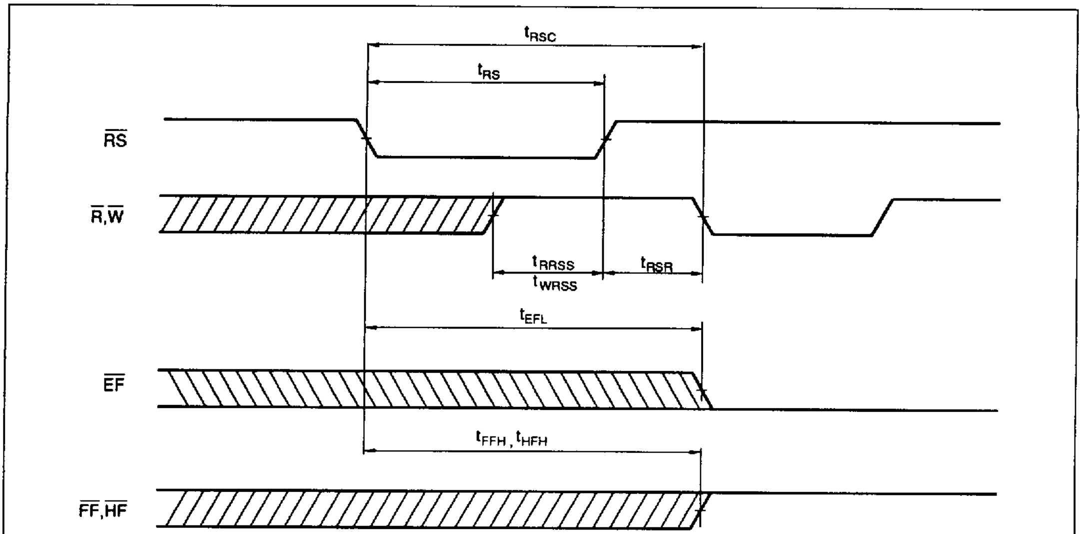
AC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range)

SYMBOL	PARAMETER	t_A = 20 ns		t_A = 25 ns		t_A = 35 ns		t_A = 50 ns		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
READ CYCLE TIMING										
t_{RC}	Read Cycle Time	30	–	35	–	45	–	65	–	ns
t_A	Access Time	–	20	–	25	–	35	–	50	ns
t_{RR}	Read Recovery Time	10	–	10	–	10	–	15	–	ns
t_{RPW}	Read Pulse Width [2]	20	–	25	–	35	–	50	–	ns
t_{RLZ}	Data Bus Active from Read LOW [3]	5	–	5	–	5	–	5	–	ns
t_{WLZ}	Data Bus Active from Write HIGH [3,4]	10	–	10	–	10	–	10	–	ns
t_{DV}	Data Held Valid from Read Pulse HIGH	5	–	5	–	5	–	5	–	ns
t_{RHZ}	Data Bus High-Z from Read HIGH [3]	–	15	–	15	–	15	–	20	ns
WRITE CYCLE TIMING										
t_{WC}	Write Cycle Time	30	–	35	–	45	–	65	–	ns
t_{WPW}	Write Pulse Width [2]	20	–	25	–	35	–	50	–	ns
t_{WR}	Write Recovery Time	10	–	10	–	10	–	15	–	ns
t_{DS}	Data Setup Time	10	–	10	–	15	–	20	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	ns
RESET TIMING										
t_{RSC}	Reset Cycle Time	30	–	35	–	45	–	65	–	ns
t_{RS}	Reset Pulse Width [2]	20	–	25	–	35	–	50	–	ns
t_{RSR}	Reset Recovery Time	10	–	10	–	10	–	15	–	ns
t_{RRSS}	Read HIGH to $\overline{RS}$ HIGH	20	–	25	–	35	–	50	–	ns
t_{WRSS}	Write HIGH to $\overline{RS}$ HIGH	20	–	25	–	35	–	50	–	ns
RETRANSMIT TIMING [5]										
t_{RTC}	Retransmit Cycle Time	30	–	35	–	45	–	65	–	ns
t_{RT}	Retransmit Pulse Width [2]	20	–	25	–	35	–	50	–	ns
t_{RTR}	Retransmit Recovery Time	10	–	10	–	10	–	15	–	ns
FLAG TIMING										
t_{EFL}	Reset LOW to Empty Flag LOW	–	30	–	35	–	45	–	65	ns
$t_{HFH,FFH}$	Reset HIGH to Half-Full and Full Flags HIGH	–	30	–	35	–	45	–	65	ns
t_{REF}	Read LOW to Empty Flag LOW	–	20	–	25	–	35	–	45	ns
t_{RFF}	Read HIGH to Full Flag HIGH	–	20	–	25	–	35	–	45	ns
t_{WEF}	Write HIGH to Empty Flag HIGH	–	20	–	25	–	35	–	45	ns
t_{WFF}	Write LOW to Full Flag LOW	–	20	–	25	–	35	–	45	ns
t_{WHF}	Write LOW to Half-Full Flag LOW	–	20	–	25	–	35	–	45	ns
t_{RHF}	Read HIGH to Half-Full Flag HIGH	–	20	–	25	–	35	–	45	ns
EXPANSION TIMING										
t_{XOL}	Expansion Out LOW	–	20	–	25	–	35	–	50	ns
t_{XOH}	Expansion Out HIGH	–	20	–	25	–	35	–	50	ns
t_{XI}	Expansion In Pulse Width	20	–	25	–	35	–	50	–	ns
t_{XIR}	Expansion In Recovery Time	10	–	10	–	10	–	10	–	ns
t_{XIS}	Expansion in Setup Time	10	–	10	–	15	–	15	–	ns

NOTES:

1. All timing measurements are performed at 'AC Test Condition' levels.
2. Pulse widths less than minimum value are not allowed.
3. Values are guaranteed by design; not currently tested.
4. Only applies to read-data flow-through mode.
5. See also Note 2, Figure 18.

TIMING DIAGRAMS



NOTES:

1. $t_{RSC} = t_{RS} + t_{RSR}$.
2. $\overline{W}$ and $\overline{R} \geq V_{IH}$ around the rising edge of $\overline{RS}$.

Figure 9. Reset Timing

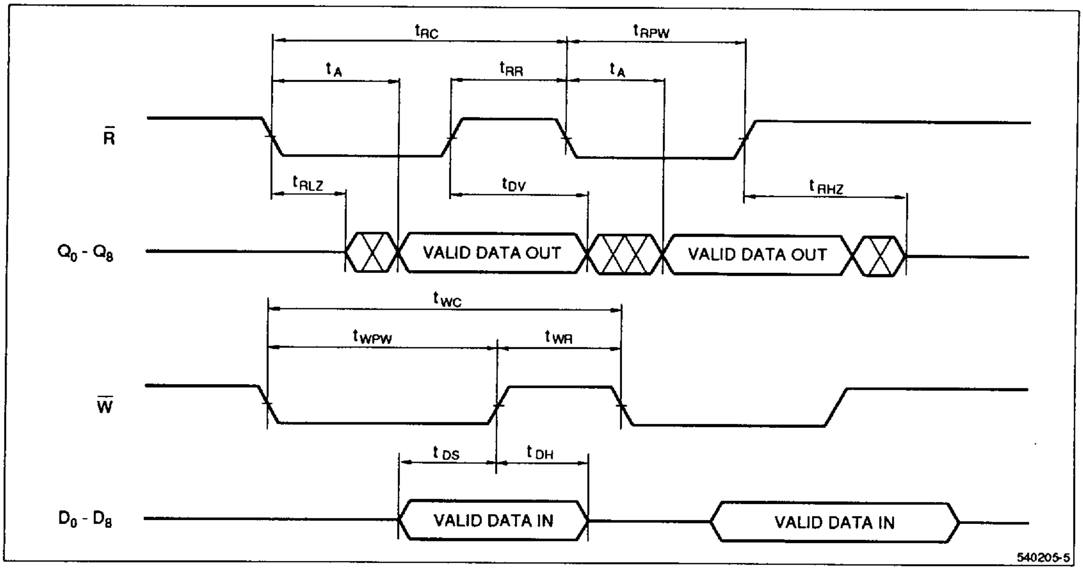


Figure 10. Asynchronous Write and Read Operation

TIMING DIAGRAMS (cont'd)

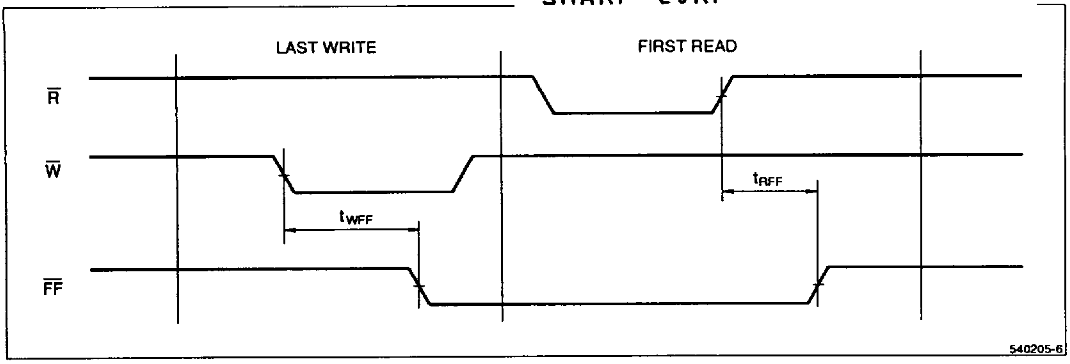


Figure 11. Full Flag From Last Write to First Read

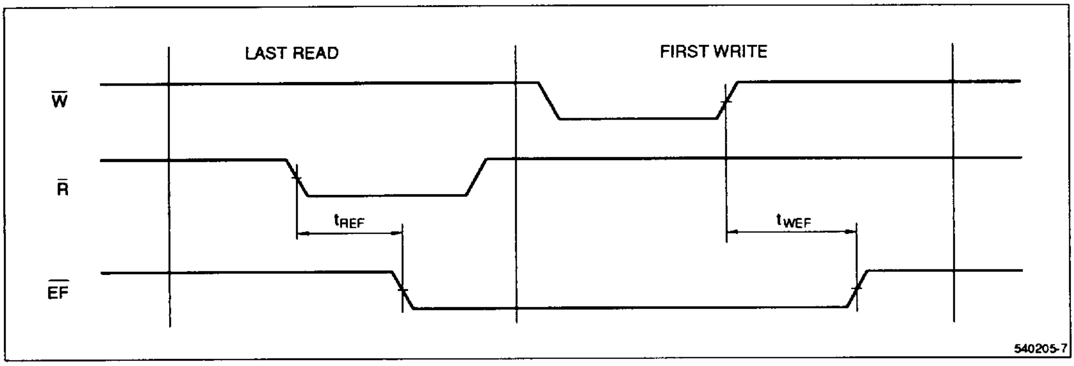
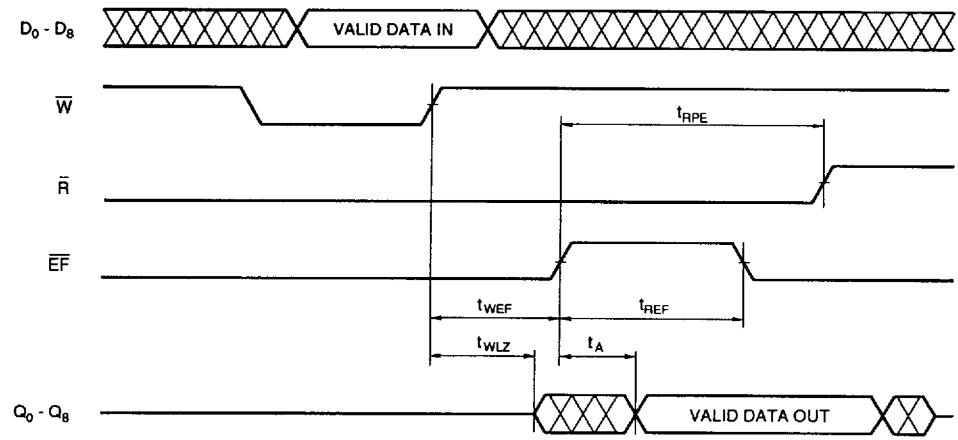


Figure 12. Empty Flag From Last Read to First Write

TIMING DIAGRAMS (cont'd)



NOTES:
1. $t_{RPE} = t_{RPW}$.
2. t_{RPE}: Effective Read Pulse Width after Empty Flag HIGH.

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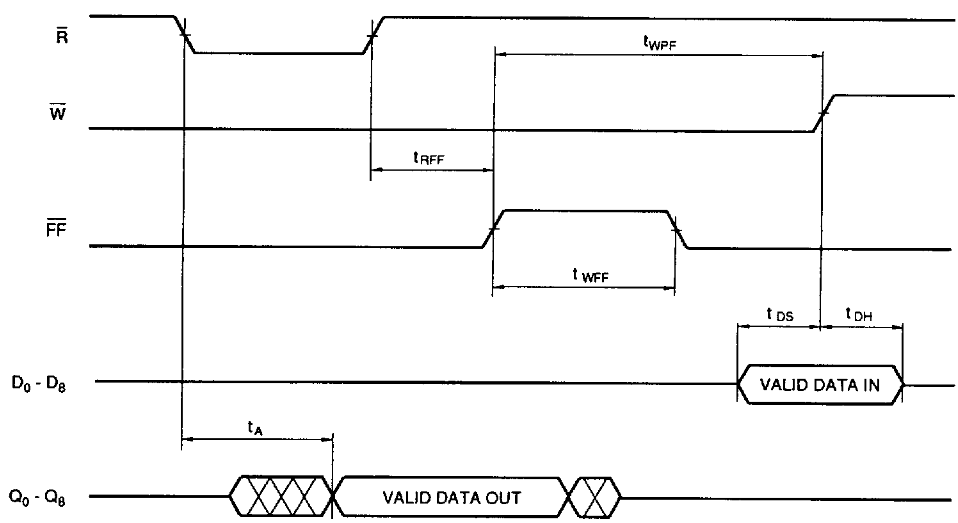
Figure 13. Read Data Flow-Through



NOTES:
1. $t_{WPF} = t_{WPW}$.
2. t_{WPF}: Effective Write Pulse Width after Full Flag HIGH.

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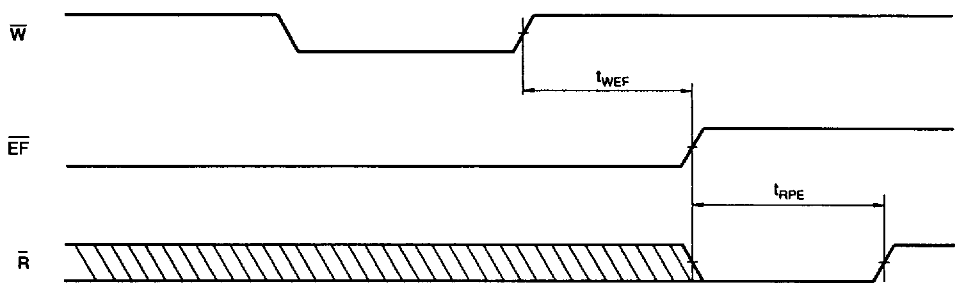
Figure 14. Write Data Flow-Through

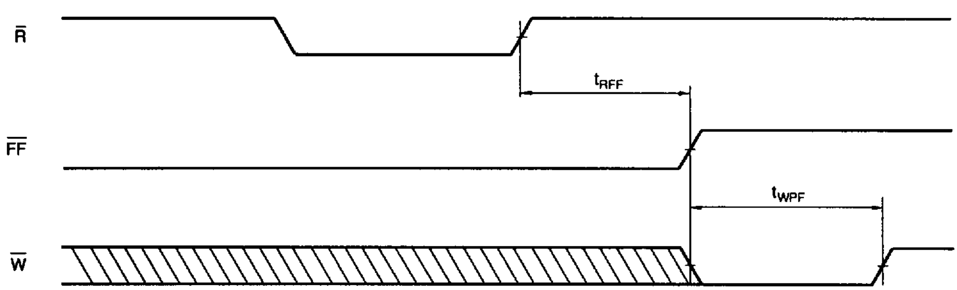
TIMING DIAGRAMS (cont'd)



NOTES:
1. $t_{RPE} = t_{RPW}$.
2. t_{RPE}: Effective Read Pulse Width after Empty Flag HIGH.

540205-10

Figure 15. Empty Flag Timing



NOTES:
1. $t_{WPF} = t_{WPW}$.
2. t_{WPF}: Effective Write Pulse Width after Full Flag HIGH.

540205-11

Figure 16. Full Flag Timing

TIMING DIAGRAMS (cont'd)

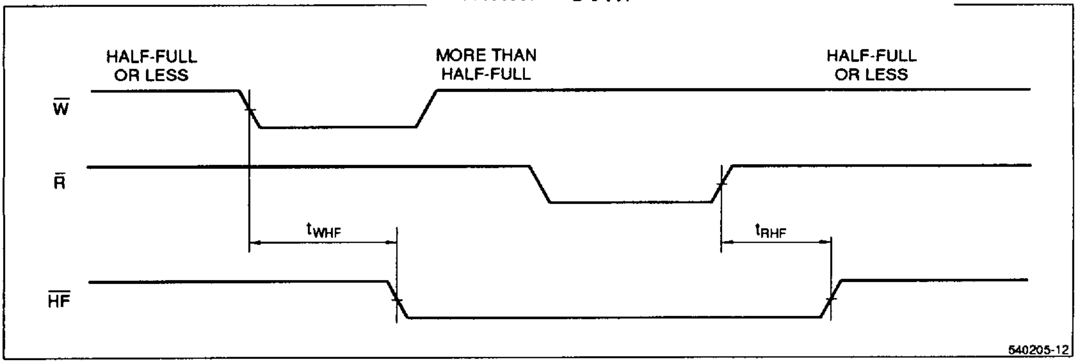
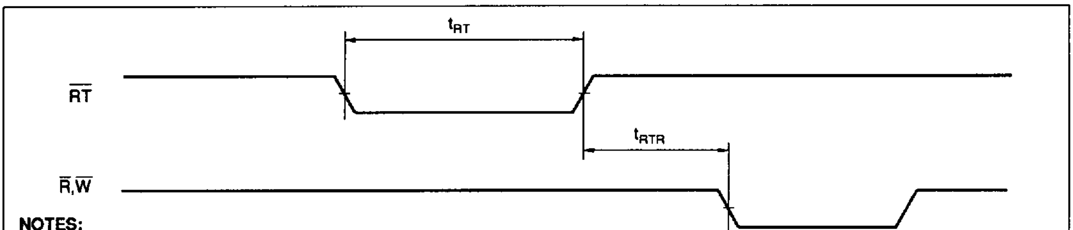


Figure 17. Half-Full Flag Timing



NOTES:

1. $t_{RTC} = t_{RT} + t_{RTR}$.
2. $\overline{FF}$, $\overline{HF}$, and $\overline{EF}$ may change state during retransmit; but they will become valid by t_{RTC}.

540205-13

Figure 18. Retransmit Timing

TIMING DIAGRAMS (cont'd)

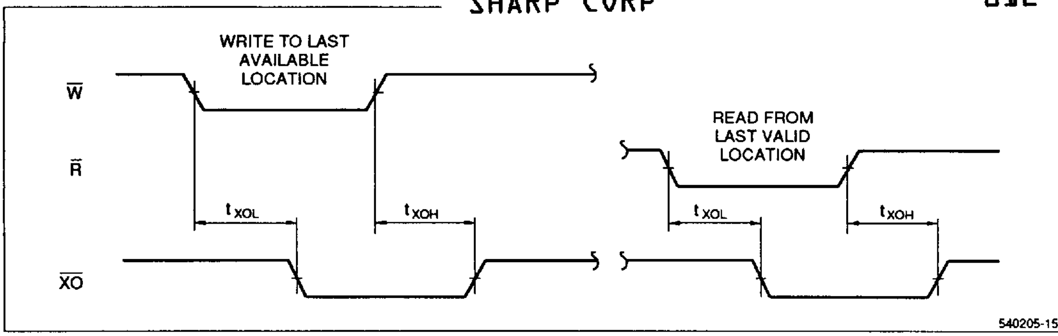


Figure 19. Expansion-Out Timing

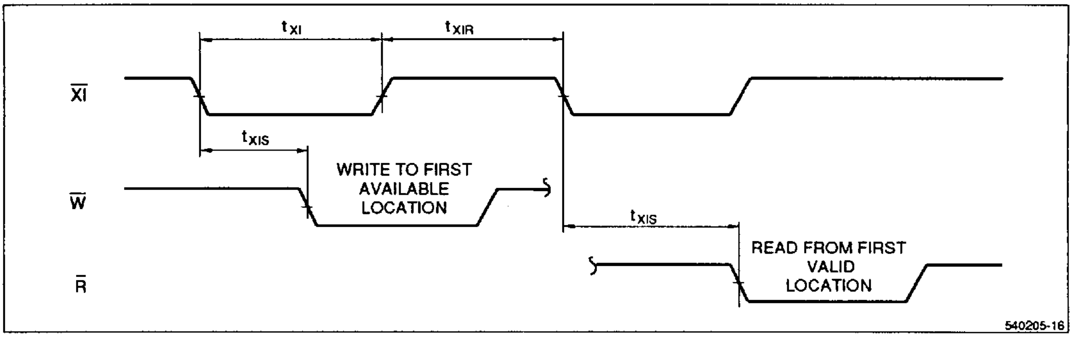


Figure 20. Expansion-In Timing

ORDERING INFORMATION

LH540205	X	- ##
Device Type	Package	Speed

Speed: 20, 25, 35, 50 — Access Time (ns)

Package:
- Blank 28-pin, 600-mil Plastic DIP * (DIP28-P-600)
- D 28-pin, 300-mil Plastic DIP (DIP28-W-300)

Device Type: CMOS 8192 x 9 FIFO

* This is an Advance information data sheet; except that all references to the 600-mil Plastic DIP package still have Product Preview status.

Example: LH540205-25 (CMOS 8192 x 9 FIFO, 28-pin, 600-mil DIP, 25 ns)

540205MD