LH540206

PRODUCT PREVIEW

CMOS 16384 × 9 Asynchronous FIFO

FEATURES

- Fast Access Times: 20/25/35/50/65/80 ns
- Fast-Fall-Through Time Architecture Based on CMOS Dual-Port SRAM Technology
- Input Port and Output Port Have Entirely Independent Timing
- Expandable in Width and Depth
- Full, Half-Full, and Empty Status Flags
- Data Retransmission Capability
- TTL-Compatible I/O
- Pin and Functionally Compatible with IDT7206
- Pin and Functionally Compatible, Except for Depth, With Smaller Industry-Standard ×9 Asynchronous FIFOs, Such as IDT7201 Series, and Sharp LH5496 and LH540201 Series
- Control Signals Assertive-LOW for Noise Immunity
- Packages:
  28-Pin, 300-mil PDIP
  28-Pin, 600-mil PDIP

FUNCTIONAL DESCRIPTION

The LH540206 is a FIFO (First-In, First-Out) memory device, based on fully-static CMOS dual-port SRAM technology, capable of storing up to 16384 nine-bit words. It follows the industry-standard architecture and package pinouts for nine-bit asynchronous FIFOs. Each nine-bit LH540206 word may consist of a standard eight-bit byte, together with a parity bit or a block-marking/framing bit.

The input and output ports operate entirely independently of each other, unless the LH540206 becomes either totally full or else totally empty. Data flow at a port is initiated by asserting either of two asynchronous, assertive-LOW control inputs: Write ($\overline{W}$) for data entry at the input port, or Read ($\overline{R}$) for data retrieval at the output port.

Full, Half-Full, and Empty status flags monitor the extent to which the internal memory has been filled. The system may make use of these status outputs to avoid the risk of data loss, which otherwise might occur either by attempting to write additional words into an already-full LH540206, or by attempting to read additional words from an already-empty LH540206. When an LH540206 is operating in a depth-cascaded configuration, the Half-Full Flag is not available.

Data words are read out from the LH540206's output port in precisely the same order that they were written in at its input port; that is, according to a First-In, First Out (FIFO) queue discipline. Since the addressing sequence for a FIFO device's memory is internally predefined, no external addressing information is required for the operation of the LH540206 device.

Drop-in-replacement compatibility is maintained with both larger sizes and smaller sizes of industry-standard nine-bit asynchronous FIFOs. The only change is in the number of internally-stored data words implied by the states of the Full Flag and the Half-Full Flag.

The Retransmit ($\overline{RT}$) control signal causes the internal FIFO-memory-array read-address pointer to be set back to zero, to point to the LH540206's first physical memory location, without affecting the internal FIFO-memory-array write-address pointer. Thus, the Retransmit control signal provides a mechanism whereby a block of data, delimited by the zero physical address and the current write-address-pointer value, may be read out *repeatedly* an arbitrary number of times. The only restrictions are that neither the read-address pointer nor the write-address pointer may 'wrap around' during this entire process, i.e., advance past physical location zero after traversing the entire memory. The retransmit facility is not available when an LH540206 is operating in a depth-expanded configuration.

PIN CONNECTIONS

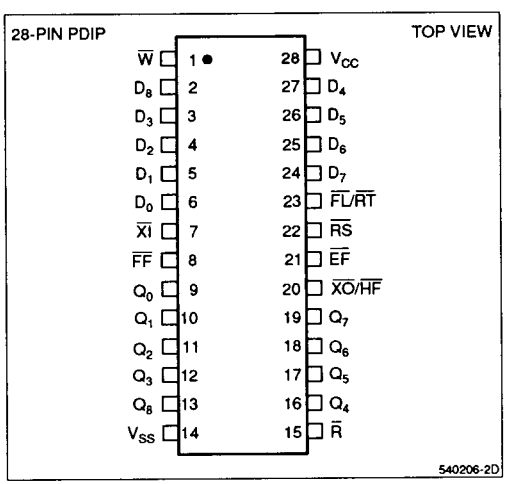

Figure 1. Pin Connections for PDIP Package

FUNCTIONAL DESCRIPTION (cont'd)

The Reset ($\overline{RS}$) control signal returns the LH540206 to an initial state, empty and ready to be filled. An LH540206 should be reset during every system power-up sequence. A reset operation causes the internal FIFO-memory-array write-address pointer, as well as the read-address pointer, to be set back to zero, to point to the LH540206's first physical memory location. Any information which previously had been stored within the LH540206 is not recoverable after a reset operation.

A cascading (depth-expansion) scheme may be implemented by using the Expansion In ($\overline{XI}$) input signal and the Expansion Out ($\overline{XO/HF}$) output signal. This scheme allows a deeper 'effective FIFO' to be implemented by using two or more individual LH540206 devices, without incurring additional latency ('fallthrough' or 'bubblethrough') delays, and without the necessity of storing and retrieving any given data word more than once. In this cascaded operating mode, one LH540206 device must be designated as the 'first-load' or 'master' device, by grounding its First-Load ($\overline{FL/RT}$) control input; the remaining LH540206 devices are designated as 'slaves,' by tying their $\overline{FL/RT}$ inputs HIGH. Because of the need to share control signals on pins, the Half-Full Flag and the retransmission capability are not available for either 'master' or 'slave' LH540206 devices operating in cascaded mode.

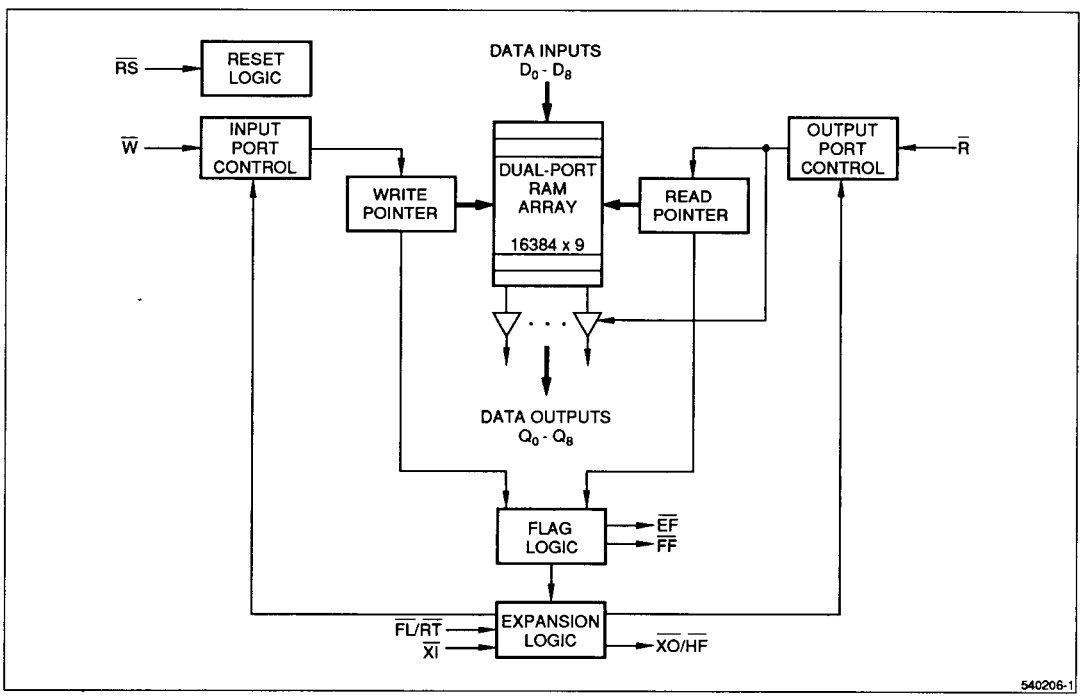

Figure 2. LH540206 Block Diagram