Preferred Device

Product Preview

TMOS 7 E-FET™ Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate

This advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls. These devices are particularly well–suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

New Features of TMOS 7

- Ultra Low On–Resistance Provides Higher Efficiency
- Reduced Gate Charge

Features Common to TMOS 7 and TMOS E-FETS

- Avalanche Energy Specified
- Diode Characterized for Use in Bridge Circuits
- IDSS and VDS(on) Specified at Elevated Temperature

MAXIMUM RATINGS ($T_C = 25^{\circ}C$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-Source Voltage	V _{DSS}	600	Vdc
Drain–Gate Voltage ($R_{GS} = 1.0 \text{ M}\Omega$)	V _{DGR}	600	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive (t _p ≤ 10 ms)	V _{GS} V _{GSM}	±20 ±40	Vdc
Drain — Continuous — Continuous @ 100°C — Single Pulse (t _p ≤10 μs)	I _D	6.0 4.8 21	Adc
Total Power Dissipation Derate above 25°C	PD	142 1.14	Watts W/°C
Operating and Storage Temperature Range	T _J , T _{stg}	-55 to 150	°C
Single Drain-to-Source Avalanche Energy — Starting T _J = 25°C (V _{DD} = 100 V, V _{GS} = 10 Vdc, I _L = 6 A, L = 25 mH, R _G = 25 Ω)	EAS	450	mJ
Thermal Resistance — Junction-to-Case — Junction-to-Ambient	R _θ JC R _θ JA	0.88 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	TL	260	°C

This document contains information on a new product. Specifications and information herein are subject to change without notice.



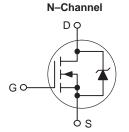
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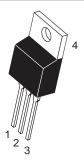
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TMOS POWER FET 6 AMPERES 600 VOLTS

RDS(on) = 1.2 Ω







TO-220AB CASE 221A STYLE 5

PIN ASSIGNMENT		
1	Gate	
2	Drain	
3	Source	
4	Drain	

ORDERING INFORMATION

Device	Package	Shipping
NTP6N60	TO220AB	50 Units/Rail

Preferred devices are recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS ($T_C = 25$ °C unless otherwise noted)

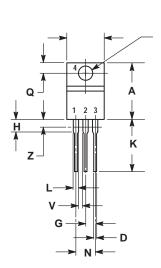
CI	Symbol	Min	Тур	Max	Unit	
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage		V(BR)DSS	600			Vdc
(VGS = 0 Vdc, ID = 0.25 mAd Temperature Coefficient (Pos		600 —	715		mV/°C	
Zero Gate Voltage Collector Cu (V _{DS} = 600 Vdc, V _{GS} = 0 Vd		IDSS	_	_	10	μAdc
$(V_{DS} = 600 \text{ Vdc}, V_{GS} = 0 \text{ Vd})$				_	100	
Gate-Body Leakage Current (\	$V_{GS} = \pm 20 \text{ Vdc}, V_{DS} = 0)$	IGSS(f)	_ _	_	100 100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage		V _{GS(th)}				Vdc
ID = 0.25 mA, VDS = VGS	rativo)		2.0	2.6 6.6	4.0 —	mV/°C
Temperature Coefficient (Negative)						-
	sistance (V _{GS} = 10 Vdc, I _D = 3 Adc)	R _{DS(on)}	_	0.85	1.2	Ohm
Drain-to-Source On-Voltage (V _{GS} = 10 Vdc, I _D = 6 Adc)		V _{DS(on)}	_	_	7.9	Vdc
$(V_{GS} = 10 \text{ Vdc}, I_{D} = 3 \text{ Adc}, T_{D} = $	Г _Ј = 125°С)		_	_	6.9	
Forward Transconductance (Vps = 15 Vdc, Ip = 3 Adc)		9FS	2.0	7.0	_	mhos
YNAMIC CHARACTERISTICS						
Input Capacitance		C _{iss}	_	1190	1670	pF
Output Capacitance	$(V_{DS} = 25 \text{ Vdc}, V_{GS} = 0 \text{ Vdc}, f = 1.0 \text{ MHz})$	C _{oss}	_	350	490	
Transfer Capacitance	I = 1.0 MH2)	C _{rss}		20	40	
WITCHING CHARACTERISTIC	CS (2)	100				
Turn-On Delay Time		^t d(on)	_	11	20	ns
Rise Time	$(V_{DD} = 300 \text{ Vdc}, I_{D} = 6 \text{ Adc},$	t _r	_	10	20	1
Turn-Off Delay Time	$V_{GS} = 10 \text{ Vdc},$ $R_{G} = 9.1 \Omega)$	t _{d(off)}		34	70	1
Fall Time	- NG = 3.1 <u>12</u>)	t _f		19	40	
Gate Charge	(V _{DS} = 400 Vdc, I _D = 6 Adc, V _{GS} = 10 Vdc)	Q _T		24	30	nC
· ·		Q ₁		6.0		-
		Q ₂		8.0		
		Q ₃		12	_	ł
OURCE-DRAIN DIODE CHAR	ACTEDISTICS	۷3		12		
Forward On–Voltage(1)	ACTERISTICS	V _{SD}				Vdc
Tornara on Vollago	$(I_S = 6 \text{ Adc}, V_{GS} = 0 \text{ Vdc})$	1 ,20	_	0.85	1.0	"
	$(I_S = 6 \text{ Adc}, V_{GS} = 0 \text{ Vdc}, T_J = 125^{\circ}\text{C})$		_	0.73		
Reverse Recovery Time		t _{rr}		440	_	ns
	$(I_S = 6 \text{ Adc}, V_{GS} = 0 \text{ Vdc},$	ta	_	130	_	
	dig/dt = 100 A/µs	t _b	_	310	_	
Reverse Recovery Stored Charge		Q _{RR}	_	2.8	_	μС
NTERNAL PACKAGE INDUCTA	ANCE			•		
Internal Drain Inductance (Measured from contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)		L _D				nH
			_	3.5 4.5	_	
	a o.20 Horri package to certer or die)	I	_	٠.٠	_	I
Internal Source Inductance	, ,	LS				1

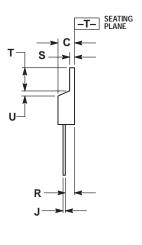
Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
 Switching characteristics are independent of operating junction temperature.

PACKAGE DIMENSIONS

TO-220AB CASE 221A-09

ISSUE Z





- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
Α	0.570	0.620	14.48	15.75
В	0.380	0.405	9.66	10.28
С	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
Н	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045		1.15	
Z		0.080		2.04

- STYLE 5:
 PIN 1. GATE
 2. DRAIN
 3. SOURCE
 4. DRAIN

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001-800-4422-3781 Email: ONlit-asia@hibbertco.com

JAPAN: ON Semiconductor, Japan Customer Focus Center 4-32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan 141-8549

Phone: 81-3-5740-2745 Email: r14525@onsemi.com

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