Mosaic Semiconductor Inc.

PUMA 2F4000

PUMA 2F4000-12/15/20

Issue 1.1 : April 1991

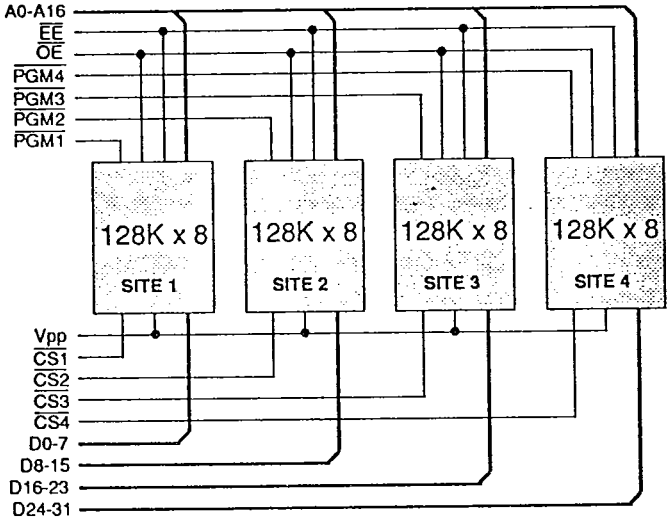
ADVANCE PRODUCT INFORMATION

4,194,304 bit CMOS High Speed FLASH EEPROM

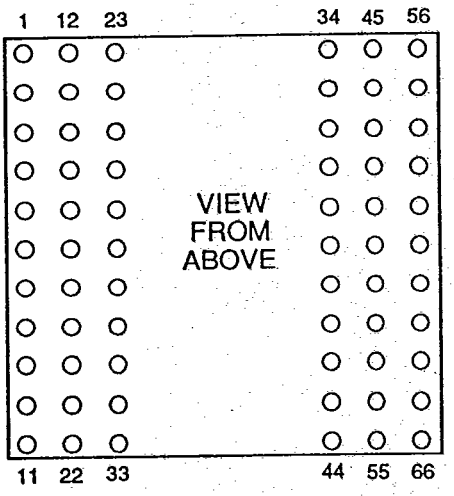
Features

FLASH Eraseable Non-volatile Memory.
User Configurable as 8,16 or 32 bit wide.
Fast access times of 120/150/200 ns.
Operating Power 600mW (typ), 32 bit mode.
300mW (typ), 16 bit mode.
150mW (typ), 8 bit mode.
Low Power Standby 400µW (max).
Single High Voltage for Erase/Write : V_{PP}=12.0V±0.4V.
Byte Program (200µs) and Chip Erase (2 sec. typ).
More than 100 Write/Erase Cycle Endurance.
Single Erase Enable pin for simple operation.
On board decoupling capacitors.
May be screened in accordance with MIL-STD-883C.

Block Diagram



Pin Definition

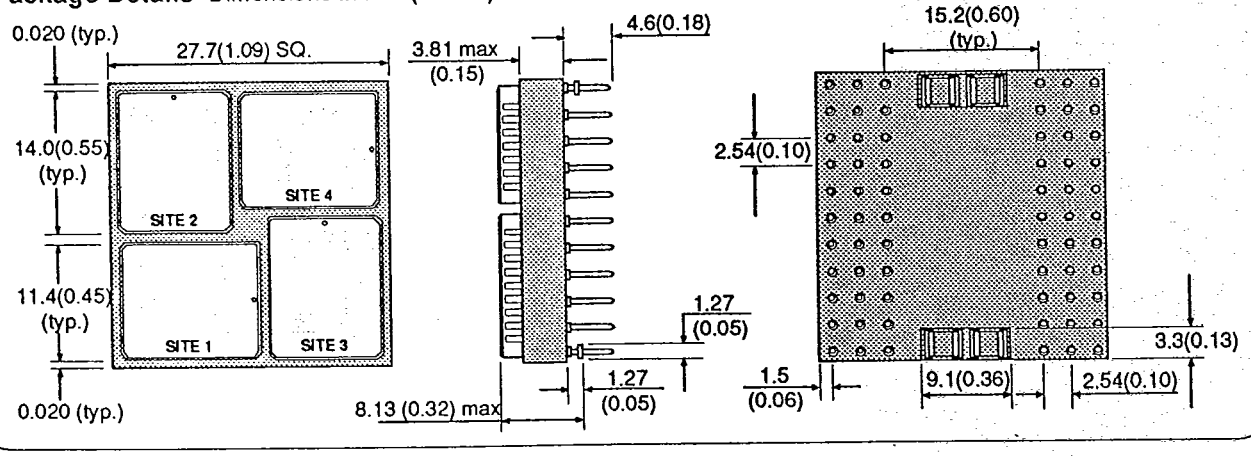


For pinout see page 7

Pin Functions

A0-16	Address Inputs
D0-D32	Data Inputs/Outputs
$\overline{CS1-4}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{PGM1-4}$	Programming Enable
$\overline{EE}$	Erase Enable
V_{PP}	Programming Voltage
V_{CC}	Power (+5V)
GND	Ground
NC	No Connect

Package Details Dimensions in mm (inches).



Module Operation

The PUMA 2F4000 is a 4,194,304 bit CMOS FLASH Electrical Eraseable and Programmable ROM. This module is configurable as 8, 16 or 32 bit wide output by using $\overline{CS1\text{-}4}$, allowing flexibility in a wide range of applications.

A high voltage (12V) on V_{PP} allows each device on the PUMA to be Byte Programmed or each entire chip to be Erased, with the end of erase indicated by D7 toggling from a "0" to a "1". During this erase time (2 seconds typ.) all control pins, address and data bus become free by control latch.

A single Erase Enable ($\overline{EE}$) pin is provided to control the Chip Erase function, and using this pin in conjunction with the other control pins means that command register operation is unnecessary.

Absolute Maximum Ratings (1)

Supply Voltage (2)	V_{CC}	-0.6 to +7.0	V
Programming Voltage	V_{PP}	-0.6 to +13.0	V
Input Voltage (2)	V_{IN}	-0.6 to +6.25	V
Operating Temperature	T_{OPR}	-60 to +140	°C
Storage Temperature	T_{STG}	-65 to +150	°C

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) Pulse Width: -2.0V for less than 20ns.

Recommended Operating Conditions

		min	*typ*	*max*	
DC Logic Supply Voltage	V_{CC}	4.5	5.0	5.5	V
DC EPROM Program Voltage	V_{PP}	11.6	12.0	12.4	V
Input High Voltage	V_{IH}	2.4	-	V_{CC}+1	V
Input Low Voltage	V_{IL}	-0.3	-	0.45	V
Operating Temperature(1)	T_A	0	-	70	°C
	T_{AI}	-40	-	85	°C (2F4000I)
	T_{AM}	-55	-	125	°C (2F4000M,MB)

Note: (1) When programming a 0.1µF high frequency by-pass capacitor is required across V_{PP} and GND to suppress noise transients

Operating Modes

The Table below show the logic inputs required to control the operating modes of each FLASH EEPROM on the PUMA2F4000.

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{PGM}$	$\overline{EE}$	V_{CC}	V_{PP}	*Outputs*
Read	0	0	1	1	5V	5V	Data Out
Output Disable	0	1	X	X	5V	5V	High Impedance
	0	0	0	X	5V	5V	High Impedance
	0	0	1	0	5V	5V	High Impedance
Standby	1	X	X	X	5V	5V	High Impedance
Program	0	1	0	1	5V	12V	Data In
Erase	0	1	1	0	5V	12V	High Impedance
Inhibit	0	1	1	1	5V	12V	High Impedance
	0	0	0	X	5V	12V	High Impedance
	0	1	0	0	5V	12V	High Impedance
	1	X	X	X	5V	12V	High Impedance
Erase Wait	1	X	X	X	5V	12V	High Impedance
Status Polling	0	0	1	0	5V	12V	D7 "0" to "1"
Program Verify Erase Verify	0	0	1	1	5V	12V	Data Out

1 = V_{IIH}
0 = V_{IL}
X = V_{IH} or V_{IL}
5V = 5.0V±10%
12V = 12.0V±0.4V

READ OPERATION

DC Electrical Characteristics (T_A= -55°C to +125°C, V_{CC}=5V±10%, V_{PP}=V_{CC}-1V to V_{CC})

Parameter		*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
Input Leakage Current		I_{IN1}	V_{IN}=5.25V, Address, $\overline{OE}$, $\overline{EE}$	-	-	8	µA
		I_{IN2}	$\overline{CS1\text{-}4}$, $\overline{PGM1\text{-}4}$	-	-	2	µA
Output Leakage Current		I_{OUT}	V_{OUT}=0 to V_{CC}	-	-	8	µA
V_{PP} Leakage Current		I_{PP}	V_{PP}=5.5V	-	-	80	µA
Standby Supply Current		I_{SB1}	$\overline{CS1\text{-}4}$=V_{IH}	-	-	4	mA
		I_{SB2}	$\overline{CS1\text{-}4}$=V_{CC} ±0.3V, I_{OUT}=0mA	-	-	80	µA
Operating Supply Current	8 BIT	I_{CCO1}	f=1MHz, I_{OUT}=0mA	-	23	-	mA
	16 BIT	I_{CCO2}	As I_{CCO1}	-	42	-	mA
	32 BIT	I_{CCO3}	As I_{CCO1}	-	80	-	mA
	8 BIT	I_{CCO4}	f=8MHz, I_{OUT}=0mA	-	33	-	mA
	16 BIT	I_{CCO5}	As I_{CCO4}	-	62	-	mA
	32 BIT	I_{CCO6}	As I_{CCO4}	-	120	-	mA
Input Low Voltage		V_{IL}	Notes (1,3)	-0.3	-	0.8	V
Input High Voltage		V_{IH}	Notes (2,3)	2.2	-	V_{CC}+1	V
Output LowVoltage		V_{OL}	I_{OL}=2.1mA	-	-	0.45	V
Output HighVoltage		V_{OH}	I_{OH}=-400µA	2.4	-	-	V

Notes (1) -1.0V for pulse width ≤ 50 ns
(2) Vcc+1.5V for pulse width ≤20 ns. If V_{IH} is over the specified max. value, READ operation cannot be guaranteed.
(3) Only defined for DC and long cycle funcion test. V_{IL} max = 0.45V, V_{IH} min = 2.4V for AC function test.

Capacitance (T_A=25°C, f=1MHz)

Parameter	*Symbol*	*Test Condition*	*typ*	*max*	*Unit*
Input Capacitance:	C_{IN}	V_{IN}=0V, 8 bit mode	-	24	pF
Output Capacitance:	C_{OUT}	V_{OUT}=0V, 8 bit mode	-	48	pF

Note: Capacitance calculated not measured.

AC Characteristics

		-12		*-15*		*-20*		
Parameter	*Symbol*	*min*	*max*	*min*	*max*	*min*	*max*	*Unit*
Address to Output Delay	t_{ACC}	-	120	-	150	-	200	ns
$\overline{CS1\text{-}4}$ to Output Delay	t_{CE}	-	120	-	150	-	200	ns
$\overline{OE}$ to Output Delay	t_{OE}	-	65	-	70	-	80	ns
$\overline{OE}$ High to Output Float	t_{DF}	5	50	5	50	5	50	ns
Address to Output Hold	t_{OH}	0	-	0	-	0	-	ns

NOTE : T_{DF} not measured but guaranteed by design.

AC Test Conditions

* Input pulse levels: 0.45V to 2.4V
* Input rise and fall times: ≤ 20ns
* Input and Output timing reference levels: 0.8V and 2.0V
* Output load : 1 TTL gate plus 100pF.

Read Cycle Timing Waveform

See page 5 for waveform

PROGRAMMING OPERATION

DC Electrical Characteristics (T_A= 25°C ±5°C, V_{CC}=5.0V±10%, V_{PP} = 12.0V ±0.4V)

Parameter		Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current		I_{IN}	V_{IH}=5.25V	-	-	8	µA
Operating Supply Current	8 BIT	I_{CCP1}		-	13	33	mA
	16 BIT	I_{CCP2}		-	22	62	mA
	32 BIT	I_{CCP3}		-	40	120	mA
V_{PP} Supply Current	8 BIT	I_{PP1}	$\overline{CS1\text{-}4}$=$\overline{PGM1\text{-}4}$=V_{IL} (6)	-	11	43	mA
	16 BIT	I_{PP2}	As I_{PP1}	-	18	82	mA
	32 BIT	I_{PP3}	As I_{PP1}	-	32	160	mA
Input Low Voltage		V_{IL}	Note (4)	-0.3	-	0.8	V
Input High Voltage		V_{IH}	Note (5)	2.2	-	V_{CC} +1	V
Output LowVoltage (Verify)		V_{OL}	I_{OL}=2.1mA	-	-	0.45	V
Output HighVoltage (Verify)		V_{OH}	I_{OH}=-400µA	2.4	-	-	V

Notes (1) V_{CC} must be applied before V_{PP} and removed after V_{PP}.
(2) V_{PP} must not exceed 13V including overshoot.
(3) Device reliability may be affected if device is installed or removed while V_{PP}= 12.5V.
(5) -1.0V for pulse width ≤ 20 ns.
(6) If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.
(7) When programming a 0.1µF high frequency by-pass capacitor is required across V_{PP} and GND to suppress noise transients

AC Characteristics (T_A= 25°C ±5°C, V_{CC}=5.0V±10%, V_{PP} = 12.0V ±0.4V)

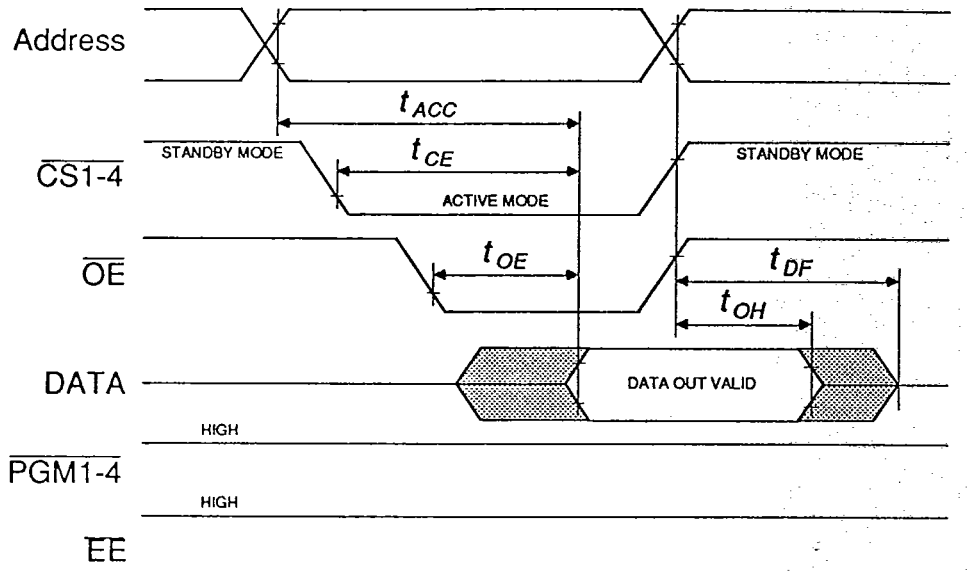
Parameter	Symbol	min	typ	max	Unit	Notes
Address Setup Time	t_{AS}	50	-	-	ns	
Chip Select Setup Time	t_{CES}	50	-	-	ns	
Data Setup Time	t_{DS}	50	-	-	ns	
Program Pulse Width	t_{PW}	TBD	200	TBD	µs	
Data Hold Time	t_{DH}	50	-	-	ns	
Address Hold Time	t_{AH}	50	-	-	ns	
Chip Select Hold Time	t_{CEH}	50	-	-	ns	
V_{PP} Setup Time	t_{VPS}	100	-	-	ns	
V_{PP} Hold Time	t_{VPH}	100	-	-	ns	
$\overline{CS1\text{-}4}$ Setup Time	t_{CER}	50	-	-	ns	1
$\overline{OE}$ Setup Time	t_{OER}	50	-	-	ns	
$\overline{PGM1\text{-}4}$ Setup Time	t_{PGR}	50	-	-	ns	1
$\overline{EE}$ Setup Time	t_{EER}	50	-	-	ns	1
$\overline{CS1\text{-}4}$ Hold Time	t_{CEF}	50	-	-	ns	1
$\overline{OE}$ Hold Time	t_{OEF}	50	-	-	ns	
$\overline{PGM1\text{-}4}$ Hold Time	t_{PGF}	50	-	-	ns	1
$\overline{EE}$ Hold Time	t_{EEF}	50	-	-	ns	1

Notes (1) $\overline{CS1\text{-}4}$, $\overline{EE}$ and $\overline{PGM1\text{-}4}$ must be fixed high during V_{PP} transition from 5V to 12V or from 12V to 5V

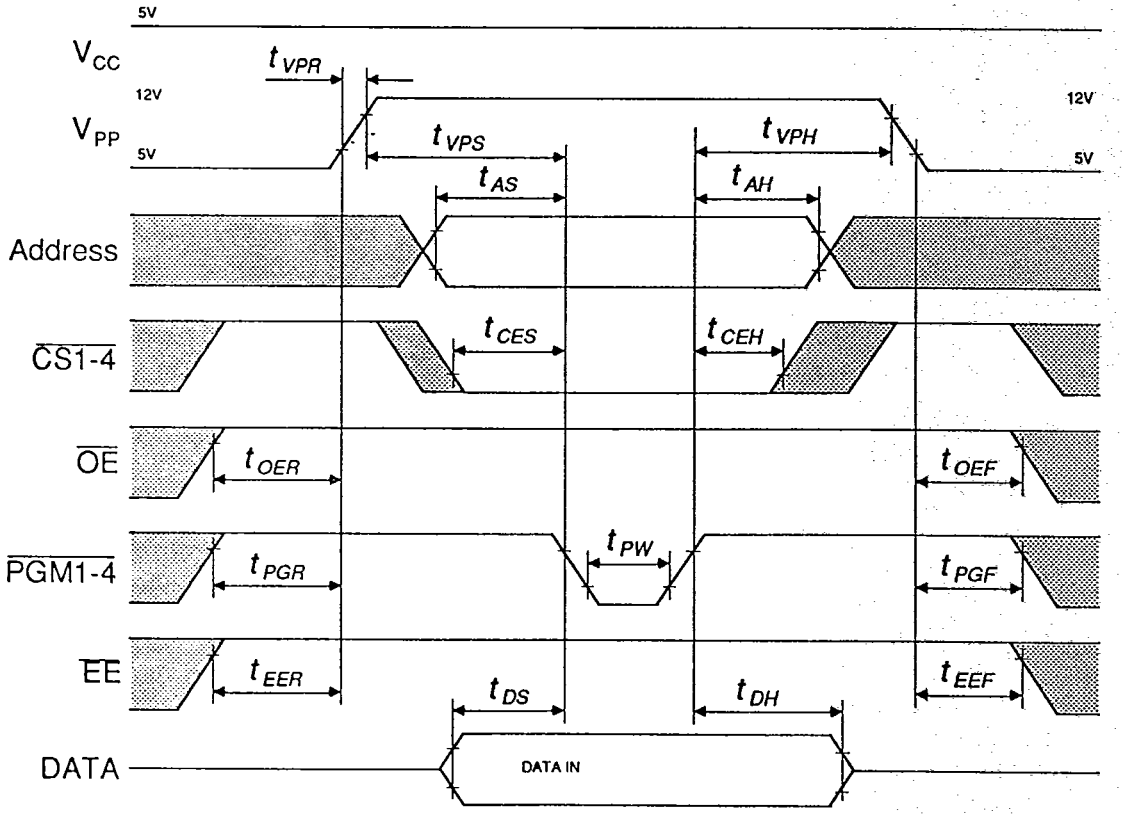
AC Test Conditions

* Input pulse levels: 0.45V to 2.4V
* Input rise and fall times: ≤ 20ns
* Input and Output timing reference levels: 0.8V and 2.0V
* Output Load : 1 TTL load + 100pF

Read Cycle Timing Waveform



Programming Cycle Timing Waveform



ERASE OPERATION

DC Electrical Characteristics (T_A= 25°C ±5°C, V_{CC}=5.0V±10%, V_{PP} = 12.0V ±0.4V)

Parameter		*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
Input Leakage Current		I_{IN1}	V_{IN}=5.25V, Address, $\overline{OE}$, $\overline{EE}$	-	-	8	µA
Input Leakage Current		I_{IN}	V_{IH}=5.25V	-	-	8	µA
Operating Supply Current	8 BIT	I_{CCE1}		-	13	33	mA
	16 BIT	I_{CCE2}		-	22	62	mA
	32 BIT	I_{CCE3}		-	40	120	mA
V_{PP} Supply Current	8 BIT	I_{EE1}	$\overline{CS1\text{-}4}$=$\overline{EE}$=V_{IL} (6)	-	33	103	mA
	16 BIT	I_{EE2}	As I_{EE1}	-	62	202	mA
	32 BIT	I_{EE3}	As I_{EE1}	-	120	400	mA
Input Low Voltage		V_{IL}	Note (4)	-0.3	-	0.8	V
Input High Voltage		V_{IH}	Note (5)	2.2	-	V_{CC} +1	V
Output LowVoltage (Verify)		V_{OL}	I_{OL}=2.1mA	-	-	0.45	V
Output HighVoltage (Verify)		V_{OH}	I_{OH}=-400µA	2.4	-	-	V

Notes (1) V_{CC} must be applied before V_{PP} and removed after V_{PP}.
(2) V_{PP} must not exceed 13V including overshoot.
(3) Device reliability may be affected if device is installed or removed while V_{PP}= 12.5V
(5) -1.0V for pulse width ≤ 20 ns.
(6) If V_{IH} is over the specified maximum value, programming operation cannot be guaranteed.
(7) When Erasing a 0.1µF high frequency by-pass capacitor is required across V_{PP} and GND to suppress noise transients

AC Characteristics (T_a= 25°C ±5°C, V_{CC}=5.0V±10%, V_{PP} = 12.0V ±0.4V)

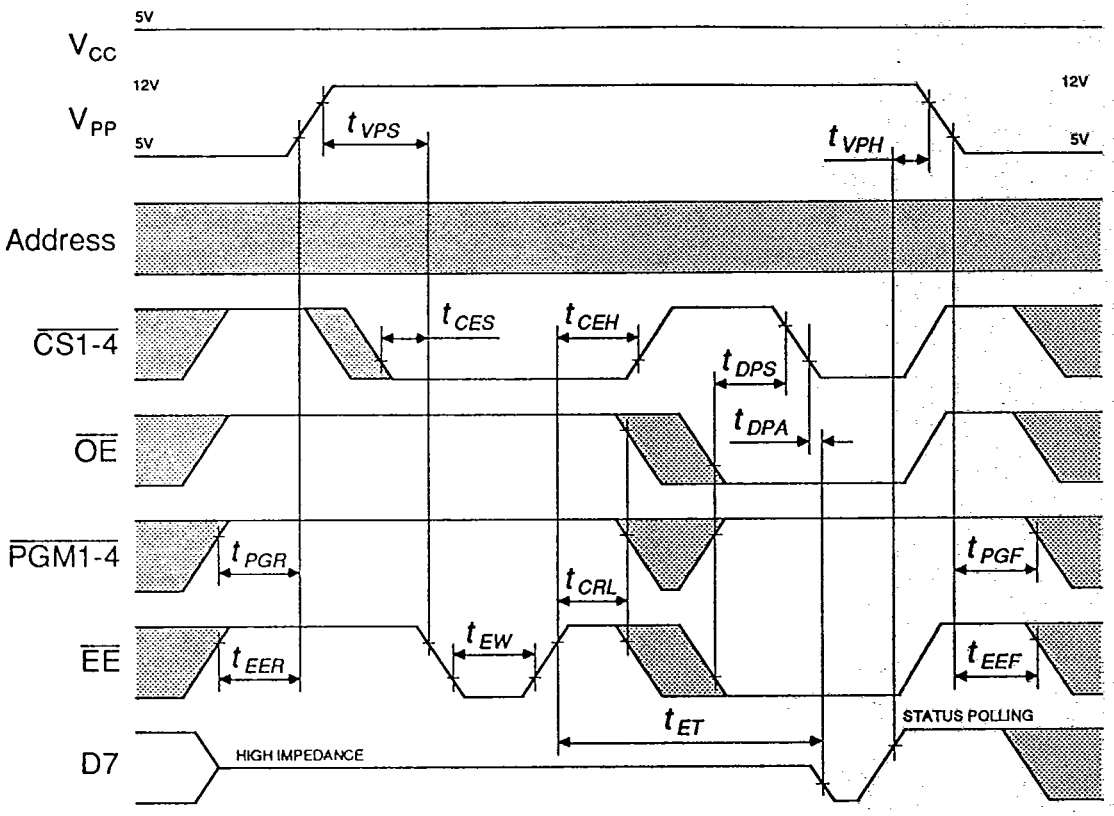
Parameter	*Symbol*	*min*	*typ*	*max*	*Unit*	*Notes*
Chip Select Setup Time	t_{CES}	50	-	-	ns	
Chip Select Hold Time	t_{CEH}	50	-	-	ns	
Erase Pulse Width	t_{EW}	100	-	-	ns	
Control Latch Time	t_{CRL}	50	-	-	ns	
Status Polling Setup Time	t_{SPS}	50	-	-	ns	
Status Polling Access Time	t_{SPA}	-	60	200	ns	
V_{PP} Setup Time	t_{VPS}	100	-	-	ns	
V_{PP} Hold Time	t_{VPH}	100	-	-	ns	
Total Erase Time	t_{ET}	0.1	2	10	s	
$\overline{CS1\text{-}4}$ Setup Time	t_{CER}	50	-	-	ns	1
$\overline{OE}$ Setup Time	t_{OER}	50	-	-	ns	
$\overline{PGM1\text{-}4}$ Setup Time	t_{PGR}	50	-	-	ns	1
$\overline{EE}$ Setup Time	t_{EER}	50	-	-	ns	1
$\overline{CS1\text{-}4}$ Hold Time	t_{CEF}	50	-	-	ns	1
$\overline{OE}$ Hold Time	t_{OEF}	50	-	-	ns	
$\overline{PGM1\text{-}4}$ Hold Time	t_{PGF}	50	-	-	ns	1
$\overline{EE}$ Hold Time	t_{EEF}	50	-	-	ns	1

Notes (1) $\overline{CS1\text{-}4}$, $\overline{EE}$ and $\overline{PGM1\text{-}4}$ must be fixed high during V_{PP} transition from 5V to 12V or from 12V to 5V

AC Test Conditions

* Input pulse levels: 0.45V to 2.4V
* Input rise and fall times: ≤ 20ns
* Input and Output timing reference levels: 0.8V and 2.0V
* Output Load : 1 TTL load + 100pF

Erase Cycle Timing Waveform



Connection Table

PGA Pin No.	Signal Name	PGA Pin No.	Signal Name	PGA Pin No.	Signal Name	PGA Pin No.	Signal Name	PGA Pin No.	Signal Name
1	D8	2	D9	3	D10	4	A14	5	A16
6	A11	7	A0	8	NC	9	D0	10	D1
11	D2	12	$\overline{PGM2}$	13	$\overline{CS2}$	14	GND	15	D11
16	A10	17	A9	18	A15	19	Vcc	20	$\overline{CS1}$
21	NC	22	D3	23	D15	24	D14	25	D13
26	D12	27	$\overline{OE}$	28	$\overline{EE}$	29	$\overline{PGM1}$	30	D7
31	D6	32	D5	33	D4	34	D24	35	D25
36	D26	37	A7	38	A12	39	Vpp	40	A13
41	A8	42	D16	43	D17	44	D18	45	Vcc
46	$\overline{CS4}$	47	$\overline{PGM4}$	48	D27	49	A4	50	A5
51	A6	52	$\overline{PGM3}$	53	$\overline{CS3}$	54	GND	55	D19
56	D31	57	D30	58	D29	59	D28	60	A1
61	A2	62	A3	63	D23	64	D22	65	D21
66	D20								

Military Screening Procedure

Module Screening Flow for high reliability product is in accordance with MIL-STD-883C method 5004 Level B and is detailed below:

MB MODULE SCREENING FLOW

SCREEN	*TEST METHOD*	*LEVEL*
Visual and Mechanical		
External visual	2017 Condition B (or manufacturers equivalent)	100%
Temperature cycle	1010 Condition C (10 Cycles,-65°C to +150°C)	100%
Burn-In		
Pre Burn-in Electrical	Per Applicable device Specifications at T_A = +25°C (optional)	100%
Burn-In	Method 1015, Codition D, T_A = +125°C	100%
Final Electrical Tests	Per applicable Device Specification	
Static (dc)	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Functional	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Switching (ac)	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Percent Defective Allowable (PDA)	Calculated at Post Burn-in at T_A=+25°C	10%
Quality Conformance	Per applicable Device Specification	Sample
External Visual	2009 Per HMP or customer specification	

Ordering Information

PUMA 2F4000MB-20

Speed	12	= 120 ns
	15	= 150 ns
	20	= 200 ns
Temp. range/screening	Blank	= Commercial Temp.
	I	= Industrial Temp.
	M	= Military Temp.
	MB	= Screened in accordance with MIL STD 883C
Memory Type	F	= FLASH EEPROM

mosaic

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