CMOS single-chip 8-bit microcontroller

80C652/83C652/87C652

T-49-19-08

DESCRIPTION

The 80C652/83C652/87C652 Single-Chip 8-Bit Microcontroller is manufactured in an advanced CMOS process and is a derivative of the 80C51 microcontroller family. The 80C652/83C652/87C652 has the same instruction set as the 80C51. Three versions of the derivative exist:

83C652 — 8k bytes mask programmable ROM

80C652 — ROMless version

87C652 — EPROM version

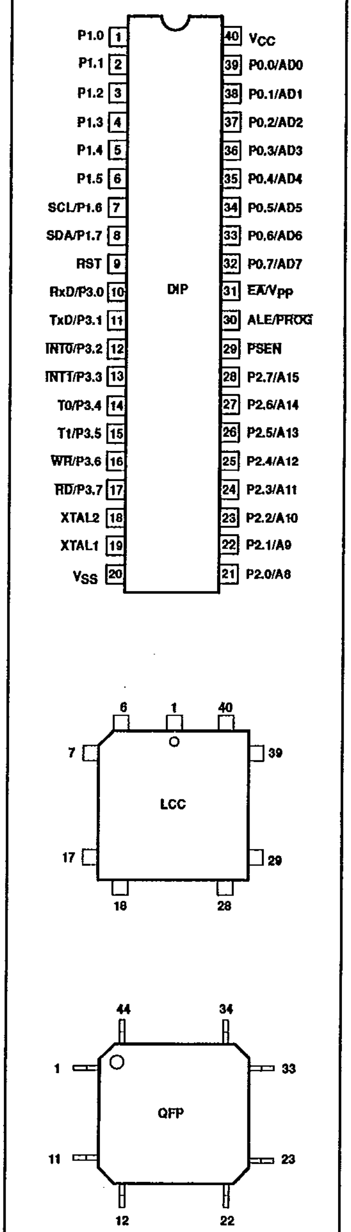
This device provides architectural enhancements that make it applicable in a variety of applications for general control systems. The 8XC652 contains a non-volatile 8k × 8 read-only program mem-ory (83C652) EPROM (87C652), a volatile 256 × 8 read/write data memory, four 8-bit I/O ports, two 16-bit timer/event counters (identical to the timers of the 80C51), a multi-source, two-priority-level, nested interrupt structure, an I²C interface, UART and on-chip oscillator and timing circuits. For systems that require extra capability, the 8XC652 can be expanded using standard TTL compatible memories and logic.

The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 45 two-byte and 17 three-byte. With a 16MHz crystal, 58% of the instructions are executed in 0.75µs and 40% in 1.5µs. Multiply and divide instructions require 3µs.

FEATURES

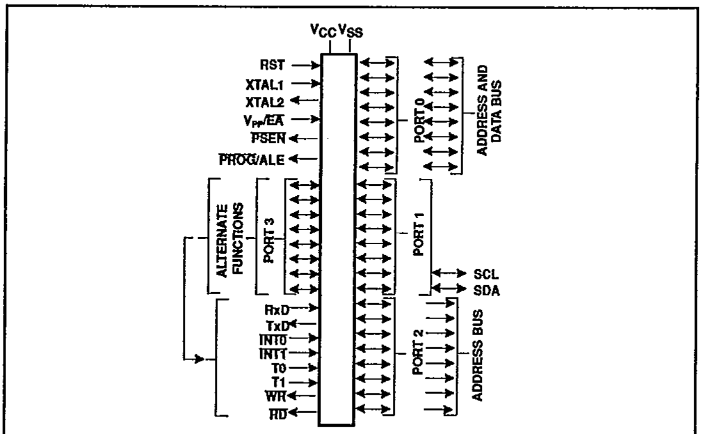
- 80C51 central processing unit
- 8k × 8 ROM expandable externally to 64k bytes (87C652 EPROM is not expandable)
- 256 × 8 RAM, expandable externally to 64k bytes
- Two standard 16-bit timer/counters
- Four 8-bit I/O ports
- I²C-bus serial I/O port with byte oriented master and slave functions
- Full-duplex UART facilities
- Power control modes
  - Idle mode
  - Power-down mode
- ROM code protection
- Five package styles
- Extended temperature ranges
- OTP package available
- Three speed ranges
  - 16MHz
  - 20MHz (87C652 only)
  - 24MHz (80C652/83C652 only)

PIN CONFIGURATION



SEE PAGE 524 FOR QFP AND LCC PIN FUNCTIONS.

LOGIC SYMBOL



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PART NUMBER SELECTION

PHILIPS PART ORDER NUMBER PART MARKING		SIGNETICS PART ORDER NUMBER			TEMPERATURE (°C)	
ROMless	ROM[4]	ROMless	ROM	EPROM	AND PACKAGE	FREQUENCY
P80C652FBP	P83C652FBP/xxx	S80C652-4N40	S83C652-4N40	S87C652-4N40	0 to +70, plastic DIP	16MHz
				S87C652-4F40	0 to +70, ceramic DIP with window	16MHz
P80C652FBA	P83C652FBA/xxx	S80C652-4A44	S83C652-4A44	S87C652-4A44	0 to +70, plastic PLCC	16MHz
				S87C652-4K44	0 to +70, ceramic CLCC with window	16MHz
P80C652FBB	P83C652FBB/xxx	S80C652-4B44	S83C652-4B44	S87C652-4B44	0 to +70, plastic QFP	16MHz
P80C652FFP	P83C652FFP/xxx	S80C652-5N40	S83C652-5N40	S87C652-5N40	–40 to +85, plastic DIP	16MHz
				S87C652-5F40	–40 to +85, ceramic DIP with window	16MHz
P80C652FFA	P83C652FFA/xxx	S80C652-5A44	S83C652-5A44	S87C652-5A44	–40 to +85, plastic PLCC	16MHz
				S87C652-5K44	–40 to +85, ceramic CLCC with window	16MHz
P80C652FFB	P83C652FFB/xxx	S80C652-5B44	S83C652-5B44	S87C652-5B44	–40 to +85, plastic QFP	16MHz
P80C652FHP	P83C652FHP/xxx	S80C652-6N40	S83C652-6N40		–40 to +125, plastic DIP	16MHz
P80C652FHA	P83C652FHA/xxx	S80C652-6A44	S83C652-6A44		–40 to +125, plastic PLCC	16MHz
P80C652FHB	P83C652FHB/xxx	S80C652-6B44	S83C652-6B44		–40 to +125, plastic QFP	16MHz
				S87C652-7N40	0 to +70, plastic DIP	20MHz
				S87C652-7F40	0 to +70, ceramic DIP with window	20MHz
				S87C652-7A44	0 to +70, plastic PLCC	20MHz
				S87C652-7K44	0 to +70, ceramic CLCC with window	20MHz
				S87C652-7B44	0 to +70, plastic QFP	20MHz
				S87C652-8N40	–40 to +85, plastic DIP	20MHz
				S87C652-8F40	–40 to +85, ceramic DIP with window	20MHz
				S87C652-8A44	–40 to +85, plastic PLCC	20MHz
				S87C652-8K44	–40 to +85, ceramic CLCC with window	20MHz
				S87C652-8B44	–40 to +85, plastic QFP	20MHz
P80C652IBP	P83C652IBP/xxx	S80C652-AN40	S83C652-AN40		0 to +70, plastic DIP	24MHz
P80C652IBA	P83C652IBA/xxx	S80C652-AA44	S83C652-AA44		0 to +70, plastic PLCC	24MHz
P80C652IBB	P83C652IBB/xxx	S80C652-AB44	S83C652-AB44		0 to +70, plastic QFP	24MHz
P80C652IFP	P83C652IFP/xxx	S80C652-BN40	S83C652-BN40		–40 to +85, plastic DIP	24MHz
P80C652IFA	P83C652IFA/xxx	S80C652-BA44	S83C652-BA44		–40 to +85, plastic PLCC	24MHz
P80C652IFB	P83C652IFB/xxx	S80C652-BB44	S83C652-BB44		–40 to +85, plastic QFP	24MHz

NOTES:
1. 80C652 and 83C652 frequency range is 1.2MHz–16MHz.
2. 87C652 frequency range is 3.5MHz–16MHz or 3.5MHz–20MHz.
3. The 87C652 EPROM is not expandable.
4. xxx denotes the ROM code number.

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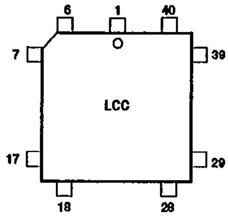
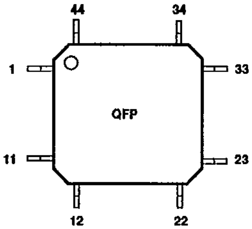
LCC PIN FUNCTIONS



Pin	Function	Pin	Function
1	NC	23	NC
2	P1.0	24	P2.0/A8
3	P1.1	25	P2.1/A9
4	P1.2	26	P2.2/A10
5	P1.3	27	P2.3/A11
6	P1.4	28	P2.4/A12
7	P1.5	29	P2.5/A13
8	P1.6/SCL	30	P2.6/A14
9	P1.7/SDA	31	P2.7/A15
10	RST	32	$\overline{PSEN}$
11	P3.0/RxD	33	ALE/$\overline{PROG}$
12	NC	34	NC
13	P3.1/TxD	35	$\overline{EA}$/V_{PP}
14	P3.2/$\overline{INT0}$	36	P0.7/AD7
15	P3.3/$\overline{INT1}$	37	P0.6/AD6
16	P3.4/T0	38	P0.5/AD5
17	P3.5/T1	39	P0.4/AD4
18	P3.6/$\overline{WR}$	40	P0.3/AD3
19	P3.7/$\overline{RD}$	41	P0.2/AD2
20	XTAL2	42	P0.1/AD1
21	XTAL1	43	P0.0/AD0
22	V_{SS}	44	V_{CC}

QFP PIN FUNCTIONS



Pin	Function	Pin	Function
1	P1.5	23	P2.5/A13
2	P1.6/SCL	24	P2.6/A14
3	P1.7/SDA	25	P2.7/A15
4	RST	26	$\overline{PSEN}$
5	P3.0/RxD	27	ALE/$\overline{PROG}$
6	NC	28	NC
7	P3.1/TxD	29	$\overline{EA}$/V_{PP}
8	P3.2/$\overline{INT0}$	30	P0.7/AD7
9	P3.3/$\overline{INT1}$	31	P0.6/AD6
10	P3.4/T0	32	P0.5/AD5
11	P3.5/T1	33	P0.4/AD4
12	P3.6/$\overline{WR}$	34	P0.3/AD3
13	P3.7/$\overline{RD}$	35	P0.2/AD2
14	XTAL2	36	P0.1/AD1
15	XTAL1	37	P0.0/AD0
16	V_{SS}	38	V_{CC}
17	NC	39	NC
18	P2.0/A8	40	P1.0
19	P2.1/A9	41	P1.1
20	P2.2/A10	42	P1.2
21	P2.3/A11	43	P1.3
22	P2.4/A12	44	P1.4

NOTES TO QFP ONLY:

1. Due to EMC improvements, it is advised to connect pins 6, 28, 39 to V_{SS} on the 80C652/83C652.

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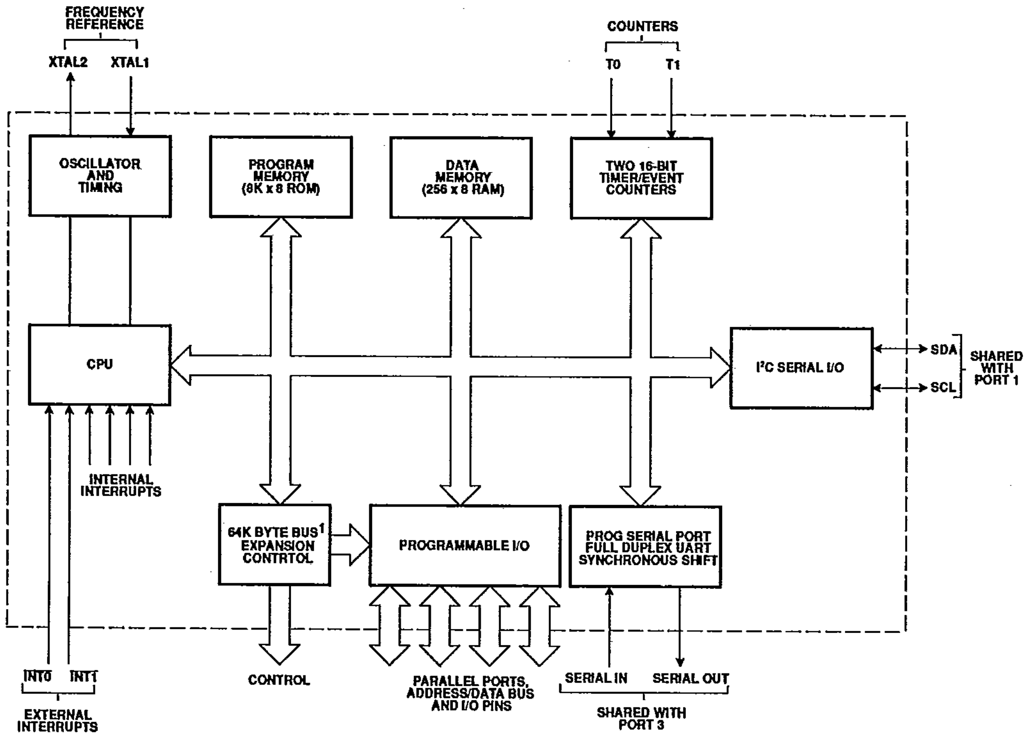
BLOCK DIAGRAM



NOTE:
1. The 87C652 EPROM is not expandable.

PIN DESCRIPTION

MNEMONIC	PIN NO. DIP	LCC	QFP	TYPE	NAME AND FUNCTION
V_{SS}	20	22	16	I	**Ground:** 0V reference.
V_{CC}	40	44	38	I	**Power Supply:** This is the power supply voltage for normal, idle, and power-down operation.
P0.0–0.7	39–32	43–36	37–30	I/O	**Port 0:** Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pull-ups when emitting 1s. Port 0 also outputs the code bytes during program verification in the 87C652. External pull-ups are required during program verification.
P1.0–P1.7	1–8	2–9	40–44, 1–3	I/O	**Port 1:** Port 1 is an 8-bit bidirectional I/O port with internal pull-ups, except P1.6 and P1.7 which are open drain. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 1 also receives the low-order address byte during program memory verification. Alternate functions include:
P1.6	7	8	2	I/O	**SCL:** I^2C-bus serial port clock line.
P1.7	8	9	3	I/O	**SDA:** I^2C-bus serial port data line.
P2.0–P2.7	21–28	24–31	18–25	I/O	**Port 2:** Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 2 pins that are externally being pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application, it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOV @Ri), port 2 emits the contents of the P2 special function register.
P3.0–P3.7	10–17	11, 13–19	5, 7–13	I/O	**Port 3:** Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally being pulled low will source current because of the pull-ups. (See DC Electrical Characteristics: I_{IL}). Port 3 also serves the special features of the 80C51 family, as listed below:
	10	11	5	I	**RxD (P3.0):** Serial input port
	11	13	7	O	**TxD (P3.1):** Serial output port
	12	14	8	I	**$\overline{INT0}$ (P3.2):** External interrupt
	13	15	9	I	**$\overline{INT1}$ (P3.3):** External interrupt
	14	16	10	I	**T0 (P3.4):** Timer 0 external input
	15	17	11	I	**T1 (P3.5):** Timer 1 external input
	16	18	12	O	**$\overline{WR}$ (P3.6):** External data memory write strobe
	17	19	13	O	**$\overline{RD}$ (P3.7):** External data memory read strobe
RST	9	10	4	I	**Reset:** A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to V_{SS} permits a power-on reset using only an external capacitor to V_{CC}.
ALE/$\overline{PROG}$	30	33	27	I/O	**Address Latch Enable/Program Pulse:** Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. This pin is also the program pulse input ($\overline{PROG}$) during EPROM programming.
$\overline{PSEN}$	29	32	26	O	**Program Store Enable:** The read strobe to external program memory. When the 87C652 is executing code from the external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory. $\overline{PSEN}$ is not activated during fetches from internal program memory.
$\overline{EA}$/V_{PP}	31	35	29	I	**External Access Enable/Programming Supply Voltage:** $\overline{EA}$ must be externally held low to enable the device to fetch code from external program memory locations 0000H and 1FFFH. If $\overline{EA}$ is held high, the device executes from internal program memory unless the program counter contains an address greater than 1FFFH. This pin also receives the 12.75V programming supply voltage (V_{PP}) during EPROM programming.
XTAL1	19	21	15	I	**Crystal 1:** Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	18	20	14	O	**Crystal 2:** Output from the inverting oscillator amplifier.

NOTE:
To avoid "latch-up" effect at power-on, the voltage on any pin at any time must not be higher than V_{CC} + 0.5V or V_{SS} – 0.5V, respectively.

ROM CODE PROTECTION (83C652)

The 83C652 has an additional security feature. ROM code protection may be selected by setting a mask programmable security bit (i.e., user dependent). This feature may be requested during ROM code submission. When selected, the ROM code is protected and cannot be read out at any time by any test mode or by any instruction in the external program memory space.

The MOVC instructions are the only instructions that have access to program code in the internal or external program memory. The $\overline{EA}$ input is latched during RESET and is "don't care" after RESET. This implementation prevents reading internal program code by switching from external program memory to internal program memory during a MOVC instruction or any other instruction that uses immediate data.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier. The pins can be configured for use as an on-chip oscillator, as shown in the logic symbol, page 522.

To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, because the input to the internal clock circuitry is through a divide-by-two flip-flop. However, minimum and maximum high and low times specified in the data sheet must be observed.

RESET

A reset is accomplished by holding the RST pin high for at least two machine cycles (24 oscillator periods), while the oscillator is running. To insure a good power-on reset, the RST pin must be high long enough to allow the oscillator time to start up (normally a few milliseconds) plus two machine cycles. At power-on, the voltage on V_{CC} and RST must come up at the same time for a proper start-up.

IDLE MODE

In the idle mode, the CPU puts itself to sleep while all of the on-chip peripherals stay active. The instruction to invoke the idle mode is the last instruction executed in the normal operating mode before the idle mode is activated. The CPU contents, the on-chip RAM, and all of the special function registers remain intact during this mode. The idle mode can be terminated either by any enabled interrupt (at which time the process is picked up at the interrupt service routine and continued), or by a hardware reset which starts the processor in the same manner as a power-on reset.

POWER-DOWN MODE

In the power-down mode, the oscillator is stopped and the instruction to invoke power-down is the last instruction executed. Only the contents of the on-chip RAM are preserved. A hardware reset is the only way to terminate the power-down mode. the control bits for the reduced power modes are in the special function register PCON. Table 1 shows the state of the I/O ports during low current operating modes.

Table 1. External Pin Status During Idle and Power-Down Mode

MODE	PROGRAM MEMORY	ALE	$\overline{PSEN}$	PORT 0	PORT 1	PORT 2	PORT 3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power-down	Internal	0	0	Data	Data	Data	Data
Power-down	External	0	0	Float	Data	Data	Data

Serial Control Register (S1CON) – See Table 2

S1CON (D8H)							
CR2	ENS1	STA	STO	SI	AA	CR1	CR0

Bits CR0, CR1 and CR2 determine the serial clock frequency that is generated in the master mode of operation.

Table 2. Serial Clock Rates

CR2	CR1	CR0	BIT FREQUENCY (kHz) AT f_{OSC}				f_{OSC} DIVIDED BY
			6MHz	12MHz	16MHz	24MHz	
0	0	0	23	47	62.5	94	256
0	0	1	27	54	71	107[1]	224
0	1	0	31.25	62.5	83.3	125[1]	192
0	1	1	37	75	100	150[1]	160
1	0	0	6.25	12.5	17	25	960
1	0	1	50	100	133[1]	200[1]	120
1	1	0	100	200[1]	267[1]	400[1]	60
1	1	1	> 0.25 < 62.5	> 0.5 < 62.5	> 0.67 < 56	> 0.98 < 50	96 × (256 – (reload value Timer 1)) (Reload value range: 0 – 254 in mode 2)

NOTES:
1. These frequencies exceed the upper limit of 100kHz of the I²C-bus specification and cannot be used in an I²C-bus application.

ABSOLUTE MAXIMUM RATINGS[1, 2, 3]

PARAMETER	RATING	UNIT
Storage temperature range	–65 to +150	°C
Voltage on $\overline{EA}/V_{PP}$ to V_{SS} (87C652 only)	–0.5 to + 13	V
Voltage on any other pin to V_{SS}	–0.5 to + 6.5	V
Input, output current on any single pin	±5	mA
Input, output current on any two pins	±10	mA
Power dissipation (based on package heat transfer limitations, not device power consumption)	1	W

NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the AC and DC Electrical Characteristics section of this specification is not implied.
2. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.
3. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

DEVICE SPECIFICATIONS

TYPE	SUPPLY VOLTAGE (V)		FREQUENCY (MHz)		TEMPERATURE (°C)
	MIN.	MAX.	MIN.	MAX.	
P83(0)C652FB	4.0	6.0	1.2	16	0 to +70
S87C652–4	4.5	5.5	3.5	16	0 to +70
P83(0)C652FF	4.0	6.0	1.2	16	–40 to +85
S87C652–5	4.5	5.5	3.5	16	–40 to +85
P83(0)C652FH	4.5	5.5	1.2	16	–40 to +125
S87C652–7	4.5	5.5	3.5	20	0 to +70
S87C652–8	4.5	5.5	3.5	20	–40 to +85
P83(0)C652IB	4.5	5.5	1.2	24	0 to +70
P83(0)C652IF	4.5	5.5	1.2	24	–40 to +85

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DC ELECTRICAL CHARACTERISTICS

V_{SS} = 0V

SYMBOL	PARAMETER	PART TYPE	TEST CONDITIONS	LIMITS MIN.	LIMITS MAX.	UNIT
V_{IL}	Input low voltage, except $\overline{EA}$, P1.6/SCL, P1.7/SDA	0°C to +70°C –40°C to +85°C –40°C to +125°C		–0.5 –0.5 –0.5	$0.2V_{CC}$ – 0.1 $0.2V_{CC}$ – 0.15 $0.2V_{CC}$ – 0.25	V V V
V_{IL1}	Input low voltage to $\overline{EA}$	0°C to +70°C –40°C to +85°C –40°C to +125°C		–0.5 –0.5 –0.5	$0.2V_{CC}$ – 0.3 $0.2V_{CC}$ – 0.35 $0.2V_{CC}$ – 0.45	V V V
V_{IL2}	Input low voltage to P1.6/SCL, P1.7/SDA[6]			–0.5	1.5	V
V_{IH}	Input high voltage, except XTAL1, RST, P1.6/SCL, P1.7/SDA	0°C to +70°C –40°C to +85°C –40°C to +125°C		$0.2V_{CC}$ + 0.9 $0.2V_{CC}$ + 1.0 $0.2V_{CC}$ + 1.0	V_{CC} + 0.5 V_{CC} + 0.5 V_{CC} + 0.5	V V V
V_{IH1}	Input high voltage, XTAL1, RST	0°C to +70°C –40°C to +85°C –40°C to +125°C		$0.7V_{CC}$ $0.7V_{CC}$ + 0.1 $0.7V_{CC}$ + 0.1	V_{CC} + 0.5 V_{CC} + 0.5 V_{CC} + 0.5	V V V
V_{IH2}	Input high voltage, P1.6/SCL, P1.7/SDA[6]			3.0	6.0	V
V_{OL}	Output low voltage, ports 1, 2, 3, except P1.6/SCL, P1.7/SDA		I_{OL} = 1.6mA[8]		0.45	V
V_{OL1}	Output low voltage, port 0, ALE, $\overline{PSEN}$		I_{OL} = 3.2mA[8]		0.45	V
V_{OL2}	Output low voltage, P1.6/SCL, P1.7/SDA		I_{OL} = 3.0mA		0.4	V
V_{OH}	Output high voltage, ports 1, 2, 3		I_{OH} = –60μA I_{OH} = –25μA I_{OH} = –10μA	2.4 $0.75V_{CC}$ $0.9V_{CC}$		V V V
V_{OH1}	Output high voltage, Port 0 in external bus mode, ALE, $\overline{PSEN}$, RST[9]		I_{OH} = –400μA I_{OH} = –150μA I_{OH} = –40μA	2.4 $0.75V_{CC}$ $0.9V_{CC}$		V V V
I_{IL}	Logical 0 input current, ports 1, 2, 3, except P1.6/SCL, P1.7/SDA	0°C to +70°C –40°C to +85°C –40°C to +125°C	V_{IN} = 0.45V		–50 –75 –75	μA μA μA
I_{TL}	Logical 1-to-0 transition current, ports 1, 2, 3, except P1.6/SCL, P1.7/SDA	0°C to +70°C –40°C to +85°C –40°C to +125°C	See Note 7		–650 –750 –750	μA μA μA
I_{L1}	Input leakage current, port 0		0.45 < V_I < V_{CC}		±10	μA
I_{L2}	Input leakage current, P1.6/SCL, P1.7/SDA		0V < V_I < 6.0V 0V < V_{CC} < 6.0V		±10	μA μA
I_{CC}	Power supply current: Active mode @ 16MHz (80/83C652)[2,10] Active mode @ 16MHz (87C652)[2] Idle mode @ 16MHz (80/83C652)[3,10] Idle mode @ 16MHz (87C652)[3] Power down mode[4,5] Power down mode[4,5]	 –40°C to +125°C	See Note 1 V_{CC} = 6.0V		 26.5 25 6 6 50 100	 mA mA mA mA μA μA
R_{RST}	Internal reset pull-down resistor			50	150	kΩ
C_{IO}	Pin Capacitance		Freq. = 1MHz		10	pF

NOTES: See next page.

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NOTES FOR DC ELECTRICAL CHARACTERISTICS:

1. See Figures 10 through 13 for I_{CC} test conditions.
2. The operating supply current is measured with all output pins disconnected; XTAL1 driven with $t_r = t_f = 10ns$; $V_{IL} = V_{SS} + 0.5V$; $V_{IH} = V_{CC} - 0.5V$; XTAL2 not connected; $\overline{EA}$ = RST = Port 0 = P1.6 = P1.7 = V_{CC}; f_{CLK} = 16MHz. See Figure 10.
3. The idle mode supply current is measured with all output pins disconnected; XTAL1 driven with $t_r = t_f = 10ns$; $V_{IL} = V_{SS} + 0.5V$; $V_{IH} = V_{CC} - 0.5V$; XTAL2 not connected; Port 0 = P1.6 = P1.7 = V_{CC}; $\overline{EA}$ = RST = V_{SS}; f_{CLK} = 16MHz. See Figure 11.
4. The power-down current is measured with all output pins disconnected; XTAL2 not connected; Port 0 = P1.6 = P1.7 = V_{CC}; $\overline{EA}$ = RST = V_{SS}. See Figure 13.
5. $2V \leq V_{PD} \leq V_{CC}max$.
6. The input threshold voltage of P1.6 and P1.7 (SIO1) meets the I²C specification, so an input voltage below 1.5V will be recognized as a logic 0 while an input voltage above 3.0V will be recognized as a logic 1.
7. Pins of ports 1, 2, and 3 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2V.
8. Capacitive loading on ports 0 and 2 may cause spurious noise to be superimposed on the V_{OL}s of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100pF), the noise pulse on the ALE pin may exceed 0.8V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input. I_{OL} can exceed these conditions provided that no single output sinks more than 5mA and no more than two outputs exceed the test conditions.
9. Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the $0.9V_{CC}$ specification when the address bits are stabilizing.
10. I_{CCMAX} for the 80/83C652 at other frequencies can be derived from Figure 1, where FREQ is the external oscillator frequency in MHz. I_{CCMAX} is given in mA.

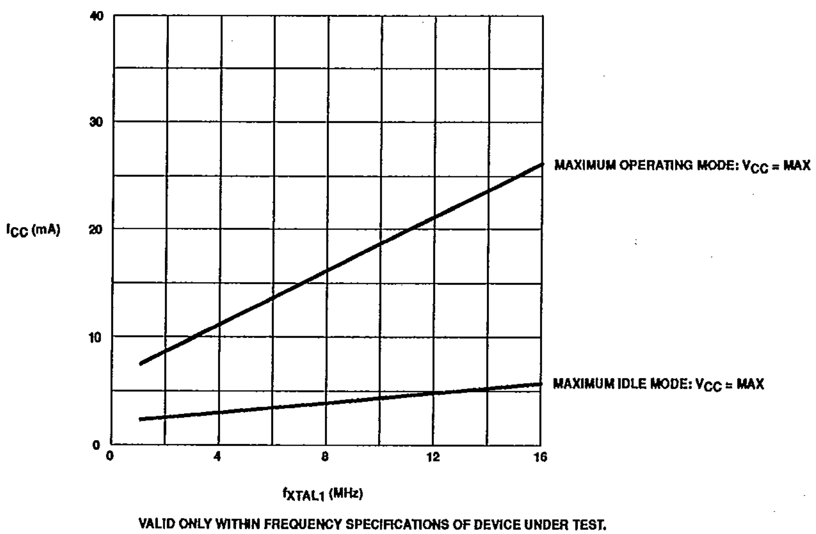

Figure 1. I_{CC} vs. Frequency

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AC ELECTRICAL CHARACTERISTICS

T_{amb} = 0°C to +70°C, or T_{amb} = –40°C to +85°C/+125°C, V_{SS} = 0V[1,2]

SYMBOL	FIGURE	PARAMETER	16MHz CLOCK MIN	16MHz CLOCK MAX	VARIABLE CLOCK MIN	VARIABLE CLOCK MAX	UNIT
$1/t_{CLCL}$	2	Oscillator frequency			1.2 (3.5)	16	MHz
t_{LHLL}	2	ALE pulse width	85		$2t_{CLCL}$–40		ns
t_{AVLL}	2	Address valid to ALE low	8		t_{CLCL}–55		ns
t_{LLAX}	2	Address hold after ALE low	28		t_{CLCL}–35		ns
t_{LLIV}	2	ALE low to valid instruction in		150		$4t_{CLCL}$–100	ns
t_{LLPL}	2	ALE low to $\overline{PSEN}$ low	23		t_{CLCL}–40		ns
t_{PLPH}	2	$\overline{PSEN}$ pulse width	143		$3t_{CLCL}$–45		ns
t_{PLIV}	2	$\overline{PSEN}$ low to valid instruction in		83		$3t_{CLCL}$–105	ns
t_{PXIX}	2	Input instruction hold after $\overline{PSEN}$	0		0		ns
t_{PXIZ}	2	Input instruction float after $\overline{PSEN}$		38		t_{CLCL}–25	ns
t_{AVIV}	2	Address to valid instruction in		208		$5t_{CLCL}$–105	ns
t_{PLAZ}	2	$\overline{PSEN}$ low to address float		10		10	ns
Data Memory							
t_{AVLL}	3, 4	Address valid to ALE low	28		t_{CLCL}–35		ns
t_{RLRH}	3, 4	$\overline{RD}$ pulse width	275		$6t_{CLCL}$–100		ns
t_{WLWH}	3, 4	$\overline{WR}$ pulse width	275		$6t_{CLCL}$–100		ns
t_{RLDV}	3, 4	$\overline{RD}$ low to valid data in		148		$5t_{CLCL}$–165	ns
t_{RHDX}	3, 4	Data hold after $\overline{RD}$	0		0		ns
t_{RHDZ}	3, 4	Data float after $\overline{RD}$		55		$2t_{CLCL}$–70	ns
t_{LLDV}	3, 4	ALE low to valid data in		350		$8t_{CLCL}$–150	ns
t_{AVDV}	3, 4	Address to valid data in		398		$9t_{CLCL}$–165	ns
t_{LLWL}	3, 4	ALE low to $\overline{RD}$ or $\overline{WR}$ low	138	238	$3t_{CLCL}$–50	$3t_{CLCL}$+50	ns
t_{AVWL}	3, 4	Address valid to $\overline{WR}$ low or $\overline{RD}$ low	120		$4t_{CLCL}$–130		ns
t_{QVWX}	3, 4	Data valid to $\overline{WR}$ transition	3		t_{CLCL}–60		ns
t_{QW}	3, 4	Data setup time before $\overline{WR}$	288		$7t_{CLCL}$–150		ns
t_{WHQX}	3, 4	Data hold after $\overline{WR}$	13		t_{CLCL}–50		ns
t_{RLAZ}	3, 4	$\overline{RD}$ low to address float		0		0	ns
t_{WHLH}	3, 4	$\overline{RD}$ or $\overline{WR}$ high to ALE high	23	103	t_{CLCL}–40	t_{CLCL}+40	ns
Shift Register[3]							
t_{XLXL}	5	Serial port clock cycle time[4]	0.75		$12t_{CLCL}$		µs
t_{QVXH}	5	Output data setup to clock rising edge[4]	492		$10t_{CLCL}$–133		ns
t_{XHQX}	5	Output data hold after clock rising edge[4]	8		$2t_{CLCL}$–117		ns
t_{XHDX}	5	Input data hold after clock rising edge[4]	0		0		ns
t_{XHDV}	5	Clock rising edge to input data valid[4]		498		$10t_{CLCL}$–133	ns
External Clock							
t_{CHCX}	6	High time[4]	20		20	$t_{CLCL}-t_{LOW}$	ns
t_{CLCX}	6	Low time[4]	20		20	$t_{CLCL}-t_{HIGH}$	ns
t_{CLCH}	6	Rise time[4]		20		20	ns
t_{CHCL}	6	Fall time[4]		20		20	ns

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AC ELECTRICAL CHARACTERISTICS (Continued)

T_{amb} = 0°C to +70°C, or T_{amb} = –40°C to +85°C/+125°C, V_{SS} = 0V[1,2]

SYMBOL	FIGURE	PARAMETER	24MHz CLOCK		VARIABLE CLOCK		UNIT
			MIN	MAX	MIN	MAX	
$1/t_{CLCL}$	2	Oscillator frequency			1.2 (3.5)	24 (20)	MHz
t_{LHLL}	2	ALE pulse width	43		$2t_{CLCL}$–40		ns
t_{AVLL}	2	Address valid to ALE low	17		t_{CLCL}–25		ns
t_{LLAX}	2	Address hold after ALE low	17		t_{CLCL}–25		ns
t_{LLIV}	2	ALE low to valid instruction in		102		$4t_{CLCL}$–65	ns
t_{LLPL}	2	ALE low to $\overline{PSEN}$ low	17		t_{CLCL}–25		ns
t_{PLPH}	2	$\overline{PSEN}$ pulse width	80		$3t_{CLCL}$–45		ns
t_{PLIV}	2	$\overline{PSEN}$ low to valid instruction in		65		$3t_{CLCL}$–60	ns
t_{PXIX}	2	Input instruction hold after $\overline{PSEN}$	0		0		ns
t_{PXIZ}	2	Input instruction float after $\overline{PSEN}$		17		t_{CLCL}–25	ns
t_{AVIV}	2	Address to valid instruction in		128		$5t_{CLCL}$–80	ns
t_{PLAZ}	2	$\overline{PSEN}$ low to address float		10		10	ns
Data Memory							
t_{AVLL}	3, 4	Address valid to ALE low	17		t_{CLCL}–25		ns
t_{RLRH}	3, 4	$\overline{RD}$ pulse width	150		$6t_{CLCL}$–100		ns
t_{WLWH}	3, 4	$\overline{WR}$ pulse width	150		$6t_{CLCL}$–100		ns
t_{RLDV}	3, 4	$\overline{RD}$ low to valid data in		118		$5t_{CLCL}$–90	ns
t_{RHDX}	3, 4	Data hold after $\overline{RD}$	0		0		ns
t_{RHDZ}	3, 4	Data float after $\overline{RD}$		55		$2t_{CLCL}$–28	ns
t_{LLDV}	3, 4	ALE low to valid data in		183		$8t_{CLCL}$–150	ns
t_{AVDV}	3, 4	Address to valid data in		210		$9t_{CLCL}$–165	ns
t_{LLWL}	3, 4	ALE low to $\overline{RD}$ or $\overline{WR}$ low	75	175	$3t_{CLCL}$–50	$3t_{CLCL}$+50	ns
t_{AVWL}	3, 4	Address valid to $\overline{WR}$ low or $\overline{RD}$ low	92		$4t_{CLCL}$–75		ns
t_{QVWX}	3, 4	Data valid to $\overline{WR}$ transition	12		t_{CLCL}–30		ns
t_{DW}	3, 4	Data setup time before $\overline{WR}$	162		$7t_{CLCL}$–130		ns
t_{WHQX}	3, 4	Data hold after $\overline{WR}$	17		t_{CLCL}–25		ns
t_{RLAZ}	3, 4	$\overline{RD}$ low to address float		0		0	ns
t_{WHLH}	3, 4	$\overline{RD}$ or $\overline{WR}$ high to ALE high	17	67	t_{CLCL}–25	t_{CLCL}+25	ns
Shift Register[3]							
t_{XLXL}	5	Serial port clock cycle time[4]	0.5		$12t_{CLCL}$		μs
t_{QVXH}	5	Output data setup to clock rising edge[4]	283		$10t_{CLCL}$–133		ns
t_{XHQX}	5	Output data hold after clock rising edge[4]	23		$2t_{CLCL}$–60		ns
t_{XHDX}	5	Input data hold after clock rising edge[4]	0		0		ns
t_{XHDV}	5	Clock rising edge to input data valid[4]		283		$10t_{CLCL}$–133	ns
External Clock							
t_{CHCX}	6	High time[4]	17		17	$t_{CLCL}-t_{LOW}$	ns
t_{CLCX}	6	Low time[4]	17		17	$t_{CLCL}-t_{HIGH}$	ns
t_{CLCH}	6	Rise time[4]		20		20	ns
t_{CHCL}	6	Fall time[4]		20		20	ns

AC ELECTRICAL CHARACTERISTICS (Continued)

T_{amb} = 0°C to +70°C, or T_{amb} = –40°C to +85°C/+125°C, V_{SS} = 0V[1,2]

SYMBOL	PARAMETER	INPUT	OUTPUT
I²C Interface			
t_{HD}; STA	START condition hold time	≥ 14 t_{CLCL}	> 4.0µs [5]
t_{LOW}	SCL low time	≥ 16 t_{CLCL}	> 4.7µs [5]
t_{HIGH}	SCL high time	≥ 14 t_{CLCL}	> 4.0µs [5]
t_{RC}	SCL rise time	≤ 1µs	– [6]
t_{FC}	SCL fall time	≤ 0.3µs	< 0.3µs [7]
t_{SU}; DAT1	Data set-up time	≥ 250ns	> 20 t_{CLCL} – t_{RD}
t_{SU}; DAT2	SDA set-up time (before rep. START cond.)	≥ 250ns	> 1µs [5]
t_{SU}; DAT3	SDA set-up time (before STOP cond.)	≥ 250ns	> 8 t_{CLCL}
t_{HD}; DAT	Data hold time	≥ 0ns	> 8 t_{CLCL} – t_{FC}
t_{SU}; STA	Repeated START set-up time	≥ 14 t_{CLCL} [5]	> 4.7µs [5]
t_{SU}; STO	STOP condition set-up time	≥ 14 t_{CLCL} [5]	> 4.0µs [5]
t_{BUF}	Bus free time	≥ 14 t_{CLCL} [5]	> 4.7µs [5]
t_{RD}	SDA rise time	≤ 1µs [8]	– [6]
t_{FD}	SDA fall time	≤ 300ns [8]	< 0.3µs [7]

NOTES:

1. Parameters are valid over operating temperature range and voltage range unless otherwise specified.
2. Load capacitance for port 0, ALE, and $\overline{PSEN}$ = 100pF, load capacitance for all other outputs = 80pF.
3. The shift register has been characterized for the 87C652 only.
4. These values are characterized but not 100% production tested.
5. At 100 kbit/s. At other bit rates this value is inversely proportional to the bit-rate of 100 kbit/s.
6. Determined by the external bus-line capacitance and the external bus-line pull-resistor, this must be < 1µs.
7. Spikes on the SDA and SCL lines with a duration of less than 3 t_{CLCL} will be filtered out. Maximum capacitance on bus-lines SDA and SCL = 400pF.
8. $t_{CLCL} = 1/f_{OSC}$ = one oscillator clock period at pin XTAL1. For 63ns < t_{CLCL} < 285ns (16MHz > f_{OSC} > 3.5MHz) the I²C interface meets the I²C-bus specification for bit-rates up to 100 kbit/s.

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EXPLANATION OF THE AC SYMBOLS

Each timing symbol has five characters. The first character is always 't' (= time). The other characters, depending on their positions, indicate the name of a signal or the logical status of that signal. The designations are:

- A – Address
- C – Clock
- D – Input data
- H – Logic level high
- I – Instruction (program memory contents)
- L – Logic level low, or ALE
- P – $\overline{\text{PSEN}}$
- Q – Output data
- R – $\overline{\text{RD}}$ signal
- t – Time
- V – Valid
- W – $\overline{\text{WR}}$ signal
- X – No longer a valid logic level
- Z – Float

Examples: t_{AVLL} = Time for address valid to ALE low.

t_{LLPL} = Time for ALE low to $\overline{\text{PSEN}}$ low.

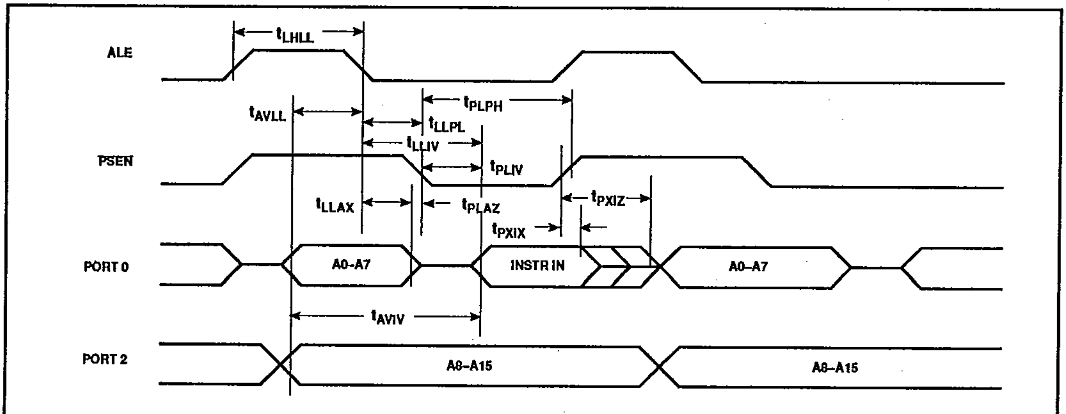

Figure 2. External Program Memory Read Cycle

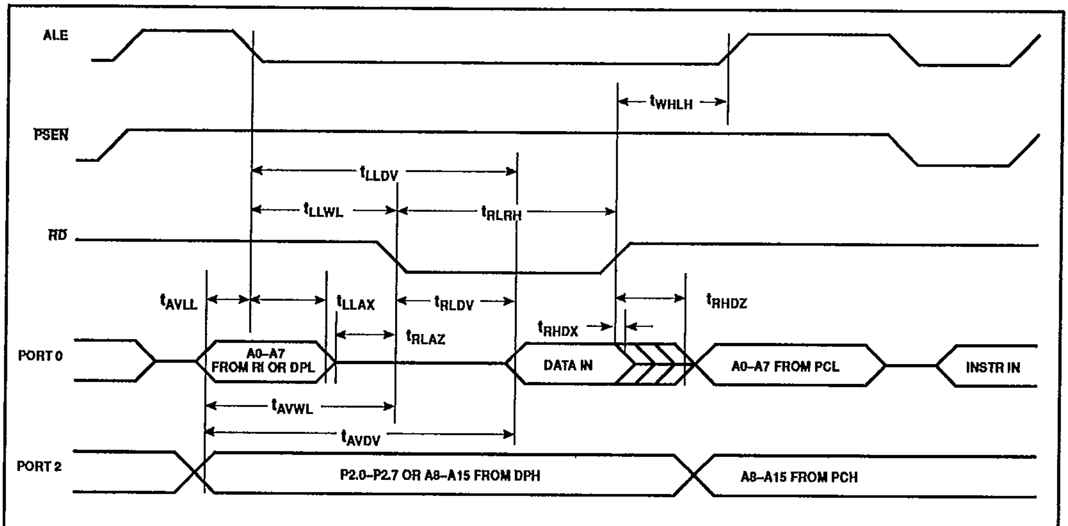

Figure 3. External Data Memory Read Cycle

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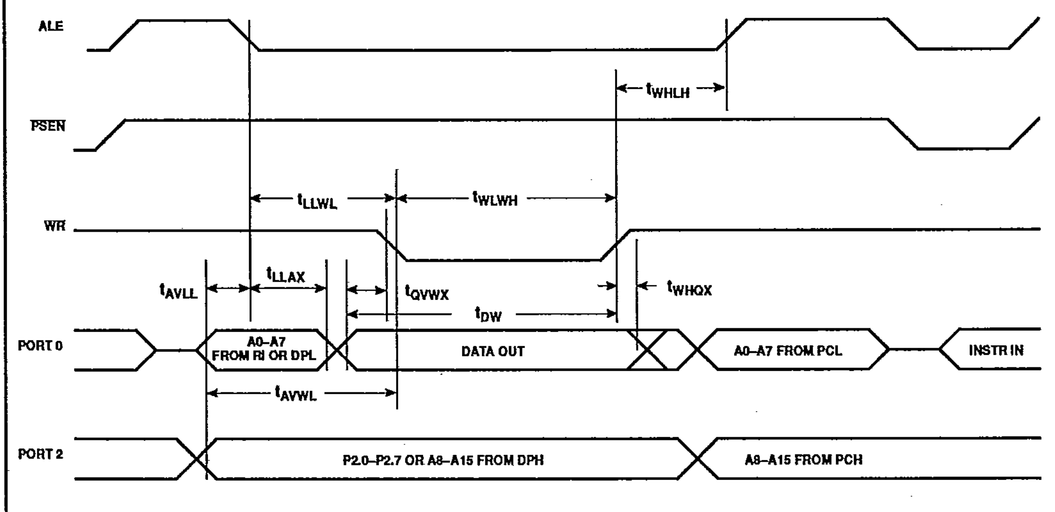

Figure 4. External Data Memory Write Cycle

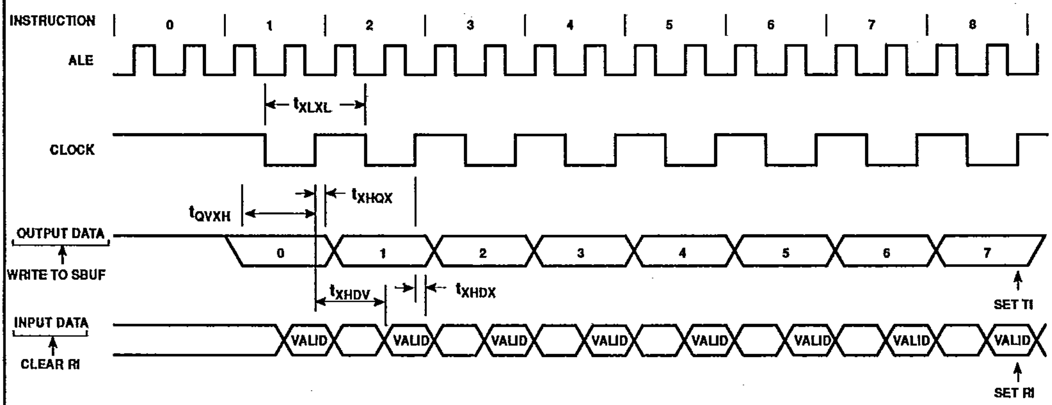

Figure 5. Shift Register Mode Timing

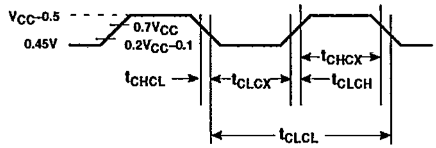

Figure 6. External Clock Drive

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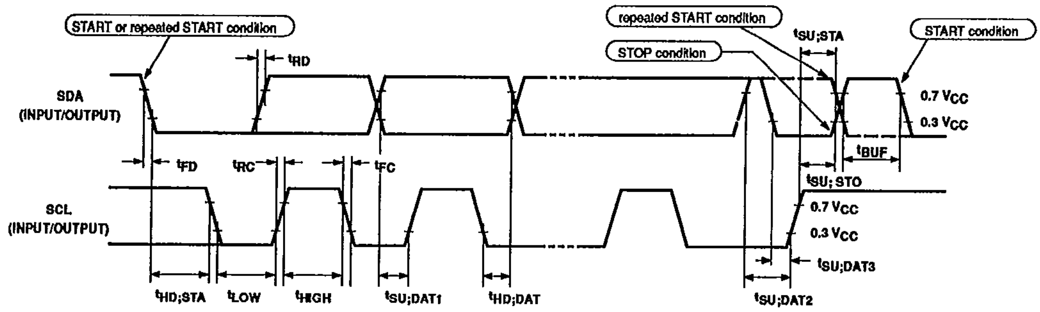
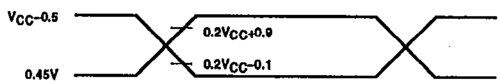


Figure 7. Timing SIO1 (I^2C) Interface



NOTE:
AC INPUTS DURING TESTING ARE DRIVEN AT V_{CC}–0.5 FOR A LOGIC '1' AND 0.45V FOR A LOGIC '0'. TIMING MEASUREMENTS ARE MADE AT V_{IH} MIN FOR A LOGIC '1' AND V_{IL} MAX FOR A LOGIC '0'.

Figure 8. AC Testing Input/Output

NOTE:
FOR TIMING PURPOSES, A PORT IS NO LONGER FLOATING WHEN A 100MV CHANGE FROM LOAD VOLTAGE OCCURS, AND BEGINS TO FLOAT WHEN A 100mV CHANGE FROM THE LOADED V_{OH}/V_{OL} LEVEL OCCURS. $I_{OH}/I_{OL} \geq \pm 20mA$.

Figure 9. Float Waveform

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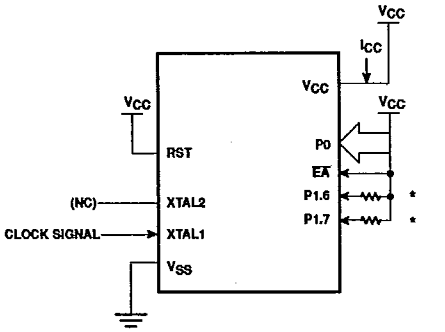

Figure 10. I_{CC} Test Condition, Active Mode
All other pins are disconnected

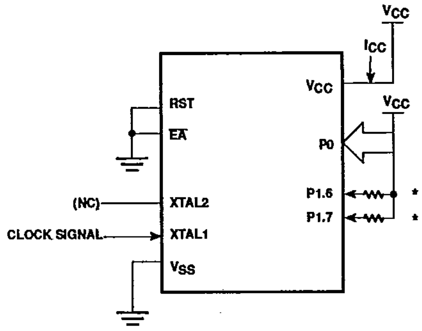

Figure 11. I_{CC} Test Condition, Idle Mode
All other pins are disconnected

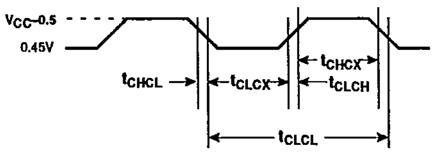

Figure 12. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes
$t_{CLCL} = t_{CHCL} = 10ns$

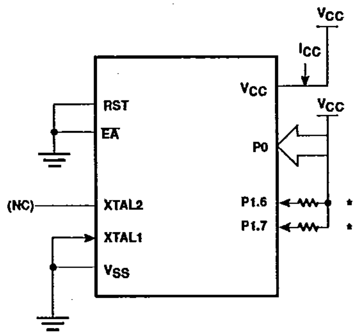

Figure 13. I_{CC} Test Condition, Power Down Mode
All other pins are disconnected
V_{CC} = 2V to 5.5V

NOTE:
* Ports 1.6 and 1.7 should be connected to V_{CC} through resistors of sufficiently high value such that the sink current into these pins does not exceed the I_{OL1} specification.

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EPROM CHARACTERISTICS

The 87C652 is programmed by using a modified Quick-Pulse Programming™ algorithm. It differs from older methods in the value used for V_{PP} (programming supply voltage) and in the width and number of the ALE/PROG pulses.

The 87C652 contains two signature bytes that can be read and used by an EPROM programming system to identify the device. The signature bytes identify the device as an 87C652 manufactured by Philips Components.

Table 3 shows the logic levels for reading the signature byte, and for programming the program memory, the encryption table, and the lock bits. The circuit configuration and waveforms for quick-pulse programming are shown in Figures 14 and 15. Figure 16 shows the circuit configuration for normal program memory verification.

Quick-Pulse Programming

The setup for microcontroller quick-pulse programming is shown in Figure 14. Note that the 87C652 is running with a 4 to 6MHz oscillator. The reason the oscillator needs to be running is that the device is executing internal address and program data transfers.

The address of the EPROM location to be programmed is applied to ports 1 and 2, as shown in Figure 14. The code byte to be programmed into that location is applied to port 0. RST, PSEN and pins of ports 2 and 3 specified in Table 3 are held at the 'Program Code Data' levels indicated in Table 3. The ALE/PROG is pulsed low 25 times as shown in Figure 15.

To program the encryption table, repeat the 25 pulse programming sequence for addresses 0 through 1FH, using the 'Pgm Encryption Table' levels. Do not forget that after the encryption table is programmed, verification cycles will produce only encrypted data.

To program the lock bits, repeat the 25 pulse programming sequence using the 'Pgm Lock Bit' levels. After one lock bit is programmed, further programming of the code memory and encryption table is disabled. However, the other lock bit can still be programmed.

Note that the EA/V_{PP} pin must not be allowed to go above the maximum specified V_{PP} level for any amount of time. Even a narrow glitch above that voltage can cause permanent damage to the device. The V_{PP} source should be well regulated and free of glitches and overshoot.

Program Verification

If lock bit 2 has not been programmed, the on-chip program memory can be read out for program verification. The address of the program memory locations to be read is applied to ports 1 and 2 as shown in Figure 16. The other pins are held at the 'Verify Code Data' levels indicated in Table 3. The contents of the address location will be emitted on port 0. External pull-ups are required on port 0 for this operation.

If the encryption table has been programmed, the data presented at port 0 will be the exclusive NOR of the program byte with one of the encryption bytes. The user will have to know the encryption table contents in order to correctly decode the verification data. The encryption table itself cannot be read out.

Reading the Signature Bytes

The signature bytes are read by the same procedure as a normal verification of locations 030H and 031H, except that P3.6 and P3.7 need to be pulled to a logic low. The values are:

(030H) = 5H indicates manufactured by Philips
(031H) = 99H indicates 87C652

Program/Verify Algorithms

Any algorithm in agreement with the conditions listed in Table 3, and which satisfies the timing specifications, is suitable.

Erasure Characteristics

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelengths shorter than approximately 4,000 angstroms. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room level fluorescent lighting) could cause inadvertent erasure. **For this and secondary effects, it is recommended that an opaque label be placed over the window.** For elevated temperature or environments where solvents are being used, apply Kapton tape Fluorglas part number 2345–5, or equivalent.

The recommended erasure procedure is exposure to ultraviolet light (at 2537 angstroms) to an integrated dose of at least 15W-sec/cm^2. Exposing the EPROM to an ultraviolet lamp of 12,000uW/cm^2 rating for 20 to 39 minutes, at a distance of about 1 inch, should be sufficient. Erasure leaves the array in an all 1s state.

Table 3. EPROM Programming Modes

MODE	RST	PSEN	ALE/PROG	EA/V_{PP}	P2.7	P2.6	P3.7	P3.6
Read signature	1	0	1	1	0	0	0	0
Program code data	1	0	0*	V_{PP}	1	0	1	1
Verify code data	1	0	1	1	0	0	1	1
Pgm encryption table	1	0	0*	V_{PP}	1	0	1	0
Pgm lock bit 1	1	0	0*	V_{PP}	1	1	1	1
Pgm lock bit 2	1	0	0*	V_{PP}	1	1	0	0

NOTES:
1. '0' = Valid low for that pin, '1' = valid high for that pin.
2. V_{PP} = 12.75V ±0.25V.
3. V_{CC} = 5V±10% during programming and verification.
* ALE/PROG receives 25 programming pulses while V_{PP} is held at 12.75V. Each programming pulse is low for 100μs (±10μs) and high for a minimum of 10μs.

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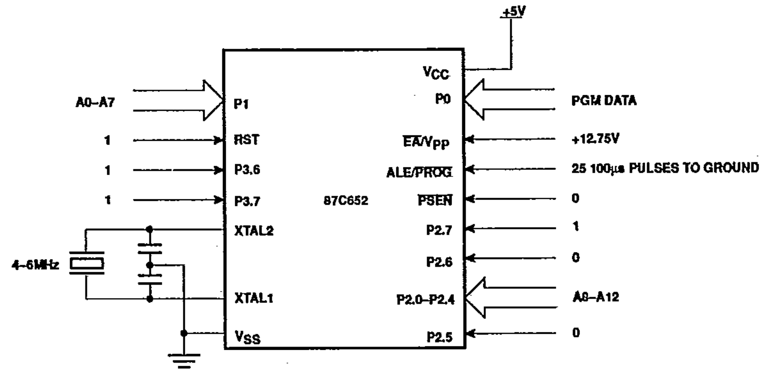

Figure 14. Programming Configuration

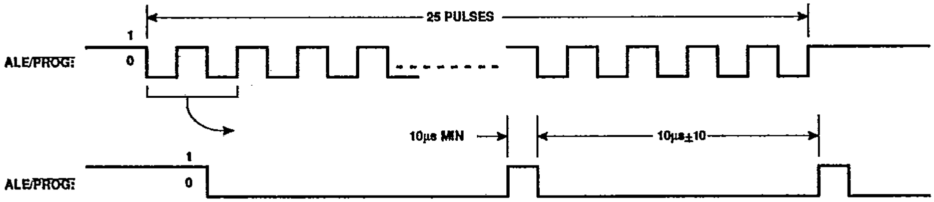

Figure 15. PROG Waveform

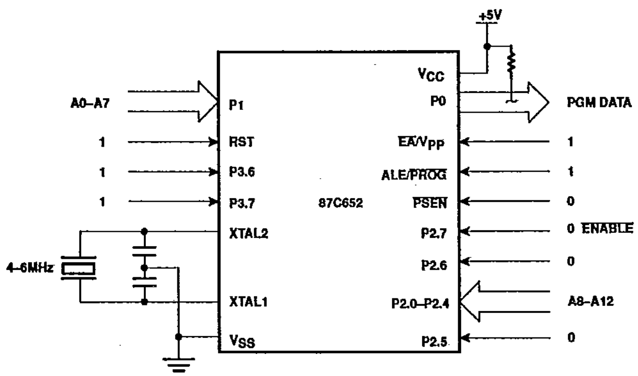

Figure 16. Program Verification

EPROM PROGRAMMING AND VERIFICATION CHARACTERISTICS

T_{amb} = 21°C to +27°C, V_{CC} = 5V±10%, V_{SS} = 0V (see Figure 17)

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{PP}	Programming supply voltage	12.5	13.0	V
I_{PP}	Programming supply current		50	mA
$1/t_{CLCL}$	Oscillator frequency	4	6	MHz
t_{AVGL}	Address setup to $\overline{PROG}$ low	$48t_{CLCL}$		
t_{GHAX}	Address hold after $\overline{PROG}$	$48t_{CLCL}$		
t_{DVGL}	Data setup to $\overline{PROG}$ low	$48t_{CLCL}$		
t_{GHDX}	Data hold after $\overline{PROG}$	$48t_{CLCL}$		
t_{EHSH}	P2.7 ($\overline{ENABLE}$) high to V_{PP}	$48t_{CLCL}$		
t_{SHGL}	V_{PP} setup to $\overline{PROG}$ low	10		µs
t_{GHSL}	V_{PP} hold after $\overline{PROG}$	10		µs
t_{GLGH}	$\overline{PROG}$ width	90	110	µs
t_{AVQV}	Address to data valid		$48t_{CLCL}$	
t_{ELQZ}	$\overline{ENABLE}$ low to data valid		$48t_{CLCL}$	
t_{EHQZ}	Data float after $\overline{ENABLE}$	0	$48t_{CLCL}$	
t_{GHGL}	$\overline{PROG}$ high to $\overline{PROG}$ low	10		µs

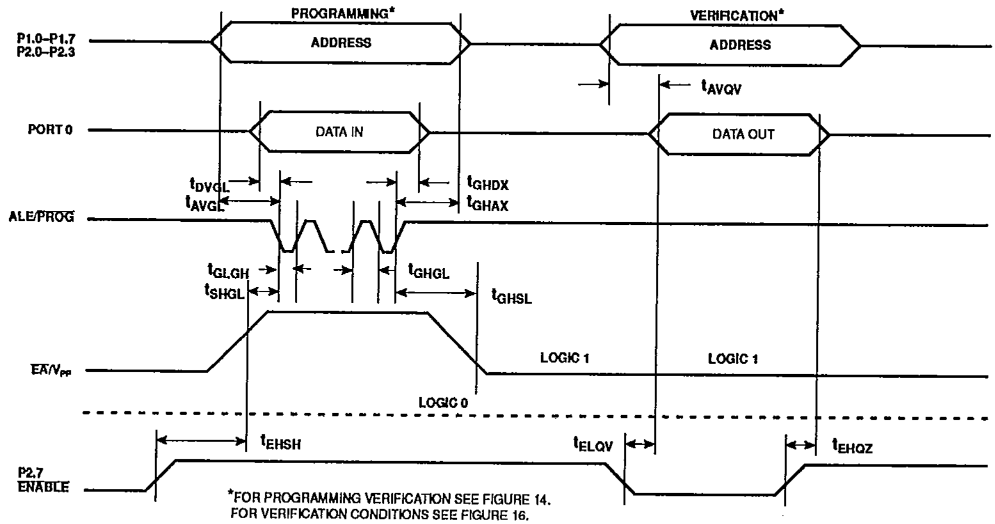

Figure 17. EPROM Programming and Verification

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.