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SSI 32P4731/41
Read Channel with 1,7 ENDEC, 4-burst Servo

Advance Information

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DESCRIPTION

The SSI 32P4731/41 devices are high performance BiCMOS single chip read channel ICs that contain all the functions needed to implement a complete zoned recording read channel for hard disk drive systems. Functional blocks include the pulse detector, programmable filter, 4-burst servo capture, time base generator, and data separator with 1,7 RLL ENDEC. Data rates can be programmed using an internal DAC whose reference current is set by a single external resistor.

Programmable functions of the SSI 32P4731/41 devices are controlled through a bi-directional serial port and banks of internal registers. This allows zoned recording applications to be supported without changing external component values from zone to zone.

The SSI 32P4731/41 utilize an advanced BiCMOS process technology along with advanced circuit design techniques which result in high performance devices with low power consumption.

FEATURES

GENERAL:
- DAC controlled programmable data rates
  - 32P4731 - 8 to 24 Mbit/s
  - 32P4741 - 14 to 40 Mbit/s
- Complete zoned recording application support
- Low power operation -
  - 32P4731 - 400 mW typical @ 5V
  - 32P4741 - 500 mW typical @ 5V
- Bi-directional serial port for register access
- Register programmable power management (Sleep mode <1 mW)
- Power supply range (4.5 to 5.5 volts)
- Small footprint 64-pin TQFP package

PULSE DETECTOR:
- Fast attack/decay modes for rapid AGC recovery
- Dual rate charge pump for fast transient recovery
- Low Drift AGC hold circuitry
- Temperature compensated, exponential control AGC
- Wide bandwidth, high precision full-wave rectifier
- Dual mode pulse qualification circuitry (user selectable)
- TTL $\overline{\text{RDIO}}$ signal output for servo timing support
- Internal LOW-Z and fast decay timing
- 0.5 ns max. pulse pairing

SERVO CAPTURE:
- 4-burst servo capture with A, B, C, D outputs
- Internal hold capacitors
- Programmable charge current (4-Bit DAC)
- Separate registers for FC and VTH during servo mode
- 4-bit DAC for AGC level control (0.75 to 1.0 Vpp)

PROGRAMMABLE FILTER:
- Programmable cutoff frequency
  - 32P4731 - 3 to 9 MHz
  - 32P4741 - 5 to 18 MHz
- Programmable boost/equalization of 0 to 13 dB
- Matched normal and differentiated outputs
- ± 10% *fc* accuracy
- ± 2% maximum group delay variation
- Less than 1% total harmonic distortion
- Low-Z input switch
- No external filter components required

TIME BASE GENERATOR:
- Better than 1% frequency resolution
- Up to 75 MHz frequency output
- Independent M and N divide-by registers
- VCO center frequency matched to data synchronizer VCO

DATA SEPARATOR:
- Fast acquisition phase lock loop with zero phase restart technique
  - 32P4731 - 3 x VCO
  - 32P4741 - 1.5 x VCO
- Integrated 1,7 RLL Encoder/Decoder
- Fully integrated data separator
  - No external delay lines or active devices required
  - No external active PLL components required
- Programmable decode window symmetry control via serial port
  - Window shift control ± 30% (4-bit)
  - Includes delayed read data and VCO clock monitor points
- Programmable early/late write precomp (3-Bits each)

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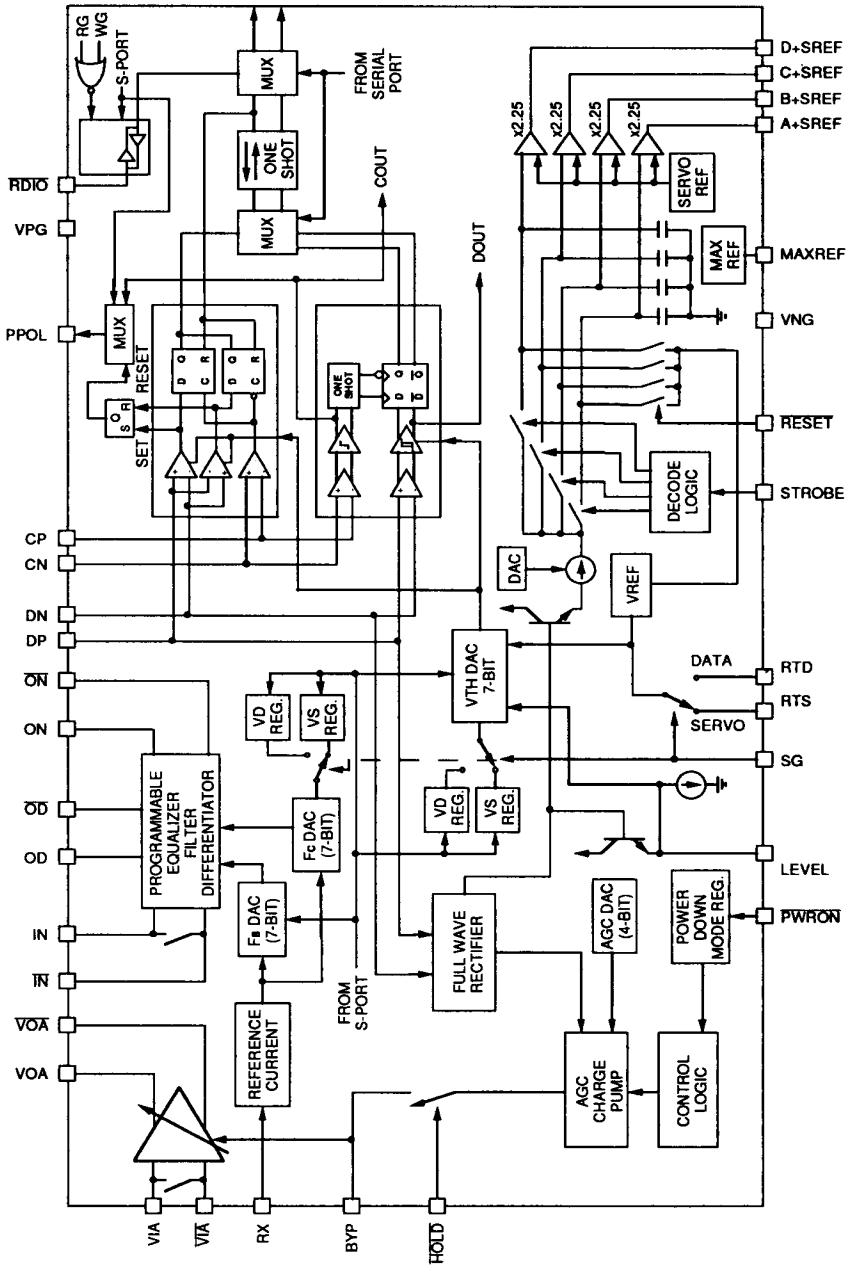

FIGURE 1(a): 32P4731/41 Block Diagram

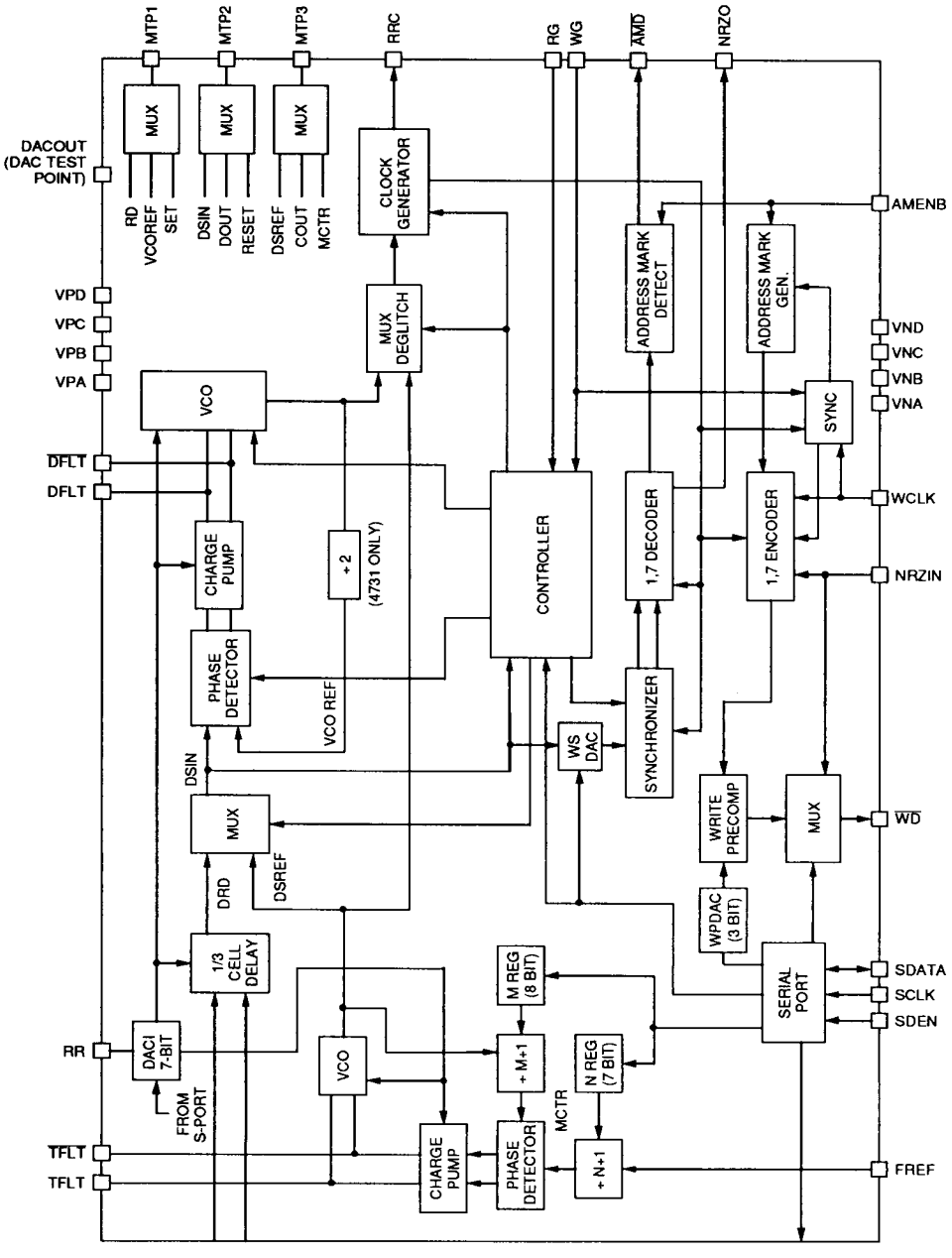

FIGURE 1(b): 32P4731/41 Block Diagram

FUNCTIONAL DESCRIPTION

The SSI 32P4731/41 implement a high performance complete read channel, including pulse detector, 4-burst servo capture, programmable active filter, time base generator, and data separator with 1,7 RLL ENDEC, at data rates up to 40 Mbit/s (32P4741). A circuit block diagram is shown in Figure 1.

Pulse Detector Circuit Description

The pulse detector, in conjunction with the programmable filter, provides all the data processing functions necessary for detection and qualification of encoded read signals. The signal processing circuits include a wide band variable gain amplifier; a wide bandwidth, high precision fullwave rectifier; and a dual rate charge pump. The entire signal path is fully-differential to minimize external noise pick up.

AGC Circuit

The gain of the AGC amplifier is controlled by the voltage (V_{BYP}) stored on the BYP hold capacitor (C_{BYP}). A dual rate charge pump drives C_{BYP} with currents that depend on the instantaneous differential voltage at the DP/DN pins. Attack currents lower V_{BYP} which reduces the amplifier gain, while decay currents increase V_{BYP} which increases the amplifier gain. When the signal at DP/DN is greater than 100% of the programmed AGC level, the nominal attack current of 0.18 mA is used to reduce the amplifier gain. If the signal is greater than 125% of the programmed AGC level, a fast attack current of eight (8) times nominal is used to reduce the gain. This dual rate approach allows AGC gain to be quickly decreased when it is too high yet minimizes distortion when the proper AGC level has been acquired.

A constant decay current of 4 μA increases the amplifier gain when the signal at DP/DN is less than the programmed AGC level. The large ratio (0.18 mA:4 μA) of the nominal attack and nominal decay currents enables the AGC loop to respond to the peak amplitudes of the incoming read signal rather than the average value. A fast decay current mode is provided to allow the AGC gain to be rapidly increased to reduce the recovery time between mode switches.

AGC Mode Control

When write gate (WG) is driven high, the dual rate charge pump is disabled causing the AGC amplifier gain to be held constant. The input impedance of both the AGC amplifier and the programmable filter is reduced. When the WG pin transitions from high to low, the Low-Z mode is activated. In this mode, the input impedance at both the AGC amplifier and the programmable filter remain low to allow for quick recovery of the AC coupling capacitors. Directly following the Low-Z mode is the fast decay mode which allows rapid acquisition of the proper AGC level. In fast decay mode, an internal FET is switched on to drive a high current into the BYP pin. The current remains active until the signal at DP/DN is above 125% of the nominal amplitude, or until an internal timer expires. The duration of both the Low-Z and fast decay modes is internally set at a nominal 1 μs. Fast decay mode is also triggered by a transition of the servo gate (SG) pin in either direction. When the pulse detector is powered-down, V_{BYP} will be held constant subject to leakage currents only. Upon power-up, the Low-Z/fast decay sequence is executed to rapidly recover from any transients or drift which may have occurred on the BYP hold capacitor.

External control for enabling the dual rate charge pump is also provided. Driving the $\overline{HOLD}$ pin low forces the dual rate charge pump output current to zero. In this mode, V_{BYP} will be held constant subject only to leakage currents.

$\overline{RDIO}$ Output Pin

A CMOS compatible inverted Read Data I/O ($\overline{RDIO}$) is provided to monitor the pulse detector output. This pin will be held high when SG is low and either RG or WG are high to reduce noise and accompanying jitter during read or write modes. Its falling edge indicates the occurrence of valid data pulse.

Qualifier Selection

The 32P4731/41 provide both hysteresis and dual comparator pulse qualification circuits that may be independently selected for read mode and servo mode operation. For read mode operation the pulse qualifier method is selected by setting the MSB in the data threshold control register (DTCR). The lower 7 bits of the DTCR also set the hysteresis level of the comparators for read mode. For servo mode operation the pulse qualifier method is selected by setting the MSB in the servo threshold control register (STCR). The lower 7 bits of the STCR set the hysteresis level of the comparators for servo mode.

Dual Comparator Qualification

When in dual comparator mode, independent positive and negative threshold qualification comparators are

used to suppress the error propagation of a positive and negative threshold hysteresis comparator. However a slight amount of hysteresis is included to increase the comparator output time when a signal that just exceeds the threshold level is detected. This eases the timing with respect to the zero crossing clock comparator. A differential comparator with programmable hysteresis threshold allows differential signal qualification for noise rejection. The programmable hysteresis threshold, VTH, is driven by a multiplying DAC which is driven by the LEVEL voltage and referenced to VRC. Hysteresis thresholds from 10 to 80% may be set with a resolution of better than 1%. A parallel R-C network of RTD and CT sets the hysteresis threshold time constant when not in the Servo mode. A qualified signal zero crossing at the CP-CN inputs triggers the output one shot, Figure 2(a).

Hysteresis Comparator Qualification

When the hysteresis qualification mode is selected, the same threshold qualification comparators and clock comparators are used to implement a polarity checking rule. In this mode, a positive peak that clears the established threshold level will set the hysteresis comparator and trigger the bidirectional one-shot that creates the read data pulses. In order to get another pulse clocked out, a peak of the opposite polarity must clear the negative threshold level to reset the hysteresis comparator and trigger the bidirectional one-shot. Figure 2(b).

Servo Demodulator Circuit Description

The 32P4731/41 servo sections capture four separate servo bursts and provide A, B, C, and D burst outputs. Internal burst hold capacitors are provided to support low leakage burst capture and reduce external component count. To support embedded servo applications, the 32P4731/41 provides additional programming registers that set the filter cutoff frequency (fc) and the hysteresis threshold level (VTH) for servo mode. When SG is activated or deactivated there is a maximum 1.5 µs settling time for the internal DACs to recover from the register switching.

Servo Mode Operation

When the servo gate (SG) is asserted, the control DACs for fc and VTH switch from the data mode registers to the servo mode registers and the AGC goes into the fast decay mode. In addition, filter boost is disabled (as determined by the boost control bit), the AGC level is adjusted according to the AGC Level DAC and the RTS servo time constant setting resistor is connected to VRC (VRC is the internal bandgap reference.) By disabling the boost and providing the

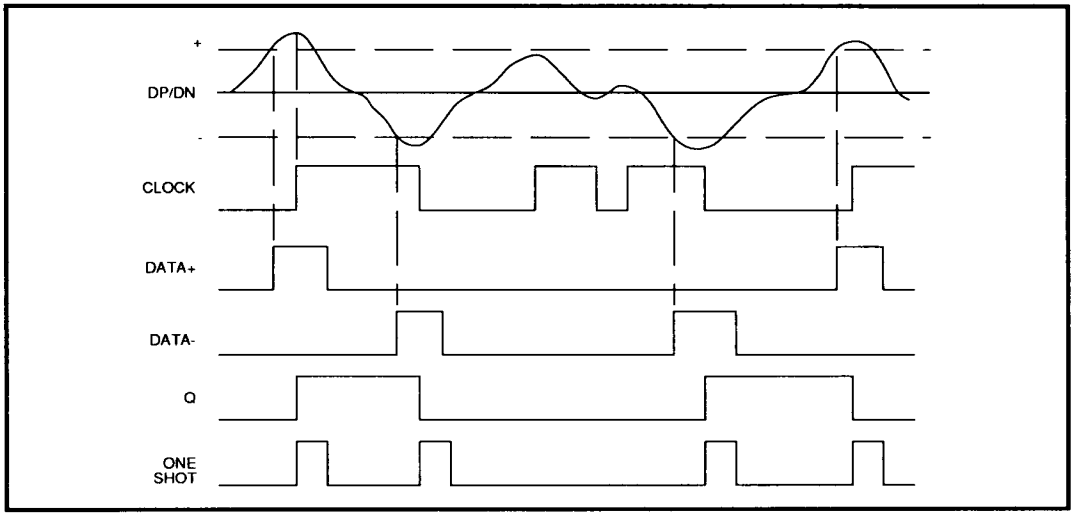

FIGURE 2(a): Dual Comparator Timing Diagram

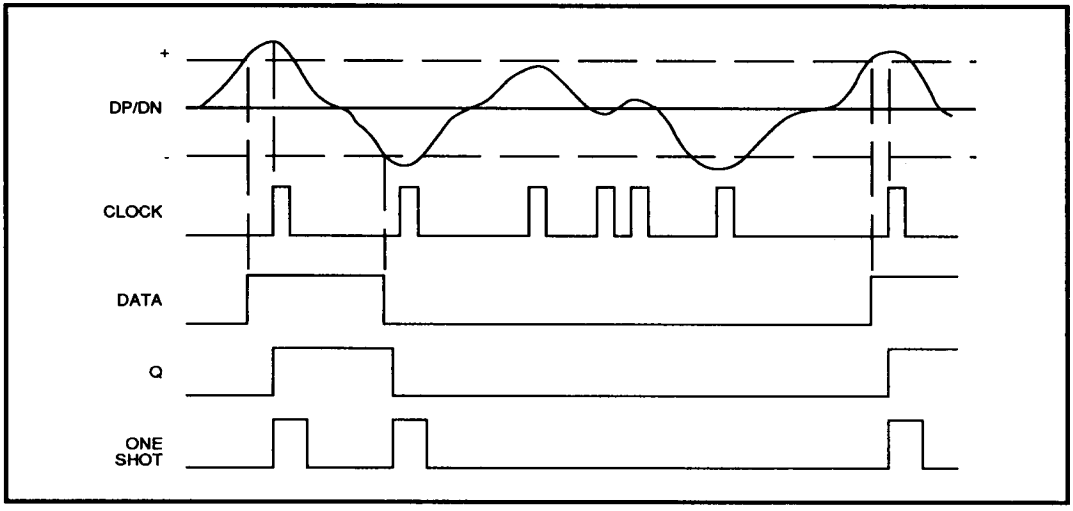

FIGURE 2(b): Hysteresis Comparator Timing Diagram

FUNCTIONAL DESCRIPTION (continued)

servo control register for *fc* the servo signal to noise ratio can be greatly improved. When SG is activated or deactivated there is a maximum 1.5 µs settling time for the internal DACs to recover from the register switching. During servo mode, the AGC circuit remains active. A 4-bit DAC (DACA) is used to set the AGC level over a range of 0.75 to 1.00 Vpp as follows:

VAGC = 1.00 - (DACA x 0.01667) Vpp
where DACA is the value of the AGC Level register

Typically, a servo preamble is used to achieve the desired AGC level and then the $\overline{\text{HOLD}}$ pin is asserted to hold the AGC gain. When SG goes low to terminate the servo mode, the AGC goes into the Fast Decay mode for 1.0 µs to allow for fast transition into the read mode.

Burst Capture

Burst capture is controlled by a single external pin designated STROBE and an internal counter. When SG is active, the first pulse on the STROBE pin gates the output of the servo peak detector to the A burst hold capacitor. The capacitor charges for as long as the STROBE pulse is high. On the falling edge of the STROBE signal, the internal counter is incremented. The next STROBE pulse will then gate the servo peak detector output to the B burst hold capacitor. Again, the capacitor charges for as long as the STROBE pulse is high. On the falling edge of STROBE, the counter is incremented again and the C burst is captured on the next STROBE pulse. On the next falling edge of STROBE, the counter is incremented again and the D burst is captured on the next STROBE pulse. After the falling edge of the fourth STROBE pulse, the counter is reset to zero and the burst capture process can be repeated. The internal counter is also reset when the SG pin is deactivated. The voltage level on the hold capacitors are buffered and amplified to generate the servo output signals. A 1.0 Vp-p differential voltage at the DP/DN pins will result in a 2.25V peak burst amplitude. The servo output signals (A, B, C, D) are referenced above an internal baseline of 0.5 volts. The output voltage at the MAXREF pin is a nominal 3.0V, and represents the maximum voltage to which the servo signal outputs will swing. It is typically used as the reference voltage for an external A/D converter. MAXREF is internally reduced to a 0.5 volt level, and establishes the servo zero-signal baseline. All four internal burst hold capacitors are discharged when the $\overline{\text{RESET}}$ pin is driven low. When the PKRESET bit is set high, the capacitors are reset below the 0.5 volt baseline. When PKRESET bit is low, the capacitors are reset to the 0.5 volt baseline.

The drive current of the servo peak detector charge pump is set by a 4-bit word (DACP) addressed through the serial port. The LSB value is 6 µA, and the offset is 1 LSB such that "0000" corresponds to 6 µA and "1111"results in 96 µA. Maximum noise immunity is obtained in the servo peak detector by choosing the smallest value of charge current to charge the internal 10 pF hold capacitor during the burst acquisition time.

Timing Outputs

To support servo timing recovery, the pulse detector section provides a CMOS output of the servo information via the $\overline{\text{RDIO}}$ pin. A negative pulse is generated for each servo peak that is qualified through the pulse detector circuitry. Additional servo timing information is supported by the PPOL output. The PPOL pin provides pulse polarity information for the qualified peaks, where a high level TTL output indicates a positive pulse. To reduce noise progagation, $\overline{\text{RDIO}}$ and PPOL will not toggle when either RG or WG are active.

PROGRAMMABLE FILTER CIRCUIT DESCRIPTION

The SSI 32P4731/41 programmable filter consist of an electronically controlled low-pass filter with a separate differentiated low-pass output. A seven-pole, low-pass filter is provided along with a single-pole, single-zero differentiator. Both outputs have matched group delays (< 1 ns typical.) A fixed delay of 1.25 ns (typ.) is added to the differentiated outputs to guarantee set-up timing in the data qualifier circuit. The delay matching is unaffected by any amount of programmed equalization or bandwidth. Programmable bandwidth and boost/ equalization is provided by internal 7-bit control DACs. Differentiation pulse slimming equalization is accomplished by a two-pole, low-pass with a two-pole, high-pass feed forward section to provide complimentary real axis zeros. A variable attenuator is used to program the zero locations. The filter implements a 0.05 degree equiripple linear phase response.

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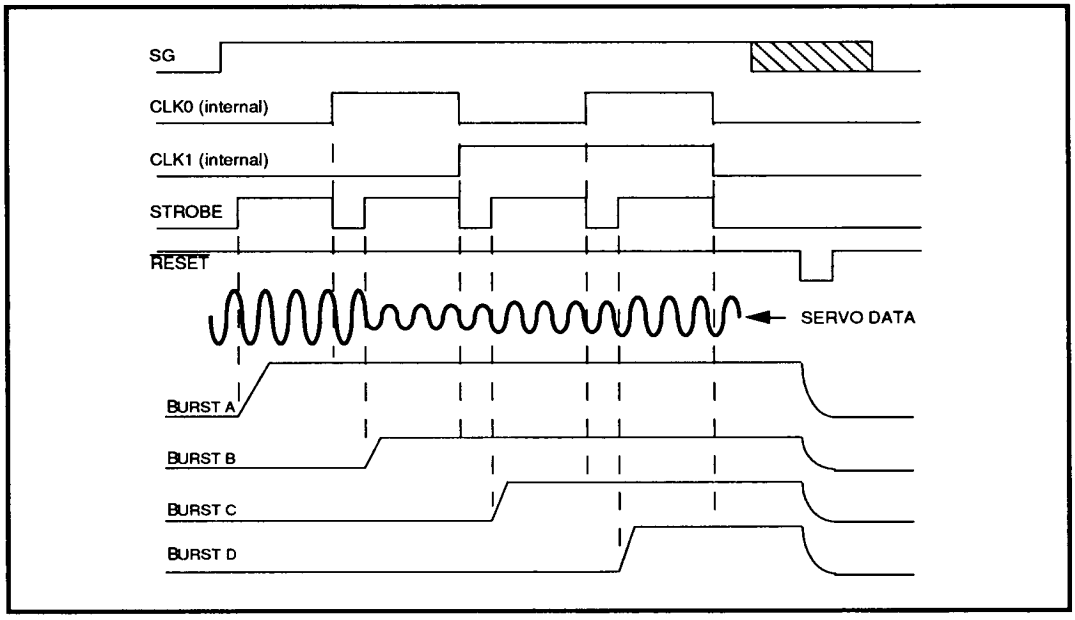

FIGURE 3: Servo Capture Timing

FUNCTIONAL DESCRIPTION (continued)

The normalized transfer functions (i.e., $\omega c = 2\pi fc = 1$) are:

$$Vnorm/Vi = [(-Ks^2 + 17.98016)/D(s)] \times An$$

and

$$Vdiff/Vi = (Vnorm/Vi) \times (s/0.86133) \times Ad$$

Where D (s)=

$(s^2+1.68495s+1.31703)(s^2+1.54203\ s+2.95139)(s^2+1.14558s+5.37034)(s+0.86133)$,

An and Ad are adjusted for a gain of 2 at $fs=(2/3)fc$.

Filter Operation

AC coupled differential signals from the AGC amplifier are applied to the IN/$\overline{IN}$ inputs of the filter. To improve settling time of the coupling capacitors, the IN/$\overline{IN}$ inputs are placed into a Low-Z state for 1.0 µs when WG goes inactive or when the $\overline{PWRON}$ pin is brought low. The programmable bandwidth and boost/equalization features are controlled by internal DACs and the registers programmed through the serial port. The current reference for both DACs is set using a single external resistor connected from pin RX to ground. The voltage at pin RX is proportional to absolute temperature (PTAT), hence the current for the DACs is a PTAT reference current.

Bandwidth Control

The programmable bandwidth is set by the filter cutoff DAC. This DAC has two separate 7-bit registers that can program the DAC value as follows:

fc = 0.0708 x DACF (MHz), for the 32P4731

fc = 0.1417 x DACF (MHz), for the 32P4741

where DACF = DMCR or SMCR value

In the data mode, the Data Mode Cutoff Register (DMCR) is used to determine the filter's 3 dB cutoff frequency. In the servo mode, the Servo Mode Cutoff Register (SMCR) is used. Switching of the registers is controlled by the servo gate (SG) pin. The filter cutoff set by the internal DAC is the unboosted 3 dB frequency. When boost/equalization is added, the actual 3 dB point will move out. Table 1 provides information on boost verses 3 dB frequency.

Boost/Equalization Control

The programmable equalization is also controlled by an internal DAC. The 7-bit Filter Boost Control Register (FBCR) determines the amount of equalization that will be added to the 3 dB cutoff frequency, as follows:

Boost = 20 log [(0.0273 x FBCR) + 1] (dB)

For example, with the DAC set for maximum output (FBCR = 7F or 127) there will be 13 dB of boost added at the 3 dB frequency. This will result in +10 dB of signal boost above the 0 dB baseline. When SG is active the boost can be disabled by setting bit 7 in FBCR. When bit 7 is "0" and SG is active the boost will automatically be set to 0 dB. If bit 7 is "1" the boost will remain at its programmed value regardless of the state of SG.

Time Base Generator Circuit Description

The time base generator, which is a PLL based circuit, provides programmable reference frequency FOUT. The frequency can be programmed with an accuracy

TABLE 1: 3 dB Cutoff Frequency versus Boost Magnitude

BOOST (dB)	fc Multiplier	BOOST (dB)	fc Multiplier
0	1.00	7	2.42
1	1.21	8	2.51
2	1.50	9	2.59
3	1.80	10	2.66
4	2.04	11	2.73
5	2.20	12	2.80
6	2.32	13	2.88

better than 1%. An external passive loop filter is required to control the PLL locking characteristics. The filter is fully-differential and balanced in order to suppress common mode noise.

In Read, Write and Idle modes, the time base generator is programmed to provide a stable reference frequency (FOUT) for the data synchronizer. In Write and Idle modes, FOUT is the output of the time base generator. In Read mode FOUT is disabled after the data synchronizer has achieved lock and switched over to read data as the source for the RRC. This minimizes jitter in the data synchronizer PLL. The reference frequency is programmed using the M and N registers of the time base generator via the serial port, and is related to the external reference clock input, FREF, as follows:

$$FOUT = ((M+1)/(N+1))FREF$$

The VCO center frequency and the phase detector gain of the time base generator are controlled by an internal DAC addressed through the data recovery control register (DRCR). This DAC also sets the 1/3 cell delay, VCO center frequency, and phase detector gain for the data synchronizer circuitry.

$$Fvco = [12.5/(RR+0.4)] \times [(0.622 \times IDAC) + 4.27] \text{ MHz}$$

where IDAC is the value in the DRCR and RR is the value (kΩ) of the external RR resistor.

DATA SEPARATOR CIRCUIT DESCRIPTION

The data separator circuit provides complete encoding, decoding, and synchronization for RLL 1,7 format data. In the Read mode, the circuit performs sync field search and detect, data synchronization, address mark detection, and data decoding. In the Write mode, the circuit provides address mark generation, data encoding, and write precompensation for NRZ data applied to the NRZIN pin. Data rate is established by the time base generator and DACI. The DAC generates a reference current which sets the VCO center frequency, the phase detector gain, and the 1/3 cell delay.

Phase Locked Loop

The circuit employs a dual mode phase detector; harmonic in the Read mode and non-harmonic in the Write and Idle modes. In the read mode the harmonic phase detector updates the PLL with each occurrence of a $\overline{DRD}$ pulse. In the Write and Idle modes the non-harmonic phase detector is continuously enabled, thus maintaining both phase and frequency lock onto the reference frequency of the internal time base generator. By acquiring both phase and frequency lock to the input reference frequency and utilizing a zero phase restart technique, the VCO transient is minimized and false lock to DLYD DATA is eliminated. The phase detector incorporates a charge pump in order to drive the loop filter directly. The polarity and width of the output current pulses correspond to the direction and magnitude of the phase error.

The data synchronizer also requires an external passive loop filter to control its PLL locking characteristics. This filter is also fully-differential and balanced in order to suppress common mode noise.

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READ/WRITE MODE CONTROL

The read gate (RG) and write gate (WG) inputs control the device operating mode. RG is an asynchronous input and may be initiated or terminated at any position on the disk. WG is also an asynchronous input, but should not be terminated prior to the last output write data pulse.

Read Mode

The data synchronizer utilizes a fully integrated fast acquisition PLL to accurately develop the decode window. Read gate (RG) initiates the PLL locking sequence and selects the PLL reference input; a high level (read mode) selects the internal $\overline{DRD}$ signal and a low level selects the reference clock. In the read mode the falling edge of $\overline{DRD}$ enables the phase detector while the rising edge is phase compared to the rising edge of the VCO reference (VCOR.) As depicted in Figure 5, $\overline{DRD}$ is a 1/3 cell wide (TVCO) pulse whose leading edge is defined by the falling edge of $\overline{RD}$. A decode window is developed from the VCOR clock.

Read Mode Soft Sector Operation

In soft sector operation the address mark must be detected before RG can be asserted to continue read mode operation. Soft sector operation is entered by driving the AMENB pin high to initiate an address mark search function. An address mark pattern consists of two 8T patterns followed by two 12T patterns. The address mark detect circuit searches the internal read data ($\overline{RD}$) for the address mark pattern. First the address mark detect circuit looks for a 6 "0's" within the 8T patterns. Having detected a 6 "0's" the address mark detect circuit then looks for a 9 "0's" within the 12T

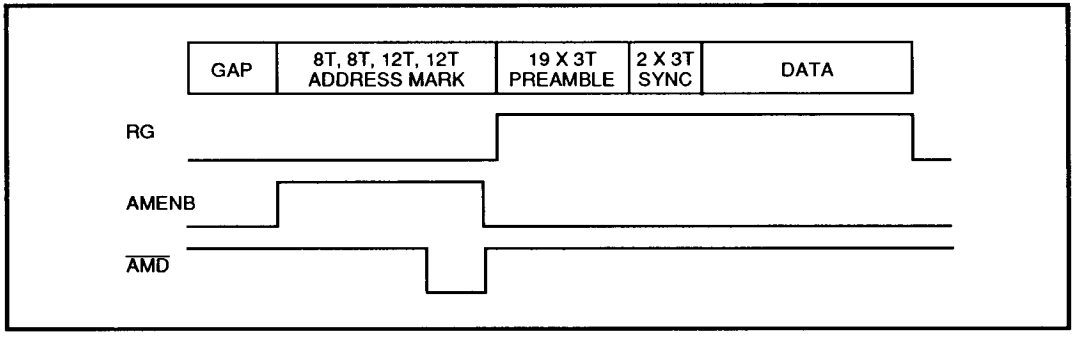


FIGURE 4: Read Mode Soft Sector Operation

FUNCTIONAL DESCRIPTION (continued)

patterns. If the 9 "0's" pattern is not detected within 5 $\overline{RD}$ bits after detecting the 6 "0's" pattern, the address mark detect sequence will reset and look for a 6 "0's" pattern again. When the address mark detect circuit has acquired a 6 "0's", 9 "0's" sequence the $\overline{AMD}$ output transitions low. $\overline{AMD}$ will remain low until the AMENB input is driven low. Reference Figure 4.

Preamble Search

After the address mark (AM) has been detected, RG can be asserted to initiate the preamble search. When RG is asserted, an internal counter is triggered to count positive transitions of the internal read data, RD. Once the counter reaches count 3 (3 consecutive 3T patterns detected) the internal read gate is enabled. This switches the phase detector reference from the internal time base to the delayed read data ($\overline{DRD}$) signal. At the same time an internal zero phase restart signal restarts the VCO in phase with the $\overline{DRD}$. This prepares the VCO to be synchronized to data when the bit sync circuitry is enabled after VCO lock is established.

VCO Lock and Bit Sync Enable

One of two VCO locking modes will be entered depending on the state of the gain shift (GS) bit, or bit 1, in the Control B register. If GS = "1", the phase detector will enter a gain shift mode of operation. The phase detector starts out in a high gain mode of operation to support fast phase acquisition. After an internal counter counts the first 14 transitions of the internal $\overline{DRD}$ signal, the gain is reduced by a factor of 3. This reduces the bandwidth and damping factor of the loop by $\sqrt{3}$ which provides improved jitter performance in the data follow mode. The counter continues to count the next 4 $\overline{DRD}$ transitions (a total of 19 x 3T from assertion of RG) and then asserts an internal VCO lock signal. The VCO lock signal activates the decoder bit synchronization circuitry to define the proper decode boundaries. The next 2 x 3T patterns are used to set the proper decode window so that VCO is in sync with RRC and RRC is in sync with the data. Following this, the NRZ output is enabled and the data is toggled through the decoder for the duration of the RG.

When the VCO lock signal is asserted, the internal RRC source is also switched from the time base generator to the VCO clock signal that is phase locked to $\overline{DRD}$. During the internal RRC switching period the external RRC signal may be held for a maximum of 2 NRZ clock periods, however no short duration glitches will occur.

When the GS bit is set to "0" the phase detector gain shift function is disabled. The VCO lock sequence is identical to that of the gain shift mode explained above, except that no gain shift is made after the first 15 transitions.

Split Field Servo Operation

The data separator circuit supports split field servo operation. For soft sector operation, the AMENB pin is asserted only at the beginning of the data sector (see Figure 7.) Within the data sector and following the servo burst, it is not necessary to provide another address mark pattern.

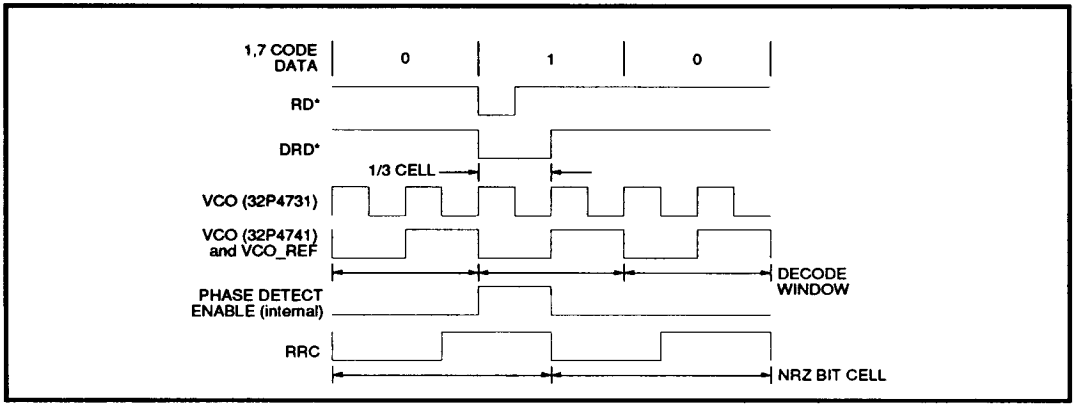


FIGURE 5: Data Synchronization Waveform

When SG goes low after the servo burst, the hard sector VCO lock sequence is automatically initiated. This reduces the overhead required.

READ MODE HARD SECTOR OPERATION

The hard sector operation is entered by holding the AMENB pin low. In hard sector operation, $\overline{AMD}$ remains inactive and the address mark search sequence is not entered. The hard sector read operation starts with assertion of the RG. Once read gate is asserted the VCO lock sequence is identical to the soft sector operation.

Window Shift

Shifting the phase of the VCO clock effectively shifts the relative position of the $\overline{DRD}$ pulse within the decode window. Decode window control is provided via the WS control bits of the Window Shift Control Register (WSCR). Further description of the WSCR will follow.

Non-Read Mode

In the non-Read modes, the PLL is locked to the reference clock. This forces the VCO to run at a frequency which is very close to that required for tracking actual data. When the reference input to the PLL is switched, the VCO is stopped momentarily, then restarted in an accurate phase alignment with the next PLL reference input pulse. By minimizing the phase alignment error in this manner, the acquisition time is substantially reduced.

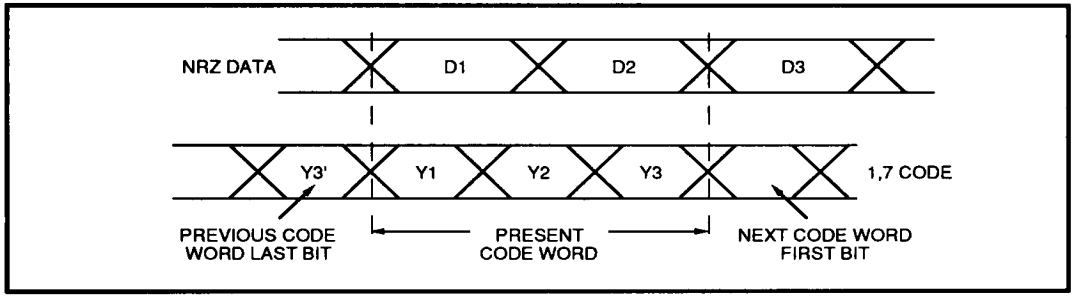


FIGURE 6: NRZ Data Word to 1, 7 Code Word Bit Comparision
(Reference Table 4 for decode scheme)

FUNCTIONAL DESCRIPTION (continued)

Write Mode

In the Write mode the circuit converts NRZIN data from the controller into 1,7 RLL formatted data for storage on the disk. In soft sector operation the circuit generates an address mark and a preamble pattern. In hard sector operation the circuit generates the preamble pattern but no preceding address mark. Write mode is entered by asserting WG while the RG is held low. During Write mode the VCO and the RRC are referenced to the internal time base generator signal, FOUT.

Write Mode Soft Sector Operation

In soft sector operation an address mark pattern is written prior to the preamble and encoded data. To initiate the soft sector mode the AMENB is asserted 1 NRZ period after WG is asserted. Once AMENB is asserted, the address mark pattern of two 8T patterns followed by two 12T patterns is automatically generated. Following the address mark pattern, 3T patterns will be generated as long as the NRZIN data is held low. While the address mark and preamble are being written the encoder is active. Therefore, WCLK must be toggling and NRZIN must be held low ("0".) The first non zero NRZIN input bit indicates the end of the preamble pattern. After a delay of 5 NRZIN bit time periods, non-preamble data begins to toggle out of $\overline{WD}$. At the end of the write cycle, 5 bits of blank NRZ time passes to insure the encoder is flushed of data before the WG can be transitioned low. $\overline{WD}$ stops toggling a maximum of 2 NRZ (RRC) time periods after WG goes low. Reference Figures 9 and 12 for detailed timing information.

Write Mode Hard Sector Operation

In hard sector operation AMENB is held low and no address mark pattern is generated. The preamble pattern is generated in the same sequence as the soft sector operation. During preamble generation the WCLK is toggled and NRZIN data is held low ("0".) Termination of a hard sector write operation follows the same sequence as soft sector mode.

Direct Write Function

The 32P4731/41 includes a Direct Write (DW) function that allows the NRZIN data to bypass the encoder and write precomp circuitry. When the DW bit is set in the CBR, the data applied to NRZIN will bypass the encoder and write precomp and directly control the WD output buffer. This allows the user to perform DC erase and media tests.

Operating Modes and Control

The 32P4731/41 has several operating modes that support read, write, servo, and power management functions. Mode selection is accomplished by controlling the read gate (RG), write gate (WG), servo gate (SG), and $\overline{PWRON}$ pins. Additional modes are also controlled by programming the Power Down Control Register (PDCR), the Control A (CAR) register, and the Control B (CBR) register via the serial port.

External Mode Control

For normal operation the $\overline{PWRON}$ pin is driven low. During normal operation the 32P4731/41 is controlled by the read gate (RG), write gate (WG), and servo gate (SG) pins. (Reference Table 2.)

Control Registers

Control registers CAR and CBR allow the user to configure the 32P4731/41 test points for evaluation of different internal signals and also control other device functions. CAR controls functions of the pulse detector, filter, and time base generator. CBR controls test points and functions of the data separator.

Power Down Control

For power management, the $\overline{PWRON}$ pin can be used in conjunction with the Power Down Control Register (PDCR) to set the operating mode of the device. The PDCR provides a control bit for each of the functional blocks. When the $\overline{PWRON}$ pin is brought high ("1") the device is placed into Sleep mode (<5 mW) and all circuits are powered down except the serial port. This allows the user to program the serial port registers while still conserving power. Register information is retained during the Sleep mode so it is not necessary to reprogram the serial port registers after returning to an Active mode. When the $\overline{PWRON}$ pin is driven low ("0"), the contents of the PDCR determine which blocks will be active. Register mapping for the PDCR is shown in Table 3. To improve recovery time from the Sleep mode, the inputs to the AGC, Filter and DP/DN are placed into a Low-Z mode for 1 μs.

Following the Low-Z mode the AGC is placed into the fast decay mode.

Serial Interface Operation

The serial interface is a bi-directional port for reading and writing programming data from/to the internal registers of the 32P4731/41. For data transfers SDEN is brought high, serial data is presented at the SDATA pin, and a serial clock is applied to the SCLK pin. After the SDEN goes high, the first 16 pulses applied to the SCLK pin will shift the data presented at the SDATA pin into an internal shift register on the rising edge of each clock. An internal counter prevents more than 16 bits from being shifted into the register. The data in the shift register is latched when SDEN goes low. If less than 16 clock pulses are provided before SDEN goes low, the data transfer is aborted.

All transfers are shifted into the serial port LSB first. The first byte of the transfer is address and instruction information. The LSB of this byte is the R/W bit which determines if the transfer is a read (1) or a write (0). The remaining 7-bits determine the internal register to be accessed. Table 3 provides register mapping information. The second byte contains the programming data. In read mode (R/W = 1) the 32P4731/41 will output the register contents of the selected address. In write mode the device will load the selected register with data presented on the SDATA pin. At initial power-up, the contents of the internal registers will be in an unknown state and they must be programmed prior to operation. During power down modes, the serial port remains active and register programming data is retained. Detailed timing information is provided in Figure 13(b) and in the electrical specifications.

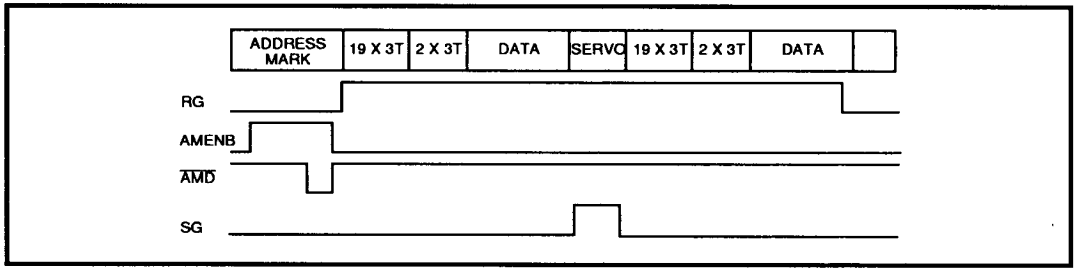


FIGURE 7: Split Field Servo Operation

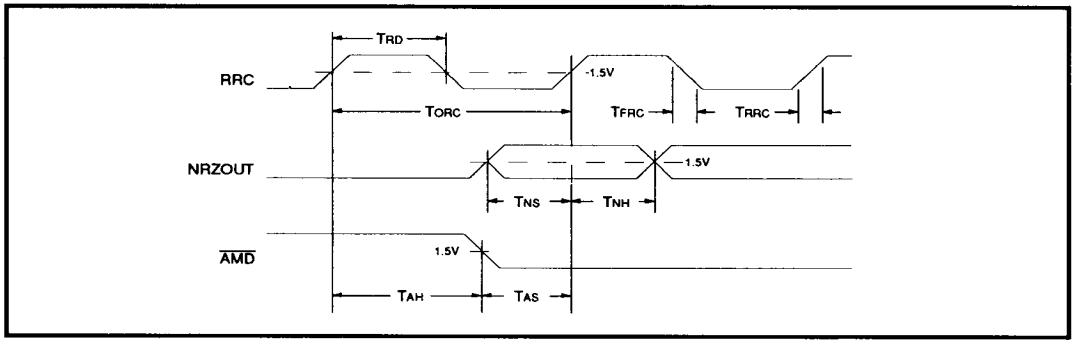


FIGURE 8: NRZ Read Timing

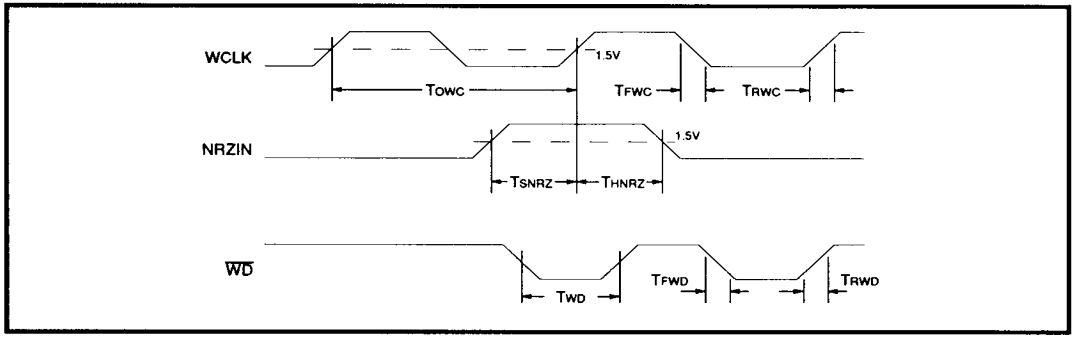


FIGURE 9: $\overline{WD}$ and NRZ Write Timing

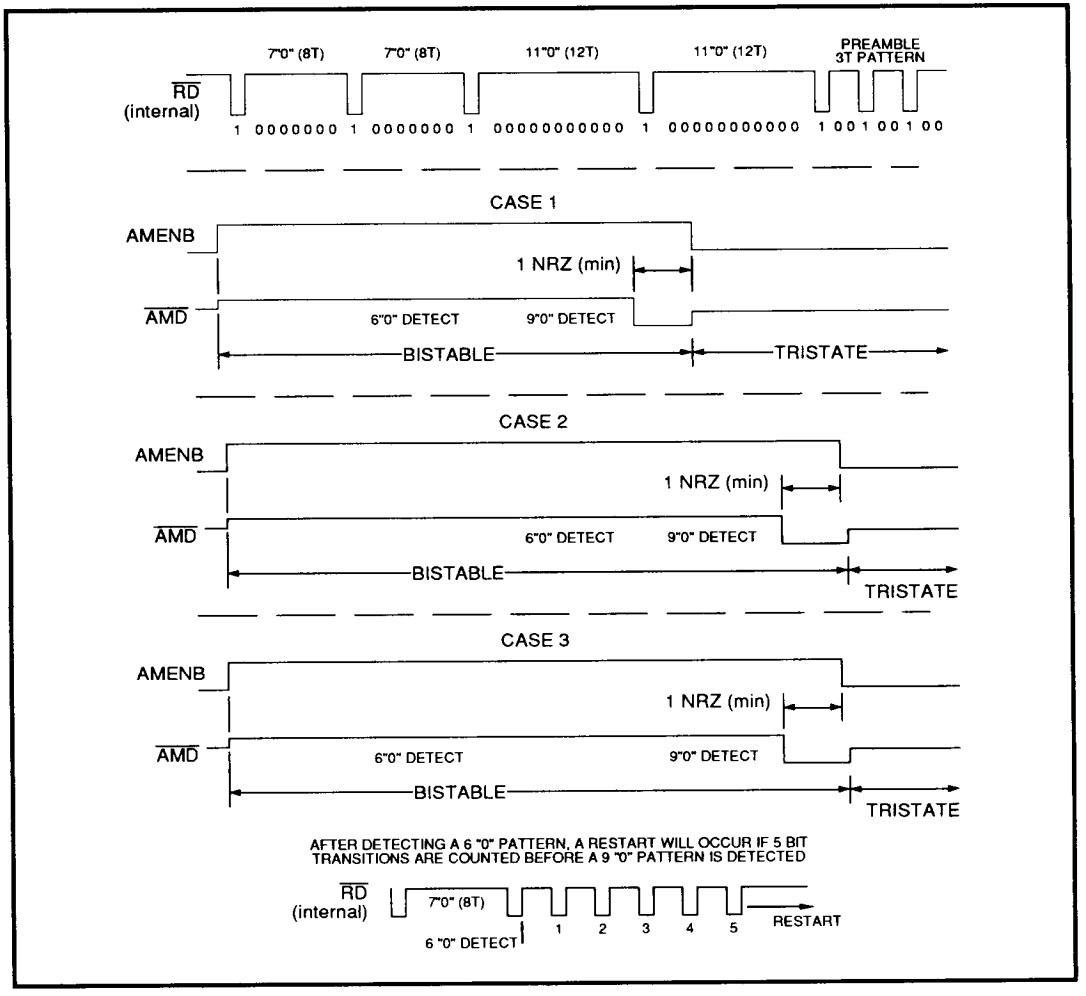


FIGURE 10: Address Mark Search (Soft Sector)

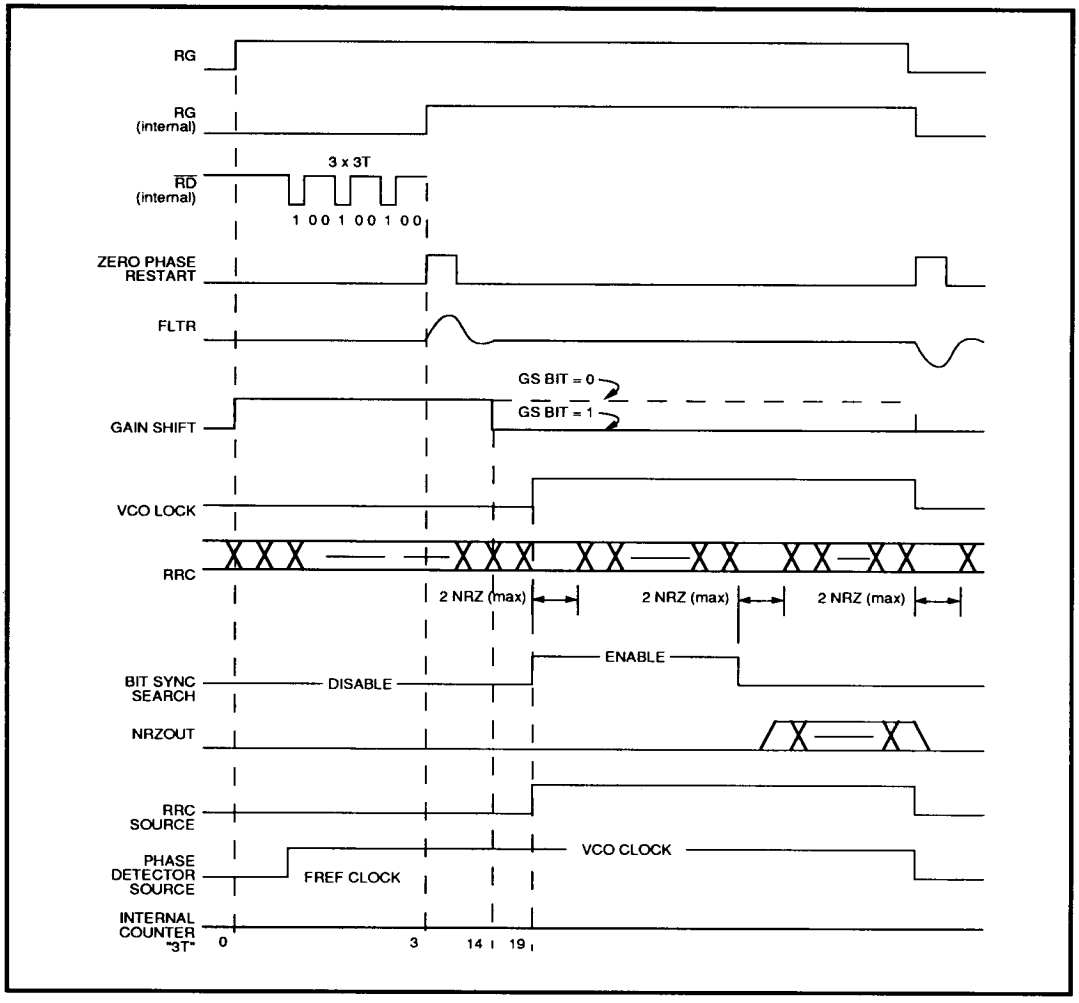


FIGURE 11: Read Mode Locking Sequence (Hard and Soft Sector)

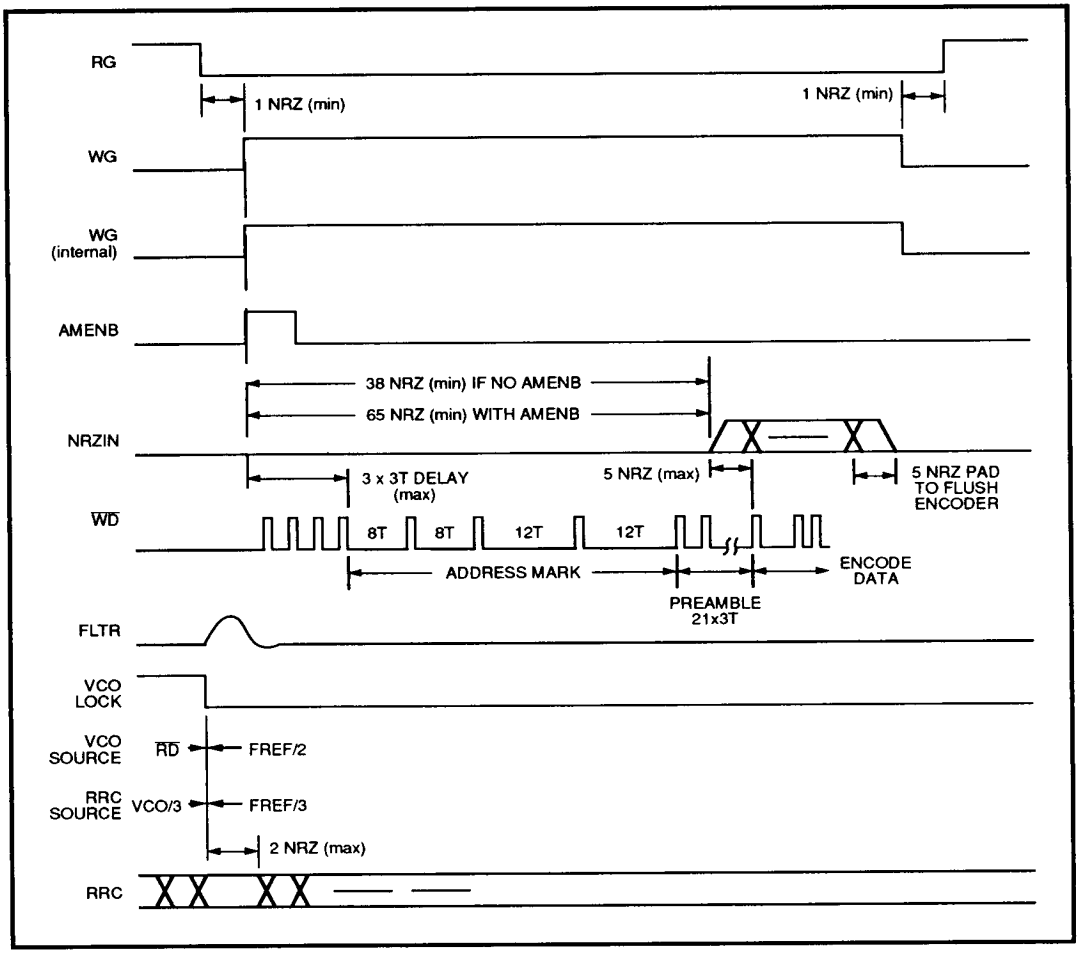


FIGURE 12: Write Data Operation (Hard and Soft Sector)

TABLE 2: Mode Control Table

CONTROL LINES				DEVICE MODE:	DAC CONTROL			
$\overline{PWRON}$	RG	SG	WG		VTH	FC	BOOST	AGC LEVEL
1	X	X	X	**SLEEP MODE:** All functions are powered down. The serial port registers remain active and register programming data is saved.	off	off	off	off
0	0	0	1	**WRITE MODE:** The pulse detector is inactive. The data synchronizer VCO is locked to the internal time base generator. Write precomp circuit is clocked by internal time base. $\overline{RDIO}$ and PPOL are inactive.	DR	DR	DR	DR
0	1	0	X	**READ MODE:** The pulse detector is active. The data synchronizer begins the preamble lock sequence. $\overline{RDIO}$ and PPOL are inactive.	DR	DR	DR	DR
0	X	1	X	**SERVO MODE:** The pulse detector is active and the servo control registers are enabled for the Fc DAC and the VTH DAC. $\overline{RDIO}$ and PPOL are active. The data synchronizer and time base generator can be disabled using the PDCR.	SR	SR	off	SR
0	0	0	0	**IDLE MODE:** The contents of the PDCR determine which blocks are powered-up. In normal operation with all blocks powered-up, the pulse detector is active, the data synchronizer VCO is locked to the time base generator, and the data control registers are used for VTH and FC.	DR	DR	DR	DR
				If multiple control signals are active, the priority order will be PWRON, SG, RG, and WG. For example, if SG and RG are both "1", the servo mode will be active.				

DAC CONTROL Key: DR = data register, SR = servo register, off = disabled

REGISTER NAME	A6	ADDRESS A0	R/W	D7	DATA BIT MAP --	--	TBG 1=DISABLE 0=ENABLE	DATA SEP 1=DISABLE 0=ENABLE	FILTER 1=DISABLE 0=ENABLE	--	D0
POWER DOWN CONTROL	0	0 0 0 0 1	0 0	--	--	--	TBG 1=DISABLE 0=ENABLE	DATA SEP 1=DISABLE 0=ENABLE	FILTER 1=DISABLE 0=ENABLE	--	PD/SERVO 1=DISABLE 0=ENABLE
DATA MODE CUTOFF	0	0 0 0 0 1	1 0	*	DAC BIT 6	DAC BIT 5	DAC BIT 4	DAC BIT 3	DAC BIT 2	DAC BIT 1	DAC BIT 0
SERVO MODE CUTOFF	0	0 1 0 0 1	1 0	*	DAC BIT 6	DAC BIT 5	DAC BIT 4	DAC BIT 3	DAC BIT 2	DAC BIT 1	DAC BIT 0
FILTER BOOST	0	0 0 1 0 1	1 0	SRVO BST 1=ENABLE 0=DISABLE	DAC BIT 6	DAC BIT 5	DAC BIT 4	DAC BIT 3	DAC BIT 2	DAC BIT 1	DAC BIT 0
DATA THRESHOLD	0	0 0 1 0 1	0 0	1=DUAL 0=HYS	DAC BIT 6	DAC BIT 5	DAC BIT 4	DAC BIT 3	DAC BIT 2	DAC BIT 1	DAC BIT 0
SERVO THRESHOLD	0	0 1 0 0 1	0 0	1=DUAL 0=HYS	DAC BIT 6	DAC BIT 5	DAC BIT 4	DAC BIT 3	DAC BIT 2	DAC BIT 1	DAC BIT 0
CONTROL A	0	0 1 1 0 1	0 0	Fast Decay test mode 0=ENABLE	TMS1	TMS0	TBG 1=BYPASS 0=NORMAL	TBG TEST POINT ENABLE	PUMP DWN 1=TP ON 0=TP OFF	PUMP UP 1=TP ON 0=TP OFF	PHASE DET 1=ENABLE 0=DISABLE
CONTROL B	0	0 0 1 1 0	0 0	*	MTPE 1=ENABLE 0=DISABLE	PUMP DWN 1=TP ON 0=TP OFF	PUMP UP 1=TP ON 0=TP OFF	PHASE DET 1=ENABLE 0=DISABLE	RDI 1 = INPUT 0 = OUTPUT	GAIN SHFT 1 = ON 0 = OFF	DIR WRITE 1 = ON 0 = OFF
N COUNTER	0	0 0 0 1 1	0 0	*	N COUNT BIT 6	N COUNT BIT 5	N COUNT BIT 4	N COUNT BIT 3	N COUNT BIT 2	N COUNT BIT 1	N COUNT BIT 0
M COUNTER	0	0 0 1 1 1	0 0	M COUNT BIT 7	M COUNT BIT 6	M COUNT BIT 5	M COUNT BIT 4	M COUNT BIT 3	M COUNT BIT 2	M COUNT BIT 1	M COUNT BIT 0
DATA RECOVERY	0	0 0 0 1 0	0 0	*	IDAC BIT 6	IDAC BIT 5	IDAC BIT 4	IDAC BIT 3	IDAC BIT 2	IDAC BIT 1	IDAC BIT 0
WINDOW SHIFT	0	0 0 0 1 0	1 0	TDAC 1	TDAC 0	WIN SHFT 1=ENABLE 0=DISABLE	WS DIR 1=LATE 0=EARLY	WS3*	WS2*	WS1*	WS0*
WRITE PRECOMP	0	0 0 1 1 0	1 0	PK RESET 1=HI RES 0=NORMAL	WL2*	WL1*	WL0*	WR PRCMP 1=ENABLE 0=DISABLE	WE2*	WE1*	WE0*
AGC LEVEL	0	1 0 0 0 1	0 0	DACP BIT 3	DACP BIT 2	DACP BIT 1	DACP BIT 0	DAC BIT 3	DAC BIT 2	DAC BIT 1	DAC BIT 0

TABLE 3: Serial Port Register Mapping

***These bits are used only for testing. They should be programmed to 0 in actual operation.**

Control Register CA:

BIT	NAME	FUNCTION
0	EPDT	Enable Phase Detector (Time Base Generator): This bit disables the output of the phase detector to the VCO. An external voltage applied across the TFLT pins drives the VCO to a fixed frequency. 1 = Phase detector active 0 = Phase detector charge pump disabled
1	UT	Enable Pump Up Current (Time Base Generator): This bit enables a test mode for checking the charge pump output current. The charge pump will source a fixed DC current from TFLT and sink the current at $\overline{\text{TFLT}}$. 0 = No current 1 = Maximum charge pump current
2	DT	Enable Pump Down Current (Time Base Generator): This bit enables a test mode for checking the charge pump output current. The charge pump will source a fixed DC current from $\overline{\text{TFLT}}$ and sink the current at TFLT. 0 = No current 1 = Maximum charge pump current
3	ET	This bit enables the MTP3 test point output buffer. 0 = Test point disabled 1 = Test point enabled
4	BYPT	This bit enables a time base generator bypasses mode where the FREF input is connected to the phase detector input. 0 = Time base enabled 1 = Time base bypassed
5/6	TMS0/1	These bits select the test point signal sources (refer to Table 7).
7	FDTM	This bit continuously enables the AGC fast decay current. 0 = Fast decay current always on 1 = Normal fast decay operation

Control Register CB:

0	DW	This bit enables the direct write (Bypass ENDEC) function. 0 = Normal operation 1 = Bypass encoder, NRZ0 directly to WD/$\overline{\text{WD}}$
1	GS	This bit enables the phase detector gain switching in read mode. 0 = Normal operation 1 = Gain shift after 14 x 3T (read mode only)
2	RDI	This bit enables the $\overline{\text{RDIO}}$ pin as an input 0 = $\overline{\text{RDIO}}$ is an output 1 = $\overline{\text{RDIO}}$ is an input
3	EPDD	Enable Phase Detector (Data Separator): This bit disables the output of the phase detector to the VCO. An external voltage applied across the DFLT pins drives the VCO to a fixed frequency. 1 = Phase detector active 0 = Phase detector charge pump disabled

Control Register CB: (continued)

BIT	NAME	FUNCTION
4	UD	Enable Pump Up Current (Data Separator): This bit enables a test mode for checking the charge pump output current. The charge pump will source a fixed DC current from DFLT and sink the current at $\overline{DFLT}$. 0 = No current 1 = Maximum charge pump current
5	DD	Enable Pump Down Current (Data Separator): This bit enables a test mode for checking the charge pump output current. The charge pump will source a fixed DC current from $\overline{DFLT}$ and sink the current at DFLT. 0 = No current 1 = Maximum charge pump current
6	MTPE	This bit enables the multiplexed test points (MTP1, 2, 4) 0 = Test points disabled 1 = Test points enabled
7	–	Not used, must be programmed to 0.

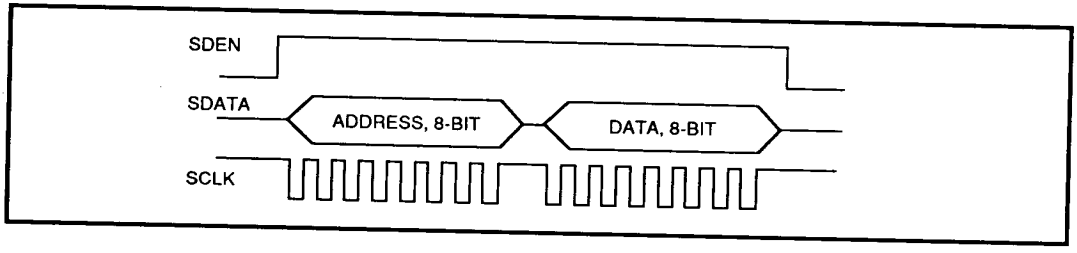


FIGURE 13(a): Serial Port Data Transfer Format

PIN DESCRIPTION

POWER SUPPLY PINS

NAME	TYPE	DESCRIPTION
VPA	-	Data separator PLL analog power supply pin.
VPB	-	Time base generator PLL analog power supply pin.
VPC	-	Internal ECL, CMOS logic power supply pin.
VPD	-	TTL buffer I/O digital power supply pin.
VPG	-	Pulse detector, filter, servo analog power supply pin.
VNA	-	Data separator PLL analog ground pin.
VNB	-	Time base generator PLL analog ground pin.
VNC	-	Internal ECL, CMOS logic ground pin.
VND	-	TTL buffer I/O digital ground pin.
VNG	-	Pulse detector, filter, servo analog ground pin.

INPUT PINS

VIA, $\overline{\text{VIA}}$	I	AGC AMPLIFIER INPUTS: Differential AGC amplifier input pins.
DP, DN	I	ANALOG INPUTS FOR DATA PATH: Differential analog inputs to data comparators, full-wave rectifier.
CP, CN	I	ANALOG INPUTS FOR CLOCK PATH: Differential analog inputs to the clock comparator.
$\overline{\text{PWRON}}$	I	Power Enable: CMOS compatible power control input. A low level CMOS input enables power to circuitry according to the contents of the PDCR. A high level CMOS input shuts down all circuitry.
$\overline{\text{HOLD}}$	I	HOLD CONTROL: TTL compatible control pin which, when pulled low, disables the AGC charge pump and holds the AGC amplifier gain at its present value.
STROBE	I	BURST STROBE: TTL compatible burst strobe input. A high level TTL input will enable the servo peak detector to charge one of the burst capacitors. The falling edge of STROBE increments an internal counter that determines which burst capacitor will charge on the next STROBE pulse (reference Figure 3 for timing.)
$\overline{\text{RESET}}$	I	RESET CONTROL INPUT: TTL compatible reset input. A low level TTL input will discharge the internal servo burst hold capacitors on channels A-D.
IN, $\overline{\text{IN}}$	I	FILTER SIGNAL INPUTS: The AGC output signals must be AC coupled into these pins.
FREF	I	REFERENCE FREQUENCY INPUT: Frequency reference input for the time base generator. FREF may be driven either by a direct coupled TTL signal or by an ac coupled ECL signal. Pin FREF has an internal pull down resistor.

INPUT PINS (continued)

NAME	TYPE	DESCRIPTION
AMENB	I	ADDRESS MARK ENABLE: TTL compatible input. A high level TTL input will enable the address mark generation circuitry in write mode and the address mark detect circuitry in read mode.
NRZIN	I	NRZ INPUT: TTL compatible write data NRZ input. This pin can be connected to the NRZO pin to form a bidirectional data port. Pin NRZIN has an internal pull up resistor.
RG	I	READ GATE: TTL compatible read gate input. A high level TTL input selects the RD input and enables the read mode/address mark detect sequences. A low level selects the FREF input. See Table 5.
SG	I	SERVO GATE: TTL compatible servo gate input. A high level TTL input activates the servo mode by selecting the servo control registers, the RDIO pin, and the RTS resistor.
WCLK	I	WRITE CLOCK: TTL compatible write clock input. Must be synchronous with the Write Data NRZ input. For short cable delays, WCLK may be connected directly to pin RRC. For long cable delays, WCLK should be connected to an RRC return line matched to the NRZ data bus line delay.
WG	I	WRITE GATE: TTL compatible write gate input. A high level TTL input enables the write mode. See Table 5.

OUTPUT PINS

$\overline{\text{AMD}}$	O	ADDRESS MARK DETECT: Address mark detect CMOS compatible output. Tristate output pin that is high impedance state when RG is low. When AMENB is high, this output indicates address mark search status. A low level output appears when an address mark has been detected. A low level on the AMENB pin resets $\overline{\text{AMD}}$.
MTP1,2,3	O	MULTIPLEXED TEST POINTS: Open emitter ECL output test points. Internal test signals are routed to these test points as determined by the CAR and CBR. Two external resistors are required to use this pin. They should be removed during normal operation to reduce power dissipation. See Table 7.
NRZO	O	NRZ OUTPUT DATA: NRZ data CMOS compatible output. Tristate output pin that is in its high impedance state when RG is low. Read data output when RG is high.
OD, $\overline{\text{OD}}$	O	DIFFERENTIAL DIFFERENTIATED OUTPUTS: Filter differentiated outputs. These outputs are AC coupled into the CP/CN inputs.
ON, $\overline{\text{ON}}$	O	DIFFERENTIAL NORMAL OUTPUTS: Filter normal low pass output signals. These outputs are AC coupled into the DP/DN inputs.
PPOL	O	PULSE POLARITY: Pulse polarity CMOS compatible output. The output is high when the pulse being qualified is positive and it is low when the pulse being qualified is negative.

PIN DESCRIPTION (continued)

INPUT PINS (continued)

NAME	TYPE	DESCRIPTION
$\overline{RDIO}$	O	READ DATA I/O: Bi-directional CMOS pin. $\overline{RDIO}$ is an output when the SG is active or the RDI bit is low in the CBR. $\overline{RDIO}$ is an input when the RDIO bit is high in the CBR. The SG overrides the bit in the CBR. $\overline{RDIO}$ is high impedance when SG is low and RG or WG is high.
RRC	O	READ REFERENCE CLOCK: Read clock CMOS compatible output. During a mode change, no glitches are generated and no more than one lost clock pulse will occur. When RG goes high, RRC initially remains synchronized to FOUT. When the Sync Bits are detected, RRC is synchronized to the $\overline{DRD}$. When RG goes low, RCC is synchronized back to the FOUT.
VOA, $\overline{VOA}$	O	AGC AMPLIFIER OUTPUT: Differential AGC amplifier output pins. These outputs are ac coupled into the filter inputs (IN/$\overline{IN}$).
$\overline{WD}$	O	WRITE DATA: Encoded write data CMOS compatible output. The data is automatically resynchronized (independent of the delay between RRC and WCLK) to the FREF reference clock. When direct write is active $\overline{WD}$ is NRZIN data.

ANALOG PINS

A, B, C, D	-	SERVO OUTPUTS: These outputs are processed versions of the voltages captured on the servo hold capacitors. They are referenced to SREF.
BYP	-	The AGC integrating capacitor CBYP, is connected between BYP and VPG.
TFLT/$\overline{TFLT}$	-	PLL LOOP FILTER: These pins are the connection points for the time base generator loop filter.
DACOUT	-	DAC VOLTAGE TEST POINT: This test point monitors the outputs of the internal DACs. The source DAC is selected by programming the two MSBs of the WSCR register: TDAC1 TDAC0 DAC MONITORED 0 0 Filter *fc* DAC 0 1 Qualifier threshold DAC (VTH) 1 0 Window shift DAC 1 1 Write precomp DAC
DFLT/$\overline{DFLT}$	-	PLL LOOP FILTER: These pins are the connection points for the data separator loop filter.
LEVEL	-	An NPN emitter output that provides a full-wave rectified signal from the DP, DN inputs. An external capacitor should be connected from LEVEL to VPG to set the hysteresis threshold time constant in conjunction with RTS and RTD. An internal current source provides 50 µA of pull-down current at this pin.
RR	-	REFERENCE RESISTOR INPUT: An external 1% resistor is connected from this pin to ground to establish a precise internal reference current for the data separator and time base generator.

INPUT PINS (continued)

NAME	TYPE	DESCRIPTION
RTS	-	SERVO TIME CONSTANT RESISTOR INPUT: An external resistor is connected from this pin to LEVEL to establish the hysteresis threshold time constant when in Servo mode.
RTD	-	DATA TIME CONSTANT RESISTOR INPUT: An external resistor is connected from this pin to LEVEL to establish the hysteresis threshold time constant when not in Servo mode.
RX	-	REFERENCE RESISTOR INPUT: An external 1% resistor is connected from this pin to VNG to establish a precise PTAT (proportional to absolute temperature) reference current for the filter.
MAXREF	-	SERVO REFERENCE: An external voltage output that can be used as the reference for an external A/D converter This represents the maximum output voltage for the A, B, C, and D outputs.

SERIAL PORT PINS

SDEN	-	SERIAL DATA ENABLE: Serial enable CMOS compatible input. A high level input enables the serial port.
SDATA	-	SERIAL DATA: Serial data CMOS compatible input. NRZ programming data for the internal registers is applied to this input.
SCLK	-	SERIAL CLOCK: Serial clock CMOS compatible input. The clock applied to this pin is synchronized with the data applied to SDATA.

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, the recommended operating conditions are as follows: 4.5V < POSITIVE SUPPLY VOLTAGE < 5.5V, 0°C < T (ambient) < 70°C, and 25°C < T(junction) < 135°C. Currents flowing into the chip are positive. Current maximums are currents with the highest absolute value.

ABSOLUTE MAXIMUM RATINGS

Operation beyond the maximum ratings may damage the device

PARAMETER	RATING
Storage Temperature	-65 to 150°C
Junction Operating Temperature	+135°C
Positive Supply Voltage (Vp)	-0.5 to 7V
Voltage Applied to any pin	-0.5V to Vp + 0.5V

POWER SUPPLY CURRENT AND POWER DISSIPATION

PARAMETER	CONDITIONS		MIN	NOM	MAX	UNIT
ICC (VPA, VPB, VPC, VPD, VPG)	Outputs and test point pins open	(32P4731) @ 24 Mb/s)		80		mA
	Ta = 27°C Vpn = 5.0 V	(32P4741) @ 40 Mb/s		100		mA
PWR Power Dissipation	Outputs and test point pins open,	(32P4731) @ 24 Mb/s		400		mW
	Ta = 27°C Vpn = 5.0 V	(32P4731) @ 40 Mb/s		500		mW
Sleep Mode Power	$\overline{PWRON}$ = 1				1	mW
Servo Mode Power	$\overline{PWRON}$ = 0 TBG Disabled Data Separator Disabled			200		mW

DIGITAL INPUTS AND OUTPUTS

TTL Compatible Inputs

Input low voltage	VIL		-0.3		0.8	V
Input high voltage	VIH		2.0		VPD+0.3	V
Input low current	IIL	VIL=0.4V			-100	µA
Input high current	IIH	VIH = 2.4V			50	µA

CMOS Compatible Inputs - Schmitt trigger type, do not leave open. Nominal 1.0 V hysteresis around VPD/2.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Input low voltage		-0.3		1.5	V
Input high voltage		3.5		VPD+0.3	

CMOS Compatible Outputs

Output low voltage	5.0 V, 25 °C IOL = 4.07 mA			0.5	V
Output high voltage	5.0 V, 25 °C IOH = -4.83 mA	4.5			V
Rise time	4.5V, 70 °C, C =15 pF, 0.8 to 2.0V			3.0	ns
Fall time	4.5V, 70 °C, C = 15 pF, 0.8 to 2.0V			4.0	ns

Test Point Output Levels (MTP1, MTP2, MTP3)

Output high level	261Ω to VPA 402Ω to AGND VPA = 5.0V	VPA-1.02			V
Output low level	261Ω to VPA 402Ω to AGND VPA = 5.0V			VPA-1.62	V

Serial Port

SCLK period	T_{CKL}	R/W Bit = 0 (Write)	100			ns
		R/W Bit = 1 (Read)	140			ns
SCLK low time,	T_{CKL}	R/W Bit = 0 (Write)	40			ns
		R/W Bit = 1 (Read)	60			ns
SCLK high time,	T_{CKH}	R/W Bit = 0 (Write)	40			ns
		R/W Bit = 1 (Read)	60			ns
Enable to SCLK	T_{SENS}		35			ns
SCLK to disable	T_{SENH}		100			ns
Data set-up time	T_{DS}		15			ns
Data hold time	T_{DH}		15			ns
SDATA tri-state delay	T_{SENDL}				50	ns
SDATA turnaround time	T_{TRN}	R/W Bit = 1 (Read)	70			ns
SDEN low time	T_{SL}		200			ns
SCLK to Valid Data	T_{SKEW}	R/W Bit = 1 (Read)			50	ns

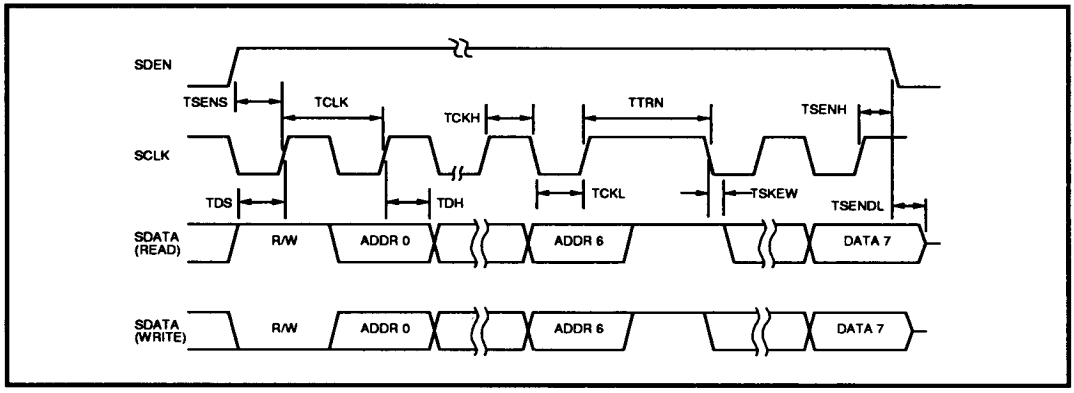


FIGURE 13(b): Serial Port Timing Information

ELECTRICAL SPECIFICATIONS (continued)

PULSE DETECTOR CHARACTERISTICS

AGC Amplifier

Input signals are AC coupled to VIA/$\overline{\text{VIA}}$, VOA/$\overline{\text{VOA}}$ outputs are AC coupled toIN/$\overline{\text{IN}}$, and ON/$\overline{\text{ON}}$ are AC coupled to DP/DN. A 1000 pF capacitor (CBYP) is connected from BYP to VPG. Unless otherwise specified, outputs are measured differentially at VOA/$\overline{\text{VOA}}$, FIN = 4 MHz, and filter boost = 0 dB.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Input range	Filter boost = 0 dB	22		240	mVpp
	Filter boost = 11 dB	20		100	mVpp
DP-DN voltage	VIA-$\overline{\text{VIA}}$ = 0.1 Vpp	0.90		1.10	Vpp
DP-DN voltage variation	22 mV < VIA-$\overline{\text{VIA}}$ < 240 mV			5	%
Gain range		1.9		22	V/V
Gain sensitivity	BYP voltage change		28		dB/V
VOA-$\overline{\text{VOA}}$ dynamic range	THD = 1% max	0.75			Vpp
Differential input impedance	WG = low	4.7	6.0	8.4	kΩ
	WG = high; or Low-Z		350		Ω
Single-ended input impedance	WG = low		3.5		kΩ
	WG = high; or Low-Z		250		Ω
Output offset voltage variation	Gain = 1.9 to 22			+200	mV
Input noise voltage	Gain = 22, VIA/$\overline{\text{VIA}}$ shorted		10	15	nV/√Hz
Bandwidth	Gain = 22	50			MHz
CMRR	Gain = 22, fc = 5MHz	40			dB

AGC Amplifier (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
PSRR	Gain = 22, fc = 5MHz	45			dB
Single-ended output resistance		150		Ω	
Gain decay time	VIA-$\overline{\text{VIA}}$ = 240 to 120 mV VOA-$\overline{\text{VOA}}$ > 0.9 Final Value		50		µs
Gain attack time	VIA-$\overline{\text{VIA}}$ = 120 to 240 mV VOA-$\overline{\text{VOA}}$ < 1.1 Final Value		1		µs

5

AGC Control
The input signals are AC coupled into DN/DP, CBYP = 1000 pF to VPG. CT = 10000 pF, RTS = RTD = Open.

DP-DN input range	For test only		1.0	1.5	Vpp
Decay current	Normal decay (I_D)		4.0		µA
	Fast decay mode (I_{DF})		1		mA
Attack current	Normal attack (I_{CH})		0.18		mA
	Fast attack mode (I_{CHF})		8 x ICH		mA
BYP leakage current	WG = high	-10		10	nA
Low-Z duration			1.0		µs
Fast decay duration			1.0		µs
LEVEL output gain	|DP-DN| = 0.5 to 1.5V	0.65	0.70	0.75	V/Vpp
LEVEL output bandwidth	-1dB	10			MHz
LEVEL offset voltage	Output - V_{RTS} or V_{RTD}, I_L = 50 µA			30	mV
Internal LEVEL pull-down current		40	50	60	µA

Data Comparator
The input signals are AC coupled into DP/DN.

DP-DN input range		0.5	1.0	1.5	Vpp
Differential input resistance	WG = low	7.0		13.0	kΩ
Single ended input resistance	WG = high		500		Ω
Threshold voltage hysteresis			.2XT%		%
Threshold (T%) accuracy	30% ≤ T% ≤ 80% 0.3 < Level - V_{RTH} < 0.75 T% = V_{THDAC} • 0.93/127	T%-5	T%	T%+5	%
Minimum threshold voltage	LEVEL-VRC < 0.1V V_{THMIN} = $V_{\overline{THDAC}}$ 97.6%/127		V_{THMIN}		V

ELECTRICAL SPECIFICATIONS (continued)

Clock Section
The input signals are AC coupled into CP/CN.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Comparator offset voltage		-4.0		4.0	mV
Differential input resistance		7.0		13.0	kΩ
Pulse pairing	Sine wave into DP/DN Phase shift 90° into CP/CN V_{SINE} = 1 Vpp, F_{SINE} = 4 MHz			0.5	ns

SERVO CAPTURE CHARACTERISTICS

MAXREF output voltage	I_{SOURCE} = 0 mA	2.85	3.00	3.15	V
MAXREF load regulation	I_{SOURCE} = 0 to 4.5 mA			20	mV
A, B, C, D output low voltage	I_{SINK} = 0.2 mA $\overline{RESET}$ = 0V (low)	0.47	0.50	0.53	V
A, B, C, D output clip level	I_{SOURCE} = 0.2 mA	VPG-1.2			V
MAXREF-A,B,C,D high voltage	22 mVpp ≤ VIA-$\overline{VIA}$ ≤ 240 mVpp AGC loop closed	0			V
A, B, C, D output impedance	$I_{SOURCE/SINK}$ = 0.2 mA			50	Ω
A, B, C, D gain	From DP/DN pins	2.20	2.25	2.30	V/V
Peak detector hold droop	STROBE = 0 V	-1	0	+1	mV/µs
Channel to channel amplitude mismatch	DP-DN = 1.0 Vpp Sinewave at 4 MHz	-15		15	mV
Peak detector acquisition to 99%	DP-DN = 1.0 Vpp sinewave Fs ≤ 6.7 MHz, DACP = 1000			800	ns
Peak detector reset time to 1%	$\overline{RESET}$ = 0 DACP = 1000			300	ns
$\overline{RESET}$ turn-on delay	From $\overline{RESET}$ fall @ 1.2V			50	ns
$\overline{RESET}$ turn-off delay	From $\overline{RESET}$ rise @ 1.2V			50	ns
$\overline{RDIO}$ pulse width	C_L = 15 pF 32P4741	10		15	ns
	32P4731	23		47	ns
$\overline{RDIO}$ turn-on delay	From WG or RG↓			150	ns
$\overline{RDIO}$ turn-off delay	From WG or RG↑			150	ns

PROGRAMMABLE FILTER CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Filter cutoff range 32P4731	*fc* @ 3 dB point *fc* = (0.0708 MHz) x DACF, Boost = 0 dB	3		9	MHz
32P4741	*fc* = (0.1417 MHz) x DACF, Boost = 0 dB 32 ≤ DACF ≤ 127	6		18	MHz
Filter cutoff accuracy	DACF = 127	-10		10	%
ON differential gain (AN)	F = 0.67 x *fc*, boost = 0 dB	1.6	2.0	2.4	V/V
OD differential gain (AD)	F = 0.67 x *fc*, boost = 0 dB	0.9AN		1.1AN	V/V
Frequency boost @ *fc*	DACS = 127		13		dB
Boost accuracy	@ 6 dB, DACS = 37	-0.75		+0.75	dB
	@ 9 dB, DACS = 67	-1.0		+1.0	dB
	@ 13 db, DACS = 127	-1.5		+1.5	dB
Group delay variation Boost = 0 dB to 13 dB	*fc* = 9 MHz FIN = 0.2 *fc* to *fc*	-1.25		1.25	ns
32P4731	3 ≤ Fc < 9 MHz FIN = 0.2 *fc* to *fc*	-2		+2	%
	3 ≤ *fc* < 9 MHz FIN = *fc* to 1.75 *fc*	-3		+3	%
Group delay variation Boost = 0 dB to 13 dB	*fc* = 18 MHz FIN = 0.2 *fc* to *fc*	-750		750	ps
32P4741	6 ≤ Fc < 18 MHz FIN = 0.2 *fc* to *fc*	-2		+2	%
	6 ≤ *fc* < 18 MHz FIN = *fc* to 1.75 *fc*	-3		+3	%
Filter differential input dynamic range	THD = 1%, F = 0.67 *fc* boost = 0 dB	0.5			Vpp
Filter differential output dynamic range	THD = 1%, F = 0.67 *fc* boost = 0 dB	1.0			Vpp
Filter differential input resistance	Normal	5.0			kΩ
	Low-Z		300		Ω
Filter differential input capacitance				7.0	pF
Output noise voltage	BW = 100 MHz, Rs = 50Ω				

ELECTRICAL SPECIFICATIONS (continued)

PROGRAMMABLE FILTER CHARACTERISTICS (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
32P4731: differentiated output	fc = 9 MHz, boost = 0 dB		2.6		mVRms
differentiated output	fc = 9 MHz, boost = 13 dB		5.6		mVRms
normal output	fc = 9 MHz, boost = 0 dB		2.0		mVRms
normal output	fc = 9 MHz, boost = 13 dB		3.6		mVRms
32P4741: differentiated output	fc =18 MHz, boost = 0 dB		3.8		mVRms
differentiated output	fc =18 MHz, boost = 13 dB		6.9		mVRms
normal output	fc =18 MHz, boost = 0 dB		2.1		mVRms
normal output	fc =18 MHz, boost = 13 dB		4.2		mVRms
Filter output sink current			0.5		mA
Filter output source current		2.0			mA
Filter output resistance	single ended			200	Ω
Rx pin voltage	Ta = 27°C		600		mV
	Tj = 127°C		800		mV
Rx resistance	1% fixed value		12.1		kΩ

TIME BASE GENERATOR CHARACTERISTICS

FREF input range		8		20	MHz
FOUT frequency range				75	MHz
FOUT jitter	TOUT = 1/FOUT	-200		+200	psRMS
	FOUT ≤ 75 MHz				
M counter range		2		255	
N counter range		2		127	
VCO center frequency period (TVCO)	FVCO=[12.5/(RR+0.4)] x [(0.622 x IDAC) + 4.27] (MHz) -1.5V ≤ TFLT-$\overline{\text{TFLT}}$ ≤ +1.5V	0.90T0		1.10T0	ns
VCO dynamic range	-1.5V ≤ TFLT-$\overline{\text{TFLT}}$ ≤ +1.5V FOUT = 54 MHz	±25		±45	%
VCO control gain KVCO	ωi = 2π/TVCO -1.5V ≤ TFLT-$\overline{\text{TFLT}}$ ≤ + 1.5V	0.14 ωi	0.175 ωi	0.26 ωi	rad/ (V-S)
Phase detector gain KD	KD = [12.5/(RR + 0.4)] x (0.6768 x IDAC + 3.4789) x 10^{-6}	0.83KD		1.17KD	A/rad

TIME BASE GENERATOR CHARACTERISTICS (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
KVCO x KD product accuracy		-28		+28	%
FREF input low time		20			ns
FREF input high time		20			ns

DATA SEPARATOR CHARACTERISTICS: Unless otherwise noted, RR = 12.1 kΩ

Read Mode

Read clock rise time TRRC	0.8 to 2.0V CL ≤ 15 pF			5	ns
Read clock fall time TFRC	2.0 to 0.8V CL ≤ 15 pF			5	ns
RRC duty cycle		40		60	%
NRZ out set-up and hold time (TNS, TNH)		8			ns
NRZ out propagation delay (TPNRZ)				±15	ns
$\overline{AMD}$ set-up and hold time (TAS, TAH)		13.0			ns
$\overline{AMD}$ propagation delay (TPAMD)				±15	ns
1/3 cell delay	TVCO = 1/[0.622 x IDAC) + 4.27]	0.8TD		1.2TD	ns

Write Mode

Write data pulse width (TWD) 32P4731	1.5V, CL ≤ 5 pF	2TVCO/3 -0-5		2TVCO/3 +0-5	ns
32P4741		TVCO+ 0.5		TVCO+ 0.5	ns
Write data rise time (TRWD)	0.8 to 2.0 V CL ≤ 15 pF			5	ns
Write data fall time (TFWD)	2.0 to 0.8 V CL ≤ 15 pF			5	ns
Write data clock rise time (TRWC)	0.8 to 2.0 V CL ≤ 15 pF			10	ns
Write data clock fall time (TFWC)	2.0 to 0.8 V CL ≤ 15 pF			8	ns
NRZ set-up time (TSNRZ)		5			ns
NRZ hold time (THNRZ)		5			ns

ELECTRICAL SPECIFICATIONS (continued)

Data Synchronization

PARAMETER	CONDITIONS		MIN	NOM	MAX	UNIT
Loop filter = TBD						
VCO center frequency period (TVCO)	FVCO=(0.622 x IDAC) + 4.27 (MHz) -1.5V≤ DFLT-$\overline{\text{DFLT}}$ ≤ +1.5V		0.90T0		1.10T0	ns
VCO dynamic range	-1.5V ≤ DFLT-$\overline{\text{DFLT}}$ ≤ +1.5V		±25		±45	%
VCO control gain KVCO	ωi = 2π/TVCO (32P4741) ωi = π/TVCO (32P4731) -1.5V ≤ DFLT-$\overline{\text{DFLT}}$ ≤ +1.5V		0.14 ωi	0.175 ωi	0.26 ωi	rad/(V-S)
Phase detector gain, KD	PLL ref = FOUT		0.83KD		1.17KD	μA/rad
	Idle mode = 1 x KD Read mode = 3 x KD Read mode after gain shift = 1 x KD KD = [12.5/(RR + 0.4)] x (0.6768 x IDAC + 3.4789) x 10^{-6}		0.83KD		1.17KD	A/rad
KVCO x KD product accuracy			-28		+28	%
VCO phase restart error			-2		+2	ns
Decode window center accuracy		32P4731	-1.5		+1.5	ns
		32P4741	-0.75		+0.75	ns
Decode window width		32P4731	(2TVCO/3)-1.5			ns
		32P4741	TVCO-0.75			ns

Window Shift Control

Window shift magnitude is set by the value in the Window Shift (WS) register. The WS register bits are as follows:

BIT	NAME	FUNCTION
0	$\overline{WSO}$	
1	$\overline{WS1}$	
2	$\overline{WS2}$	
3	$\overline{WS3}$	
4	WSD	Window shift direction. 0=early, 1=late
5	WSE	Window shift enable
6	TDAC0	Used to route signals to DAC test point
7	TDAC1	Used to route signals to DAC test point

The window shift magnitude is set as a percentage of the decode window, in 2% steps. The tolerance of the window shift magnitude is ±15%. Window shift should be set during idle mode or write mode.

$\overline{WS3}$	$\overline{WS2}$	$\overline{WS1}$	$\overline{WS0}$	Shift Magnitude
1	1	1	1	No shift
1	1	1	0	2% (minimum shift)
1	1	0	1	4%
1	1	0	0	6%
1	0	1	1	8%
1	0	1	0	10%
1	0	0	1	12%
1	0	0	0	14%
0	1	1	1	16%
0	1	1	0	18%
0	1	0	1	20%
0	1	0	0	22%
0	0	1	1	24%
0	0	1	0	26%
0	0	0	1	28%
0	0	0	0	30% (maximum shift)

ELECTRICAL SPECIFICATIONS (continued)

WRITE PRECOMP CONTROL

Write precomp magnitude is set by the value in the Write precomp (WP) register. The WP register bits are as follows:

BIT	NAME	FUNCTION
0	$\overline{WE0}$	Early Precomp Magnitude
1	$\overline{WE1}$	Early Precomp Magnitude
2	$\overline{WE2}$	Early Precomp Magnitude
3	WPE	Write Precomp enable, 0 = Disable 1 = Enable
4	$\overline{WL0}$	Late Precomp Magnitude
5	$\overline{WL1}$	Late Precomp Magnitude
6	$\overline{WL2}$	Late Precomp Magnitude
7	–	Not used

The write precomp magnitude is calculated as:

TPC = a x 0.04 x Tvco (32P4731)
TPC = a x 0.02 x Tvco (32P4741)

where a = precomp magnitude scaling factor as shown below. TREF is the period of the reference frequency provided by the internal time base generator.

$\overline{Wn2}$	$\overline{Wn1}$	$\overline{Wn0}$	Precomp Magnitude Scaling Factor
1	1	1	No precomp
1	1	0	1X
1	0	1	2X
1	0	0	3X
0	1	1	4X
0	1	0	5X
0	0	1	6X
0	0	0	7X (maximum)

BIT N-2	BIT N-1	BIT N	BIT N+1	BIT N+2	BIT N COMPENSATION
1	0	1	0	1	None
0	0	1	0	0	None
1	0	1	0	0	Early
0	0	1	0	1	Late

Late = Bit N is time shifted toward the N+1 bit by the programmed magnitude
Early = Bit N is time shifted toward the N-1 bit by the programmed magnitude

TABLE 4: 1,7 RLL Encode Table

NRZ DATA				ENCODED WRITE DATA			
Present		Next		Previous	Present		
D_1	D_2	D_1^*	D_2^*	Y_3'	Y_1	Y_2^*	Y_3^*
0	0	0		1	0	0	1
0	0	1		0	0	0	0
0	0	1		1	0	1	0
1	0	0			1	0	1
1	0	1			0	1	0
0	1	0	0	0	0	0	1
0	1	0	0	1	0	1	0
0	1	1	0		0	0	0
0	1	0	1	0	0	0	1
0	1	0	1	1	0	0	0
0	1	1	1		0	0	0
1	1	0	0	0	0	1	0
1	1	1	0	0	1	0	0
1	1	0	1	0	1	0	0
1	1	1	1	0	1	0	0

TABLE 5: 1,7 RLL Decode Table

ENCODED READ DATA						DECODED DATA	
Previous		Present			Next		
Y_2'	Y_3'	Y_1	Y_2	Y_3	Y_2^* Y_3^*	D_1	D_2
0	0	0	0	0		0	1
1	0	0	0	0		0	0
0	1	0	0	0		0	1
		1	0	0		1	1
	0	0	1	0	0 0	1	1
	0	0	1	0	1 0	1	0
	0	0	1	0	0 1	1	0
	1	0	1	0	0 0	0	1
	1	0	1	0	1 0	0	0
	1	0	1	0	0 1	0	0
0	0	0	0	1		0	1
1	0	0	0	1		0	0
0	1	0	0	1		0	0
		1	0	1		1	0

ELECTRICAL SPECIFICATIONS (continued)

TABLE 6A: 32P4731 Clock Source and Frequency vs. Mode

WG	VCO RG	REF	DECODE RCLK	ENCODE CLOCK	CLOCK	MODE
0	0	FOUT/2	FOUT/3	FOUT/2	FOUT/2	IDLE
0	1	$\overline{DRD}$	VCO/3	VCO/2	FOUT/2	READ
1	0	FOUT/2	FOUT/3	FOUT/2	FOUT/2	WRITE

NOTE 1: Until the VCO locks to the new source, the VCO/2 entries will be FOUT/2.
NOTE 2: Until the VCO locks to the new source, the VCO/3 entries will be FOUT/3.
NOTE 3: WG = RG = 1 is an indeterminate state.

TABLE 6B: 32P4741 Clock Source and Frequency vs. Mode

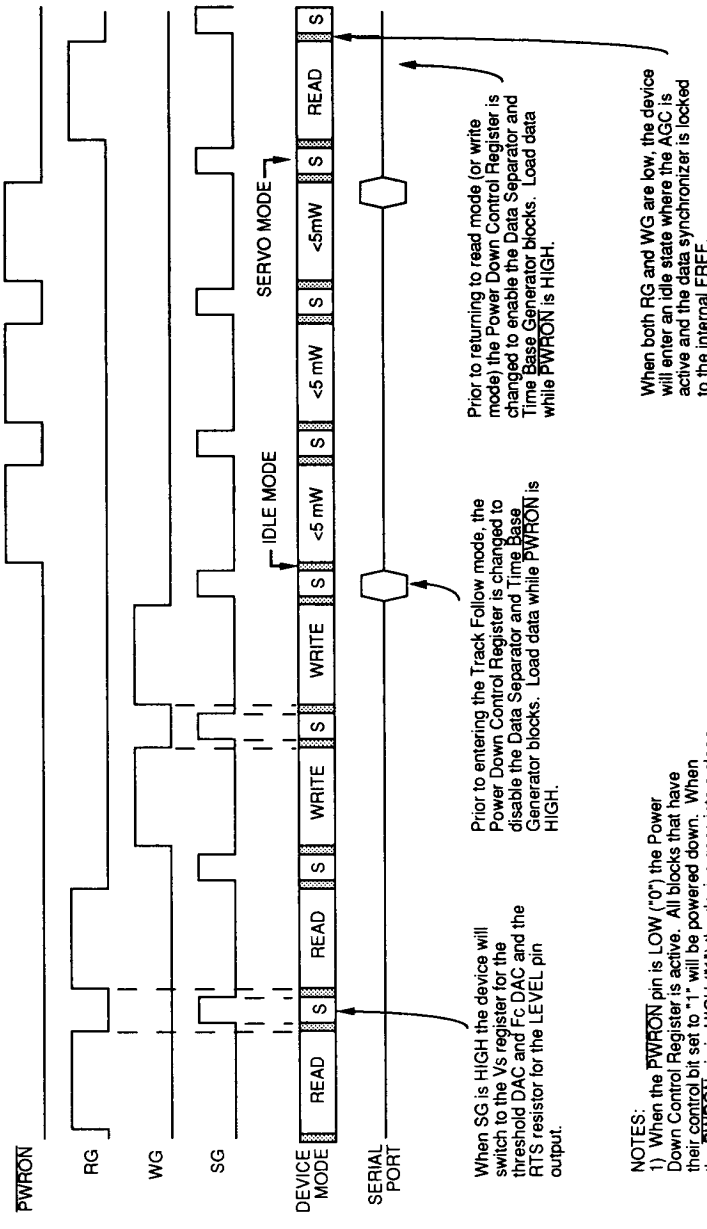
WG	RG	VCO REF	RCLK	DECODE CLOCK	ENCODE CLOCK	MODE
0	0	FOUT	2FOUT/3	FOUT	FOUT	IDLE
0	1	$\overline{DRD}$	2VCO/3	VCO	FOUT	READ
1	0	FOUT	2FOUT/3	FOUT	FOUT	WRITE

NOTE 1: Until the VCO locks to the new source, the VCO/2 entries will be FOUT.
NOTE 2: Until the VCO locks to the new source, the 2VCO/3 entries will be 2FOUT/3.
NOTE 3: WG = RG = 1 is an indeterminate state.

TABLE 7: Multiplexed Test Point Signal Selection

MTPE	TMS1	TMS0	MTP1	MTP2	MTP3
0	X	X	OFF	OFF	OFF
1	0	0	VCOREF	DS-IN	DSREF
1	0	1	RD	DOUT	COUT
1	1	0	VCOREF	DS-IN	MCTR
1	1	1	SET	RESET	COUT

COUT = Output of the pulse qualifier clock circuit
DOUT = Output of the pulse qualifier data comparators
DS-IN = Delayed read data output (read mode), Fout/2 (in non-read mode)
DSREF = Output of the time base generator
MCTR = M counter output of the time base generator
RD = Read data output from the pulse qualifier
RESET = Output of the negative threshold comparator
SET = Output of the positive threshold comparator
VCOREF = Data separator VCO reference clock



NOTES:
1) When the PWRON pin is LOW ("0") the Power Down Control Register is active. All blocks that have their control bit set to "1" will be powered down. When the PWRON pin is HIGH ("1") the device goes into a sleep mode with all blocks powered down except the serial port.

2) When the threshold DAC reference is switched, there is a maximum settling time of 1.5µsec for the DAC.

FIGURE 14: Power Control Timing

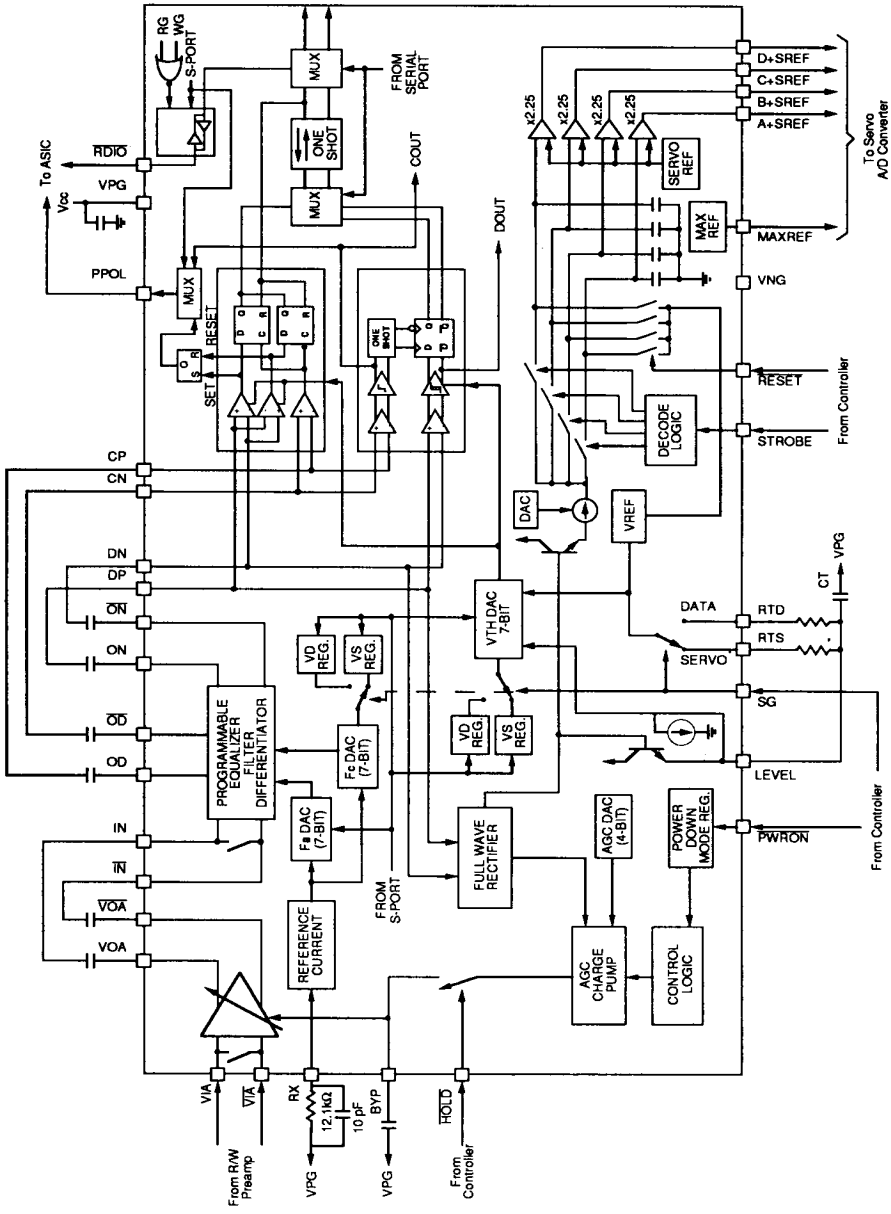


FIGURE 15A: 32P4731/41 Application Diagram

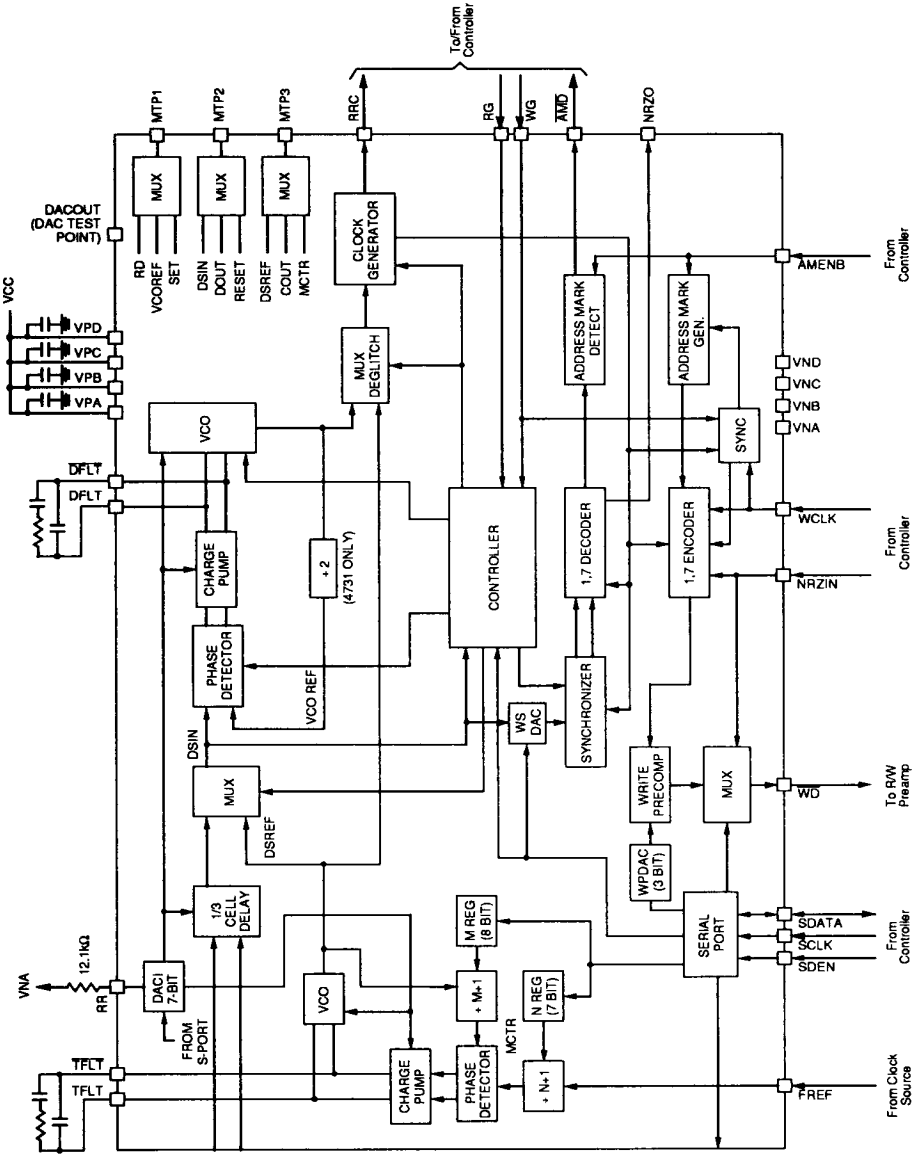
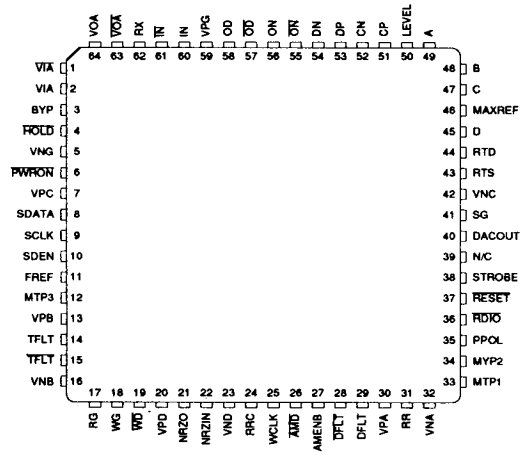


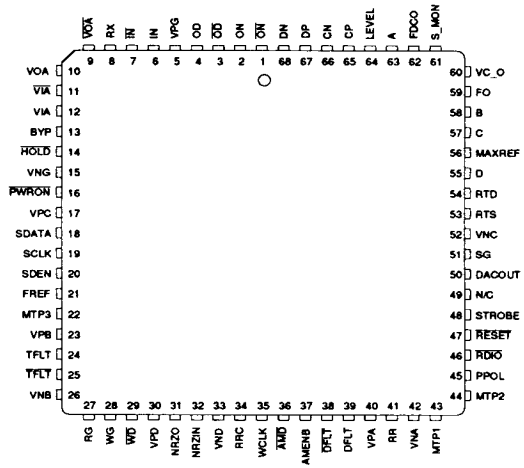
FIGURE 15B: 32P4731/41 Application Diagram

PACKAGE PIN DESIGNATIONS

(Top View)



64-Pin TQFP



68-Pin PLCC

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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