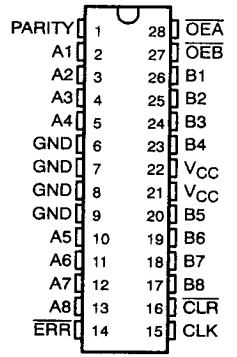
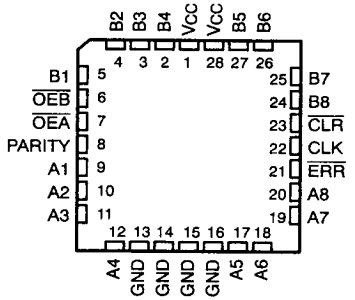
D3448, MARCH 1990–REVISED OCTOBER 1990

- **High-Speed Bus Transceivers With Parity Generator/Checker**
- **Parity-Error-Flag Open-Drain Output**
- **Register for Storage of the Parity-Error Flag**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

54AC11833 . . . JT PACKAGE
74AC11833 . . . DW OR NT PACKAGE
(TOP VIEW)



54AC11833 . . . FK PACKAGE
(TOP VIEW)



description

The 'AC11833 is an 8-bit to 9-bit parity transceiver designed for two-way communication between data buses. When data is transmitted from the A bus to the B bus, a parity bit is generated. When data is transmitted from the B bus to the A bus with its corresponding parity bit, the $\overline{ERR}$ output will indicate whether or not an error in the B data has occurred. The output enable inputs $\overline{OEA}$ and $\overline{OEB}$ can be used to disable the device so that the buses are effectively isolated.

A 9-bit parity generator/checker generates a parity-odd output (PARITY) and monitors the parity of the I/O ports with an open-drain parity error flag ($\overline{ERR}$). $\overline{ERR}$ is clocked into the register on the rising edge of the CLK input. The error flag register is cleared with a low pulse on the $\overline{CLR}$ input. When both $\overline{OEA}$ and $\overline{OEB}$ are low, data is transferred from the A bus to the B bus and inverted parity is generated. Inverted parity is a forced error condition that gives the designer more system diagnostic capability.

The 54AC11833 is characterized for operation over the full military temperature range of – 55°C to 125°C. The 74AC11833 is characterized for operation from – 40°C to 85°C.

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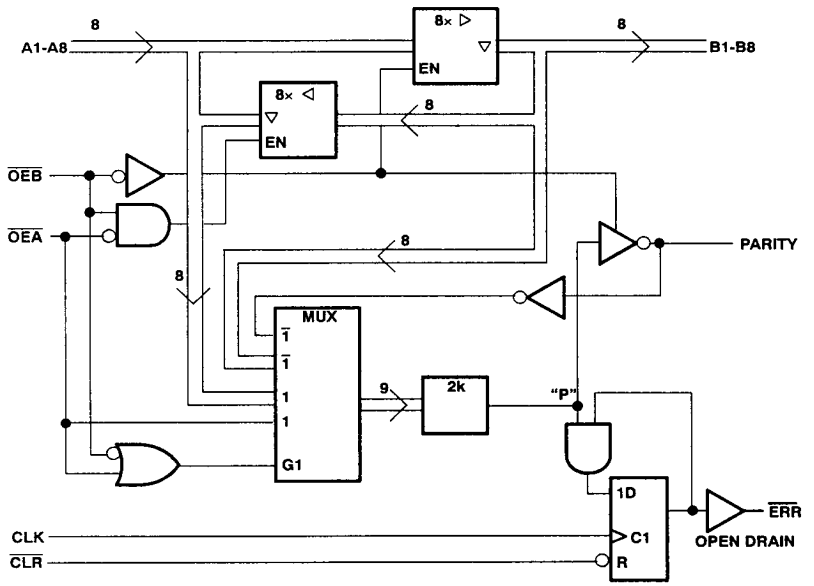
Function Table

INPUTS						OUTPUT AND I/O				FUNCTION
$\overline{OEB}$	$\overline{OEA}$	$\overline{CLR}$	CLK	AI Σ of H's	BI† Σ of H's	A	B	PARITY	$\overline{ERR}$	
L	H	X	X	Odd Even	NA	NA	A	L H	NA	A data to B bus and Generate Parity
H	L	H	↑	NA	Odd Even	B	NA	NA	H L	B Data to A Bus and Check Parity
X	X	L	X	X	X	X	NA	NA	H	Clear Error Flag Register
H	H	H L H H	No↑ No↑ ↑ ↑	X X Odd Even	X	Z	Z	Z	NC H H L	Isolation‡
L	L	X	X	Odd Even	NA	NA	A	H L	NA	A Data to B Bus and Generate Inverted Parity

NA = Not applicable, NC = No change, X = Don't care
† Summation of high-level inputs includes PARITY along with Bi inputs.
‡ In this mode, the $\overline{ERR}$ output, when clocked, shows inverted parity of the A bus.

logic diagram (positive logic)



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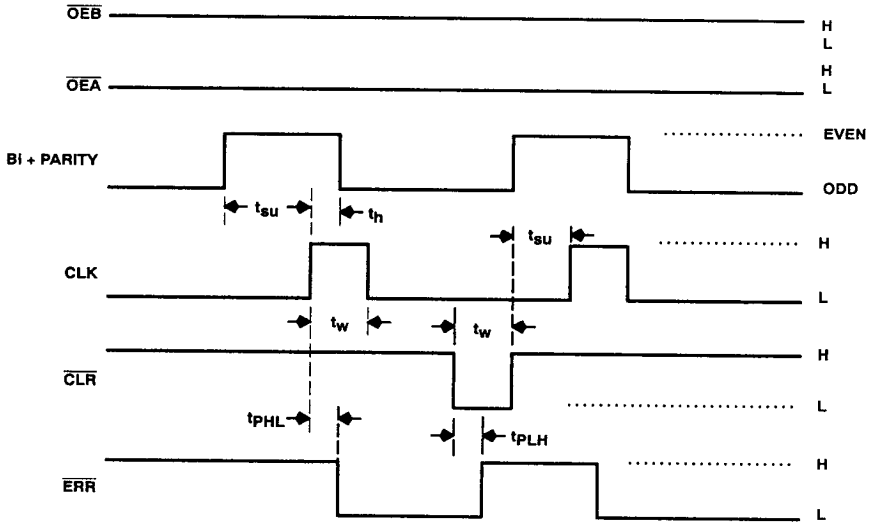
Error-Flag Function Table

INPUTS		INTERNAL TO DEVICE	OUTPUT PRE-STATE	OUTPUT	FUNCTION
$\overline{CLR}$	CLK	POINT "P"	$\overline{ERR}$ n-1	$\overline{ERR}$	
H	↑	H	H	H	Sample
H	↑	X	L	L	
H	↑	L	X	L	
L	X	X	X	H	Clear

$\overline{ERR}$ n-1 represents the state of the $\overline{ERR}$ output before any changes at $\overline{CLR}$, CLK, or point "P".

error-flag waveforms



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) ..... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) ..... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) ..... ±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) ..... ±50 mA
Continuous current through V_{CC} or GND pins ..... ±225 mA
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

			54AC11833			74AC11833			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4			−4	mA
		V_{CC} = 4.5 V			−24			−24	
		V_{CC} = 5.5 V			−24			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			54AC11833		74AC11833		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
I_{OH}	$\overline{ERR}$	$V_O = V_{CC}$	5.5 V			0.5		10		5	µA
V_{OH}	All outputs except $\overline{ERR}$	I_{OH} = – 50 µA	3 V	2.9			2.9		2.9		V
			4.5 V	4.4			4.4		4.4		
			5.5 V	5.4			5.4		5.4		
		I_{OH} = – 4 mA	3 V	2.58			2.4		2.48		
		I_{OH} = – 24 mA	4.5 V	3.94			3.7		3.8		
			5.5 V	4.94			4.7		4.8		
		I_{OH} = – 50 mA†	5.5 V				3.85				
		I_{OH} = – 75 mA†	5.5 V						3.85		
V_{OL}		I_{OL} = 50 µA	3 V			0.1		0.1		0.1	V
			4.5 V			0.1		0.1		0.1	
			5.5 V			0.1		0.1		0.1	
		I_{OL} = 12 mA	3 V			0.36		0.5		0.44	
		I_{OL} = 24 mA	4.5 V			0.36		0.5		0.44	
			5.5 V			0.36		0.5		0.44	
		I_{OL} = 50 mA†	5.5 V					1.65			
		I_{OL} = 75 mA†	5.5 V							1.65	
I_{OZ}	A or B ports, PARITY	$V_O = V_{CC}$ or GND	5.5 V			± 0.5		± 10		± 5	µA
I_I	$\overline{OEA}$, $\overline{OEB}$, CLK, and $\overline{CLR}$	$V_I = V_{CC}$ or GND	5.5 V			± 0.1		± 1		± 1	µA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			8		160		80	µA
C_i	$\overline{OEA}$, $\overline{OEB}$, CLK, and $\overline{CLR}$	$V_I = V_{CC}$ or GND	5 V		4.5						pF
C_{io}	A or B ports, PARITY	$V_O = V_{CC}$ or GND	5 V		12						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Note 2)

			T_A = 25°C		54AC11833		74AC11833		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	CLK high	5		5		5		ns
		CLK low	5		5		5		
		$\overline{CLR}$ low	5		5		5		
t_{su}	Setup time before CLK↑	Bi and PARITY	14		14		14		ns
		$\overline{CLR}$ inactive	2		2		2		
t_h	Hold time after CLK ↑, Bi and PARITY		0		0		0		ns

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

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timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Note 2)

		T_A = 25°C		54AC11833		74AC11833		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w Pulse duration	CLK high	5		5		5		ns
	CLK low	5		5		5		
	$\overline{CLR}$ low	5		5		5		
t_{su} Setup time before CLK↑	Bi and PARITY	14		14		14		ns
	$\overline{CLR}$ inactive	2		2		2		
t_h Hold time after CLK ↑, Bi and PARITY		0		0		0		ns

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS		TYP	UNIT
C_{pd} Power dissipation capacitance per transceiver	Outputs enabled	A to B	C_L = 50 pF,	f = 1 MHz	87	pF
		B to A			60	
	Outputs disabled	A to B	C_L = 50 pF,	f = 1 MHz	28	pF
		B to A			8	

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