040852

ROHM

BR46C15/BR46C16

2K × 8 High Speed CMOS Electrically Erasable PROM

FEATURES

- **2048 x 8 Bit CMOS E²PROM**
- **High Speed Read Access**
  - **— 55 ns**
- **Bipolar PROM Socket Compatibility**
- **Electrically Reprogrammable**
  - **— Program Voltage: 10.8 - 20.5 V**
- **Fast Byte Write: 5 ms**
- **TTL Compatible Inputs and Outputs**
- **Static — No Clocks Required**
- **Low Current Requirements**
  - **— 90mA max. Active**
  - **— 45mA max. Standby**
  - **— 110mA max. Programming**
- **10 Year Data Retention**
- **100% Factory Tested Programmability**
- **PROM Programmer Support Available**
- **Output Current Options:**
  - **–BR46C15; I_{OL} = 6mA**
  - **–BR46C16; I_{OL} = 12mA**

The BR46C15 is a 2K x 8 bit CMOS electrically erasable programmable read only memory (E²PROM) offering unprecedented data access speed. The device is available in both 24-pin DIP and 28-pin SOIC packages.

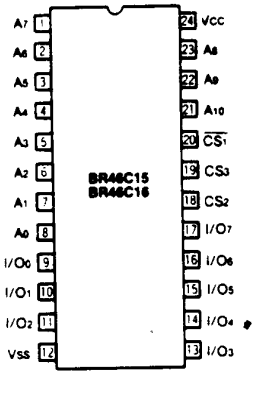
Through the application of revolutionary design techniques this versatile low power device is able to provide data access times competing with those of bipolar PROMs. Complete PROM compatibility is provided in both read and standby modes allowing this E²PROM to replace bipolar PROMs in existing sockets. The key user limitations of bipolar PROM technology, such as one-time programmability and high power requirements, are overcome by the BR46C15. In addition to being an attractive PROM replacement in existing systems, the BR46C15 also opens up a whole new domain of design possibilities.

Unprecedented E²PROM applications are now possible since this CMOS E²PROM combines the advantages of bipolar access speeds, low CMOS power needs and nonvolatile data alterability. Typical applications include high speed process controllers, environmentally adaptive robotics, programmable character generators and user programmable video display pattern generators. ROHM high speed E²PROMs can replace system combinations of high speed static RAM and nonvolatile storage used in read mostly environments.

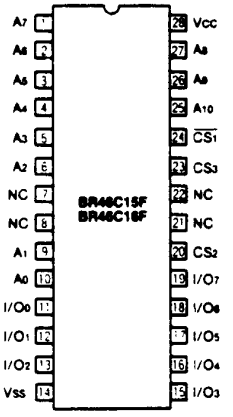
In existing bipolar PROM applications the CMOS BR46C15 reduces active and standby power requirements substantially. The reprogrammable nature of E²PROM technology provides the ideal prototyping tool for PROM applications and allows cost effective in-field code updates without requiring the removal and replacement of one time programmable PROMs.

PIN CONFIGURATION

BR46C15
BR46C16



BR46C15F
BR46C16F



PIN NAMES

A_0-A_{10}	ADDRESS INPUTS
I/O_0-I/O_7	DATA INPUTS/OUTPUTS
$\overline{CS}_1$, CS_2, CS_3	CHIP SELECT INPUTS
V_{CC}	+5V SUPPLY
V_{SS}	GROUND

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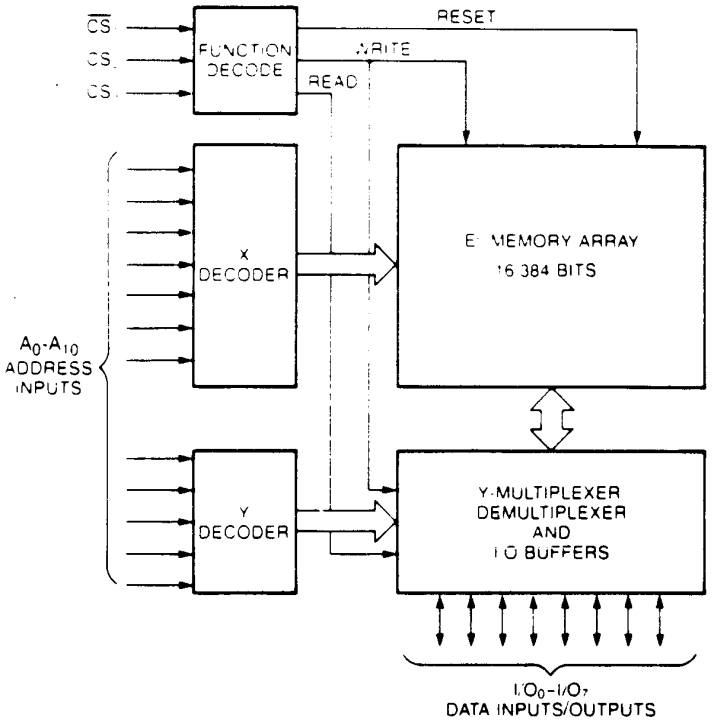
BLOCK DIAGRAM



DEVICE OPERATION

Read

Data is read from the BR46C15 with a bipolar PROM compatible read cycle. This read cycle is initiated by applying a low to $\overline{CS_1}$, a high to CS_2 and a high to CS_3. Data is available within t_{AA} from the time that the address inputs are valid or t_{CS} after the last chip select input is asserted, whichever is later. When any of the chip select control inputs are not asserted, the I/O pins remain in a high impedance state to eliminate system bus contention.

Programming Mode

The BR46C15 uses a complementary cell technique to obtain high speed data access. The complementary cells are programmed in a two stage process. The first stage is a chip reset cycle which brings both halves of every cell in the memory to a high level. This cycle completes in a maximum of 50ms. The second stage is the write cycle during which each byte is individually addressed and written.

Both of these cycles are performed with $\overline{CS_1}$ at V_{PP} (10.8V to 20.5V). This ensures high data integrity when the device is used in a 5V-only PROM socket yet allows easy rewrites when the device is placed in a PROM programmer or supplied with a high voltage signal.

Chip Reset Cycle

The chip reset cycle is executed by applying V_{PP} to $\overline{CS_1}$ and a high (V_{IH}) to CS_2 (see Chip Reset Cycle timing diagram). During the chip reset cycle both halves of each complementary cell in the memory array are set to a logic one. Since a bit is read by comparing the voltage difference between the two halves of the cell through a differential amplifier, any data read after a chip reset cycle but before a write cycle to the addressed location will be arbitrary and invalid. Once the chip is reset, the memory is ready to be written.

Byte Write Cycle

A byte may not be rewritten without first resetting the chip. Initially, and after each chip reset operation, all bits are in an indeterminate state and are prepared for programming. A byte write cycle is executed by applying V_{PP} to $\overline{CS_1}$ and a low (V_{IL}) to CS_2 while holding valid address and data values constant for a minimum t_{WP} specification (see Byte Write Cycle timing diagram). Since a high voltage supply is required for data alteration the device will operate as a read only memory in a 5V-only environment.

Standby Mode

Power consumption is reduced by 50% when the device is deselected. Applying a high to $\overline{CS_1}$, a low to CS_2, or a low to CS_3 puts the device in standby mode. Power consumption is further reduced in a CMOS environment with the address inputs held at V_{CC} or V_{SS}.

MODE SELECTION

$\overline{CS_1}$	CS_2	CS_3	Mode	I/O Pins
V_{IL}	V_{IH}	V_{IH}	Read	D_{OUT}
< 6V	V_{IL}	X	Standby	High Z
V_{IH}	X	X	Standby	High Z
< 6V	X	V_{IL}	Standby	High Z
V_{PP}	V_{IL}	X	Byte Write	D_{IN}
V_{PP}	V_{IH}	X	Chip Reset	High Z

Endurance

The BR46C15 is designed for applications requiring up to 100 write cycles per byte. Contact ROHM for special screening to higher levels of endurance.

PROGRAMMER SUPPORT

Many PROM and EPROM programmer manufacturers are supporting the BR46C15. Please contact ROHM for an up-to-date list of qualified programmers.

ABSOLUTE MAXIMUM RATINGS[1]

Temperature Under Bias ..... -65°C to +125°C
Storage Temperature ..... -65°C to +125°C
Supply Voltage ..... -1.0V to +7.0V
Voltage on any Pin with Respect to Ground (Except $\overline{CS}_1$)[2] ..... -1.0V to (V_{CC} + 0.5V)
Voltage on $\overline{CS}_1$ Pin with Respect to Ground ..... -1.0V to +20.5V
D.C. Output Current ..... -70mA

DC OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ± 10% for standard ('XLS') versions, V_{CC} = 5V ± 5% for /V5 versions.

Symbol	Parameter	Limits Min.	Limits Max.	Units	Test Conditions
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 6mA; V_{CC} = 4.5V
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -2mA; V_{CC} = 4.5V
V_C	Input Clamp Voltage		-1.0	V	I_{IN} = -18mA; V_{CC} = 4.5V
V_{PP}	Program Voltage on $\overline{CS}_1$	10.8	20.5	V	
I_{SC}	Output Short Circuit Current[3]		-70	mA	V_{OUT} = 0V; V_{CC} = 5.5V
I_{PP}	V_{PP} Supply Current		1.5	mA	WRITE or RESET modes
I_{IH}	Input Leakage Current — High		10	µA	V_{IN} = V_{CC} = 5.5V
I_{IL}	Input Leakage Current — Low		-10	µA	V_{IN} = 0V; V_{CC} = 5.5V
I_{LO}	Output Leakage Current		±10	µA	STANDBY mode; V_{CC} = 5.5V; V_{OUT} = 0 to 5.5V
I_{CC}	V_{CC} Current — Active Standard		90	mA	READ mode; t_{RC} = min.
I_{SB}	V_{CC} Current — Standby		45	mA	STANDBY mode
I_{SBC}	V_{CC} Current — CMOS Standby		35	mA	$\overline{CS}_1 \geq V_{CC}$ - 0.2V; CS_2, $CS_3 \geq$ 0.2V. $V_{IN} \leq$ 0.2V or $\geq V_{CC}$ - 0.2V

CAPACITANCE

T_A = +25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Parameter	Limits Min.	Limits Max.	Units	Test Conditions
$C_{I/O}$	Input/Output Capacitance		10	pF	STANDBY mode; $V_{I/O}$ = 2V
C_{IN}	Input Capacitance		10	pF	V_{IN} = 2V

Notes:

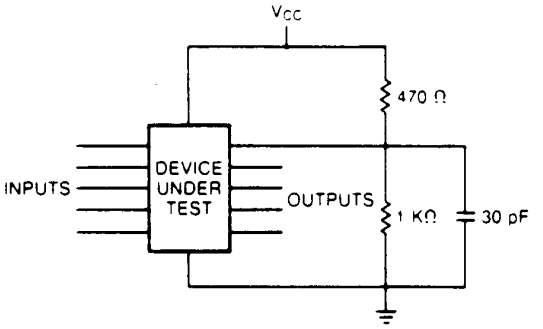
1. Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages higher than the rated maxima.
3. During I_{SC} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.
4. t_{WR} is defined as the minimum time required after a write pulse before initiating a data read cycle. This parameter is measured from the time at which the falling edge of $\overline{CS}_1$ reaches 5.5V until a valid read cycle is initiated. If a read cycle is initiated earlier than the minimum t_{WR} the output data may be invalid. Subsequent write cycles may be initiated immediately without delaying for t_{WR}.

AC CHARACTERISTICS

Read Cycle — See Figures 1 and 2.

T_A = 0°C to +70°C, V_{CC} = 5V ± 10% for standard ('XLS') versions, V_{CC} = 5V ± 5% for /V5 versions.

Symbol	Parameter	BR46C15-55 BR46C16-55 Limits		BR46C15-60 BR46C16-60 Limits		BR46C15-70 BR46C16-70 Limits		BR46C15-85 BR46C16-85 Limits		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	55		60		70		85		ns
t_{AA}	Address Access Time		55		60		70		85	ns
t_{CS}	$\overline{CS_1}$, CS_2 or CS_3 Access Time		35		40		40		45	ns
t_{LZ}	Chip Enable to Output Low Z	5		5		5		5		ns
t_{HZ}	Chip Disable to Output High Z	0	35	0	40	0	40	0	45	ns
t_{OH}	Output Hold from Address Change	10		10		10		10		ns



Input Signal Amplitude	0V to 3V
Input Rise and Fall Times	5ns from 1V to 2V
Frequency	1 MHz
Timing Reference Value	1.5V

Figure 1. AC Test Conditions

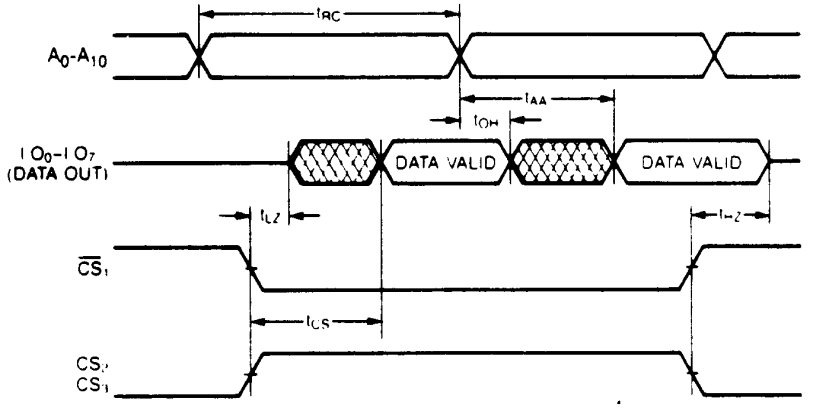


Figure 2. Read Cycle

Chip Reset and Byte Write Cycles — See Figures 3 and 4.
All Versions: T_A = +20°C to +30°C, V_{CC} = 5V ± 5%

Symbol	Parameter	BR46C15/BR46C16 LIMITS		Units
		Min.	Max.	
t_{RP}	Reset Pulse Width	50		ms
t_{WP}	Write Pulse Width	5		ms
t_{SC}	CS_2 Setup Time	0		ns
t_{HC}	CS_2 Hold Time	0		ns
t_{WR}	Write Recovery Time[4]	10		µs
t_{AS}	Address Setup Time	0		ns
t_{AH}	Address Hold Time	500		ns
t_{DS}	Data Setup Time	0		ns
t_{DH}	Data Hold Time	0		ns

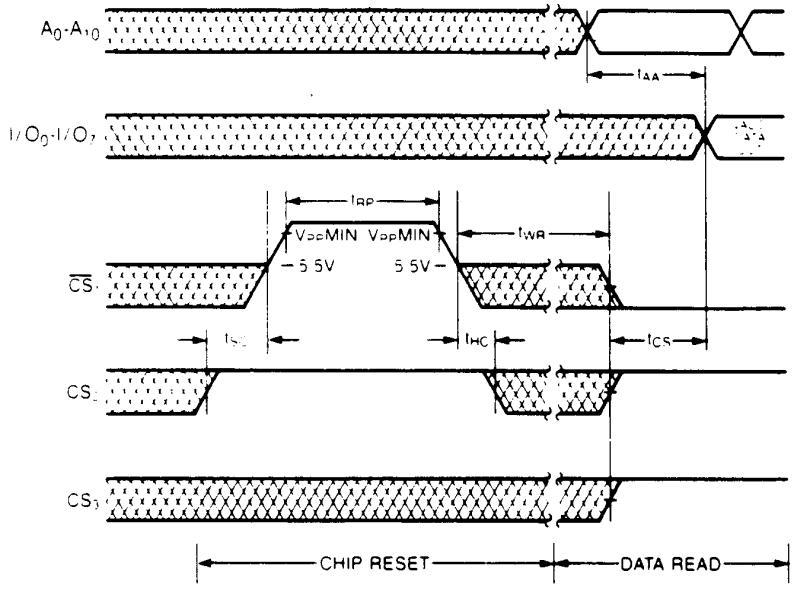


Figure 3. Chip Reset Cycle

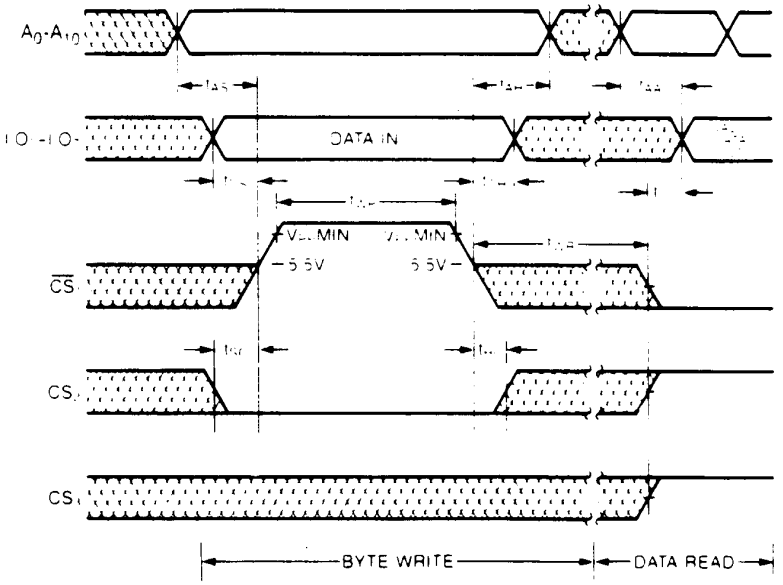
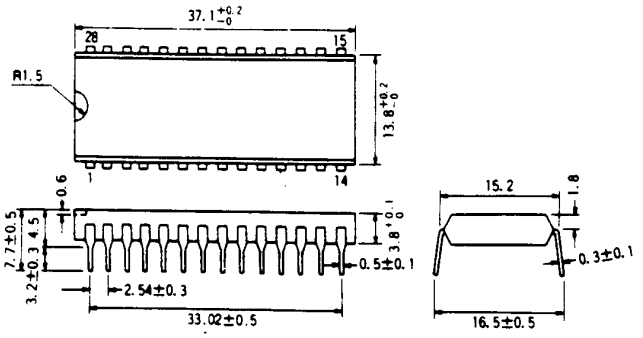


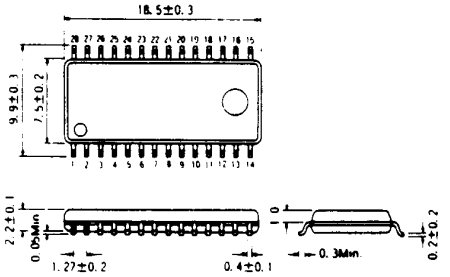
Figure 4. Byte Write Cycle

BR46C15
BR46C16



DIP24pin

BR46C15F
BR46C16F



MF28pin

ORDERING INFORMATION

Part Number	Access Time (ns)	Read Temperature Range (°C)	Programming Temperature Range (°C)	Operating Supply Variation (V)
BRS46C15*-55	55	0-70	20-30	4.5-5.5
BRS46C15*-60	60			
BRS46C15*-70	70			
BRS46C15*-85	85			
BRS46C15*-55/V5	55	0-70	20-30	4.75-5.25
BRS46C15*-60/V5	60			
BRS46C15*-70/V5	70			
BRS46C15*-85/V5	85			

* = for SOIC package type or None for plastic DIP.

Part Numbers:

BR	46C15	F
↑	↑	↑
Prefix	Part Type	Package Type: F for SOIC package None for plastic DIP

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