# HM50256 Series

### 262144-word × 1-bit Dynamic Random Access Memory

#### **FEATURES**

- Industry Standard 16-Pin DIP, 18-Pin PLCC, 16-Pin ZIP
- Single 5V (±10%)
- On chip substrate bias generator
- Low Power: 350mW active, 20mW standby
- High speed: Access Time 120ns/150ns/200ns(max.)
- Common I/O capability using early write operation
- Page mode capability
- TTL compatible
- 256 refresh cycles · · · (4ms)
- 3 variations of refresh · · · RAS only refresh, CAS before RAS refresh, Hidden refresh

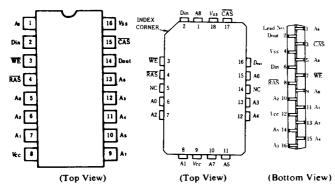
## **■ ORDERING INFORMATION**

Type No. Access Time		Package				
HM50256P-12	120ns	200 11 1 ( 1 Pl41-				
HM50256P-15	150ns	300 mil 16 pin Plastic				
HM50256P-20	200ns	DIP				
HM50256ZP-12	120ns					
HM50256ZP-15	150ns	16 pin Plastic ZIP				
HM50256ZP-20	200ns					
HM50256CP-12	120ns					
HM50256CP-15	150ns	18 pin PLCC				
HM50256CP-20	200ns	_				
	HM50256P-12 HM50256P-15 HM50256P-20 HM50256ZP-12 HM50256ZP-15 HM50256ZP-20 HM50256CP-12 HM50256CP-12	HM50256P-12 120ns HM50256P-15 150ns HM50256P-20 200ns HM50256ZP-12 120ns HM50256ZP-15 150ns HM50256ZP-20 200ns HM50256CP-12 120ns HM50256CP-12 120ns HM50256CP-15 150ns				

#### **PIN ARRANGEMENT**

HM50256P Series

HM50256CP Series
HM50256ZP Series



HM50256P Series



(DP-16B)

HM50256CP Series



(CP-18)

HM50256ZP Series



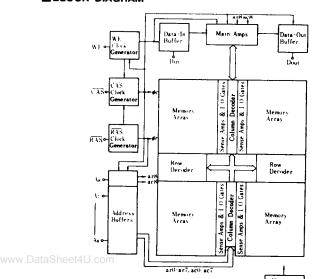
(ZP-16)

#### **■ PIN DESCRIPTION**

Ai~Ai	Address Inputs
CAS	Column Address Strobe
Din	Data In
Dout	Data Out
RAS	Row Address Strobe
WE	Read/Write Input
Vcc	Power (+5V)
Vss	Ground
A,~A,	Refresh Address Inputs



#### **■BLOCK DIAGRAM**



# **MASSOLUTE MAXIMUM RATINGS**

Voltage on any pin relative to V<sub>SS</sub> . . . . . . -1V to +7V Operating temperature, Ta (Ambient) . . . . 0°C to +70°C

# **TRECOMMENDED DC OPERATING CONDITIONS** $(Ta=0 \text{ to } +70^{\circ}\text{C})$

Parameter	Symbol	min	typ	max	Unit	Note
Supply Voltage	V <sub>cc</sub>	4.5	5.0	5.5	v	1
Input High Voltage	Vin	2.4		6.5	v	1 1
Input Low Voltage	VIL	-1.0	_	0.8	v	1

Note) 1. All voltages referenced to Vss

#### **DC** ELECTRICAL CHARACTERISTICS $(T_a-0 \text{ to } +70^{\circ}\text{C}, V_{cc}-5\text{V}\pm10\%, V_{ss}-0\text{V})$

Parameter	Symbol	HM50256-12		HM50256-15		HM50256-20			T
		min	max	min	max	min	max	Unit	Notes
Operating Current(RAS, CAS = Cycling: trc = min)	Icci	_	83	_	70	_	55	mA.	1
Standby Current(RAS - V.N. Dout - High Impedance)	Icc:		4.5		4.5	_	4.5	mA	
Refresh Current(RAS only Refresh, tac-min)	Iccs	_	62	_	53	_	42	mA	
Standby Current(RAS - VIN, Dout = Enable)	Ices	_	10	_	10	_	10	mA	1
Refresh Current(CAS before RAS Refresh, tac-min)	Icc.	_	69	_	58	_	45	m.A	<u> </u>
Page Mode Supply Current ( $\overline{RAS} = V_{IL}, \overline{CAS} = \text{Cycling}, t_{PC} = \text{min}$ )	leer	-	57		48	_	37	mA	<u> </u>
Input leakage(0 <v<7v)< td=""><td>Iu</td><td>-10</td><td>10</td><td>-10</td><td>10</td><td>-10</td><td>10</td><td>μA</td><td></td></v<7v)<>	Iu	-10	10	-10	10	-10	10	μA	
Output leakage(0 < V <sub>eet</sub> < 7V, Dout = Disable)	ILO	-10	10	-10	10	-10	10	μA	<u> </u>
Output levels High(Imi = -5mA)	Von	2.4	Vcc	2.4	Vcc	2.4	Vcc	v	$\vdash$
Output levels Low(Imt-4.2mA)	VoL	0	0.4	0	0.4	0	0.4	v	

Notes) 1. Icc depends on output loading condition when the device is selected. Icc max is specified at the output open condition.



# **ECAPACITANCE** ( $V_{cc} = 5V \pm 10\%$ , $T_a = 25^{\circ}C$ )

Parameter		Symbol	typ	max	Unit	Notes
Input Capacitance	Address, Data-in	Cn	_	5		1
	Clocks	Cn	_	7	pF	1, 2
Output Capacitance	Data-out	C <sub>0</sub>		7		1, 2

Notes) 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.

# ■ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

 $(Ta=0 \text{ to } +70^{\circ}\text{C}, \ V_{cc}=5\text{V}\pm10\%, \ V_{ss}=0\text{V})^{-10,-10}$ 

Parameter	Symbol	HM50256-12		HM50256-15		HM50256-20		1	l NI
		min	max	min	max	min	max	Unit	Notes
Random Read or Write Cycle Time	trc	220		260		330		ns	
Read-Write Cycle Time	trwc	265		310		390		ns	
RAS to CAS Delay Time	trco	25	60	25	75	30	100	ns	7
Access Time from RAS	trac		120	-	150		200	ns	2.3
Access Time from CAS	tCAC		60		75		100	ns	3, 4
Output Buffer Turn-off Delay	toff		30		40		50	ns	5
Transition Time (Rise and Fall)	tr	3	50	3	50	3	50	ns	6
RAS Precharge Time	trp	90		100		120		ns	
RAS Pulse Width	tras	120	10000	150	10000	200	10000	ns	
RAS Hold Time	trsn	60		75		100		ns	1
CAS Hold Time	tc s <sub>H</sub>	120		150		200		ns	1
CAS Pulse Width	tcas	60	10000	75	10000	100	10000	ns	
CAS to RAS Precharge Time	tcrp	10		10		10		ns	
Row Address Set-up Time	tasr	0		0	-	0	-	ns	
Row Address Hold Time	trah	15	1	15		20	-	ns	
Column Address Set-up Time	tasc	0		0		0	_	ns	
Column Address Hold Time	tc ah	20		25		30		ns	
Column Address Hold Time referenced to RAS	tar	80	1	100		130		ns	
Read Command Set-up Time	trcs	0		0		0		ns	1
Read Command Hold Time referenced to CAS	trch	0		0		U	-	ns	
Write Command Set-up Time	twcs	0	-	0		0		ns	8
Write Command Hold Time	twcn	4()		45		55		ns	
Write Command Hold Time referenced to RAS	twcR	100	1	120		155		ns	
Write Command Pulse Width	ħ₩P	40		45		55		ns	
Write Command to RAS Lead Time	trwl	40		45		55		ns	
Write Command to CAS Lead Time	tcwl	40	-	45		55		ns	
Data-in Set-up Time	tos	0	-	0		0	1	ns	9
Data-in Hold Time	toн	40		45		55		ns	8, 9
Data-in Hold Time referenced to RAS	tohr	100		120		155		ns	I
RAS to WE Delay	trw D	120		150		200		ns	
CAS to WE Delay	tcwp	60		75		100		ns	8
Page Mode Read or Write Cycle	t <sub>PC</sub>	120		145		190		ns	
Page Mode Read Modify Write Cycle	tpc m	165		195		250		ns	
CAS Precharge Time, Page Cycle	t <sub>CP</sub>	50	I	60	-	80		ns	
Read Command Hold Time referenced to RAS	trrh	10		10		10	I	ns	
Refresh Period	tref		4		4		4	ms	
CAS Set-up Time	tcsr	10		10		10		าาร	
CAS Hold Time (CAS before RAS Refresh)	tchr.	120		150	Ι -	200		ns	
RAS Precharge to CAS Hold Time	trpc	0		0	Ι	0		ns	<u> </u>

<sup>2.</sup> CAS - Vis to disable Dout.

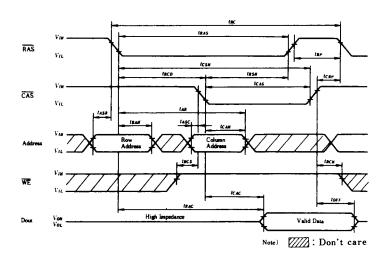
#### Notes

- 1. AC measurements assume  $t_T = 5$ ns.
- Assumes that  $t_{RCD} \leq t_{RCD}$  (max). If  $t_{RCD}$  is greater than the maximum recommended value shown in this table, IRAC exceeds the value shown.
- 3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
- Assumes that  $t_{RCD} \ge t_{RCD}$  (max).  $t_{OFF}$  (max) is defined as the time at which the output achieves the open circuit condition and output voltage levels are not referred.
- 6.  $V_{IH}$  (min) and  $V_{IL}$  (max) are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
- 7. Operation with the  $t_{RCD}$  (max) limit insures that  $t_{RAC}$  (max) can be met,  $t_{RCD}$  (max) is specified as a reference point only; if  $t_{RCD}$  is greater than the specified  $t_{RCD}$  (max) limit, access time is controlled exclusively by ICAC.

- 8. twcs, tcwp and trwp are not restrictive operating parameters.
  - They are included in the data sheet as electrical characteristics only; if  $t_{WCS} \ge t_{WCS}$  (min), the cycle is an early write cycle and the data output pin will remain open circuit (high impedance) throughout the entire cycle; if  $t_{CWD} \ge t_{CWD}$  (min) and  $t_{RWD} \ge$ IRWD (min), the cycle is a read-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeter-
- 9. These parameters are referenced to CAS leading edge in early write cycles and to WE leading edge in delayed write or read-modify-write cycles.
- An initial pause of 100 µs is required after power-up then execute at least 8 initialization cycles.
- At least, 8 CAS before RAS refesh cycles are required before using internal refresh counter.

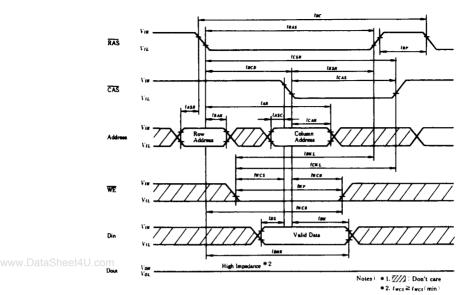
#### **TIMING WAVEFORMS**

#### READ CYCLE

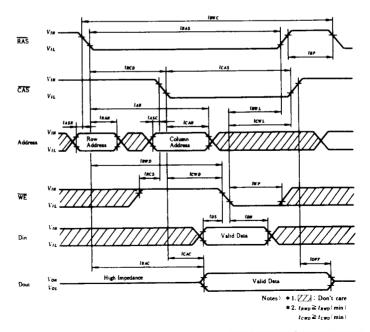




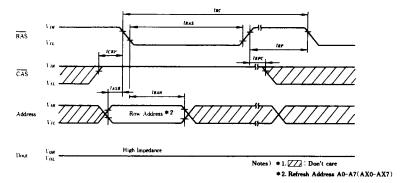
#### • WRITE CYCLE



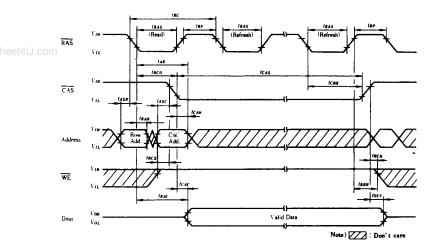
# • READ MODIFY WRITE CYCLE



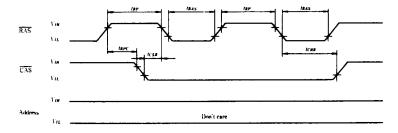
#### ● RAS ONLY REFRESH CYCLE



# • HIDDEN REFRESH CYCLE

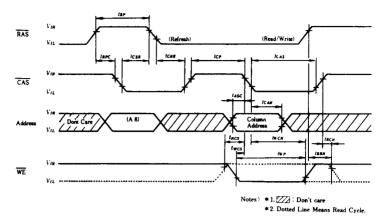


# ● CAS BEFORE RAS REFRESH CYCLE

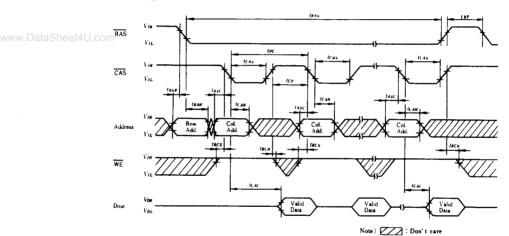




#### **COUNTER TEST**

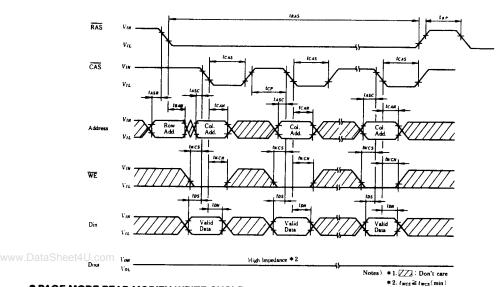


#### ● PAGE MODE READ CYCLE





#### ● PAGE MODE WRITE CYCLE



# ● PAGE MODE READ MODIFY WRITE CYCLE

