National Semiconductor

MICROCIRCUIT DATA SHEET

MNLM2990-12-X REV 0B0

Original Creation Date: 04/30/96
Last Update Date: 09/17/99
Last Major Revision Date: 04/30/96

NEGATIVE LOW DROPOUT REGULATOR

General Description

The LM2990 is low dropout, 1 ampere negative voltage regulator available with fixed output voltages of -5, -12, and -15V.

The LM2990 uses new circuit design techniques to provide low dropout and low quiescent current. The dropout voltage at 1A load current is typically 0.6V and a guaranteed worst-case maximum of 1V over the entire operating temperature range. The quiescent current is typically 1mA with 1A load current and an input-output voltage differential greater than 3V. A unique circuit design of the internal bias supply limits the quiescent current to only 9mA (typical) when the regulator is in the dropout mode (Vout - Vin $\leq$ 3V). Output voltage accuracy is guaranteed to $\pm$5% over load, and temperature extremes.

The LM2990 is short-circuit proof, and thermal shutdown includes hysteresis to enhance the reliability of the device when overloaded for an extended period of time.

Industry Part Number

LM2990

NS Part Numbers

LM2990J-12-QML
LM2990WG-12-QML

Prime Die

LM2990

Controlling Document

SEE FEATURES SECTION

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (^{O}C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- 5% output accuracy over entire operating range
- Output current in excess of 1A
- Dropout voltage typically 0.6V at 1A load
- Low quiescent current
- Internal short circuit current limit
- Internal thermal shutdown with hysteresis
- Functional complement to the LM2940 series
- CONTROLLING DOCUMENT:
  LM2990J-12-QML 5962-9571001QEA
  LM2990WG-12-QML 5962-9571001QXA

Applications

- Post switcher regulator
- Local, on-card, regulation
- Battery operated equipment

(Absolute Maximum Ratings)
(Note 1)

Input Voltage		-26V to +0.3V
Power Dissipation (Note 2, 3)		Internally Limited
Operating Temperature Range (Tj)		-55 C to +125 C
Maximum Junction Temperature (Tjmax)		150 C
Storage Temperature Range		-65 C to +150 C
Thermal Resistance		
ThetaJA		
CERDIP	(Still Air @ 0.5 C/W)	75 C/W
	(500LF/Min Air flow @ 0.5 C/W)	35 C/W
CERAMIC SOIC	(Still Air @ 0.5 C/W)	119 C/W
	(500LF/Min Air flow @ 0.5 C/W)	TBD
ThetaJC (Note 3)		
CERDIP		5 C/W
CERAMIC SOIC		3 C/W
Lead Temperature (Soldering, 10 seconds)		260 C
Package Weight (Typical)		
CERDIP		TBD
CERAMIC SOIC		TBD
ESD Susceptibility (Note 4)		2kV

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is Pdmax = (Tjmax -TA)/ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower. If this dissipation is exceeded, the die temperature will rise above 125 C, and the LM2990 will eventually go into thermal shutdown at a Tj of approximately 160 C.

Note 3: The package material for these devices allows much improved heat transfer over our standard ceramic packages. In order to take full advantage of this improved heat transfer, heat sinking must be provided between the package base (directly beneath the die), and either metal traces on, or thermal vias through, the printed circuit board. Without this additional heat sinking, device power dissipation must be calculated using junction-to-ambient, rather than junction-to-case, thermal resistance. It must not be assumed that the device leads will provide substantial heat transfer out of the package, since the thermal resistance of the leadframe material is very poor, relative to the material of the package base. The stated junction-to-case thermal resistance is for the package material only, and does not account for the additional thermal resistance between the package base and the printed circuit board. The user must determine the value of the additional thermal resistance and must combine this with the stated value for the package, to calculate the total allowed power dissipation for the device.

Note 4: Human body model, 100pF discharged through a 1.5K Ohms resistor.

Recommended Operating Conditions

(Note 1)

Maximum Input Voltage (Operational)

-26V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vin = -5V + Vo(NOM), Io = 1A, Co = 47uF.

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vo	Output Voltage	5mA ≤ Io ≤ 1A	1		-12.24	-11.76	V	1
			1		-12.60	-11.40	V	2, 3
Vrln	Line Regulation	Io = 5mA, Vo(NOM) -1V > Vin > -26V	1			60	mV	1, 2, 3
Vrld	Load Regulation	50mA ≤ Io ≤ 1A	1			70	mV	1
			1			100	mV	2, 3
Vdo	Dropout Voltage	Io = 0.1A, Delta Vo ≤ 100mV	1			0.3	V	1, 2, 3
		Io = 1A, Delta Vo ≤ 100mV	1			1	V	1, 2, 3
Iq	Quiescent Current	Io ≤ 1A	1			5	mA	1
			1			10	mA	2, 3
		Io = 1A, Vin = Vo(NOM)	1			50	mA	1, 2, 3
Ios	Short Circuit Current	Rl = 1 Ohm	1, 2		0.9		A	1
			1, 2		0.75		A	2, 3
Imax	Maximum Output Current		1, 2		1.4		A	1
Rr	Ripple Rejection	Vripple = 1Vrms, Fripple = 1KHz, Io = 5mA	1		42		dB	1
Von	Output Noise Voltage	10Hz-100Khz, Io = 5mA	1			1500	uV	1, 2, 3

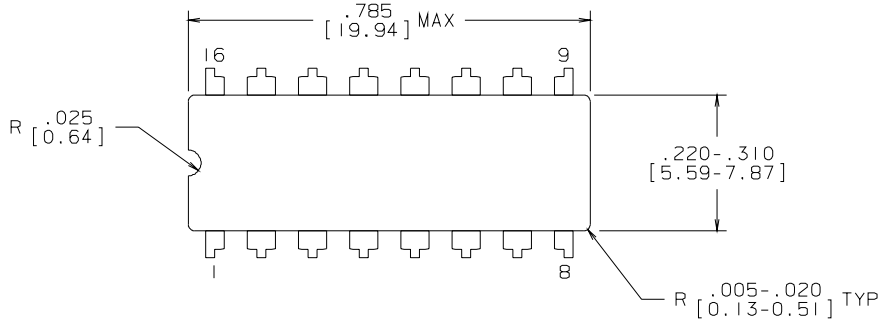
Note 1: Vo(NOM) is the nominal (typical) regulator output voltage, -5V, -12V or -15V.
Note 2: The short circuit current is less than the maximum output current with the -12V and -15V versions due to internal foldback current limiting. The -5V version, tested with a lower input voltage, does not reach the foldback current limit and therefore conducts a higher short circuit current level. If the LM2990 output is pulled above ground, the maximum allowed current sunk back into the LM2990 is 1.5A.

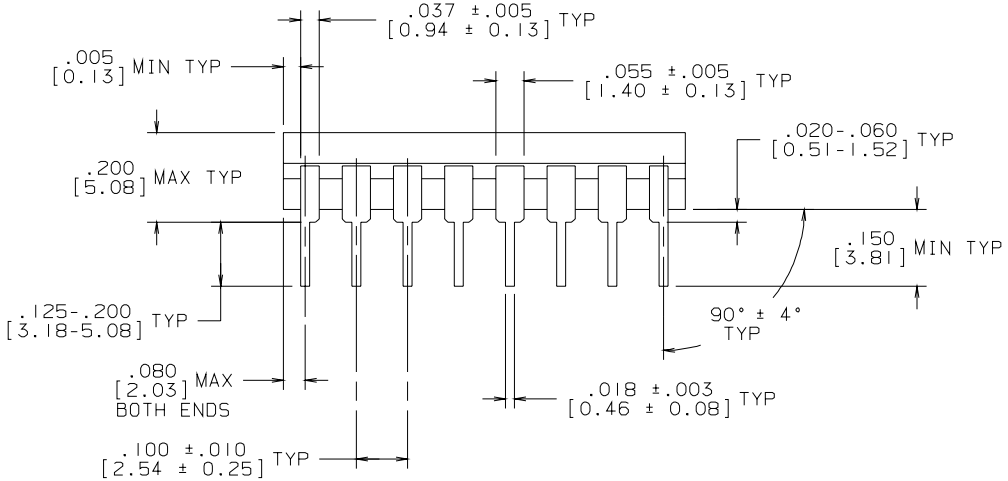
Graphics and Diagrams

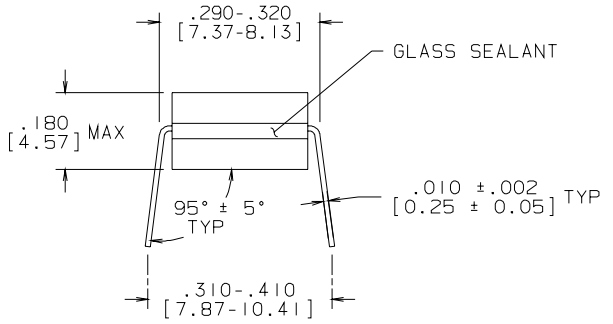
GRAPHICS#	DESCRIPTION
06324HRB3	CERDIP (J), 16 LEAD (B/I CKT)
06350HRA1	CERAMIC SOIC (WG), 16 LEAD (B/I CKT)
J16ARL	CERDIP (J), 16 LEAD (P/P DWG)
P000100B	CERDIP (J), 16 LEAD (PIN OUT)
P000383A	CERAMIC SOIC (WG), 16 LEAD (PINOUT)
WG16ARC	CERAMIC SOIC (WG), 16 LEAD (P/P DWG)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
L	REVISE PER CURRENT STD; REDRAW	09996	09/15/93	TL/







MIL/AERO CONFIGURATION CONTROL

MIL-M-38510 CONFIGURATION CONTROL

CONTROLLING DIMENSION: INCH

APPROVALS	DATE
DRAWN T. LEQUANG	09/15/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J), 16 LEAD

PROJECTION

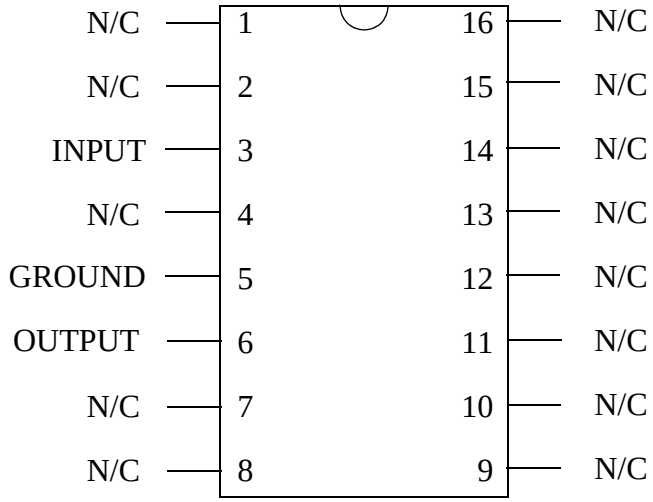
INCH [MM]

SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J16A	L

DO NOT SCALE DRAWING | SHEET 1 OF 1

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AD, DATED 04/1981.



LM2990J-XX

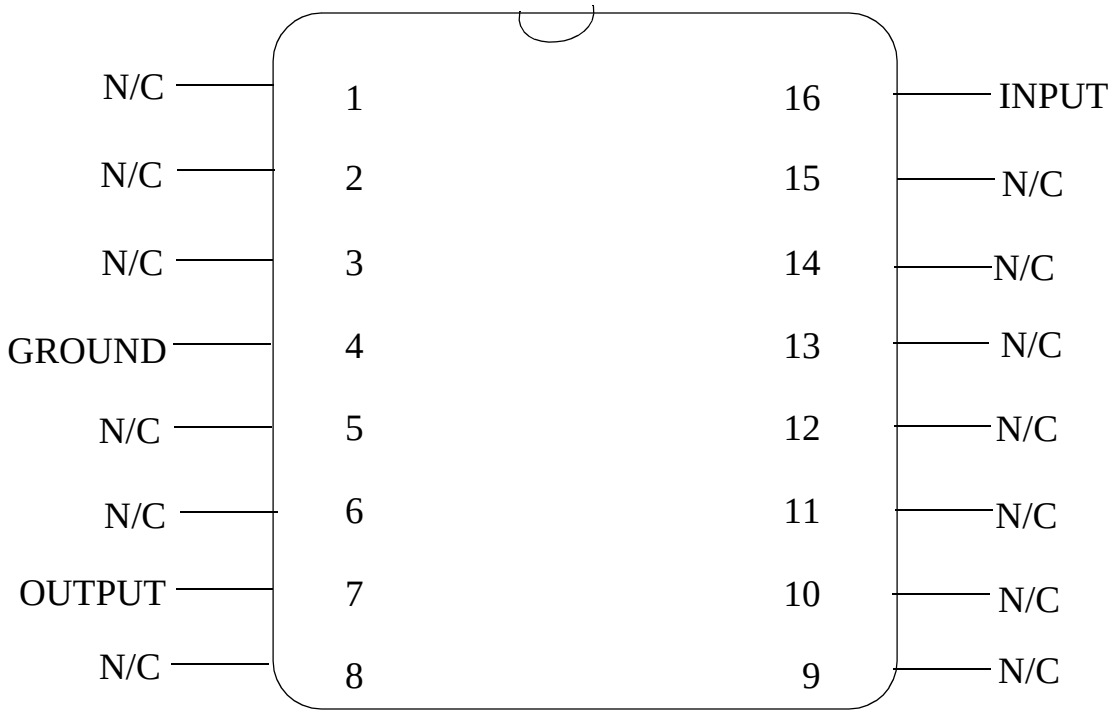
16 - LEAD DIP

CONNECTION DIAGRAM

(TOP VIEW)

P000100B

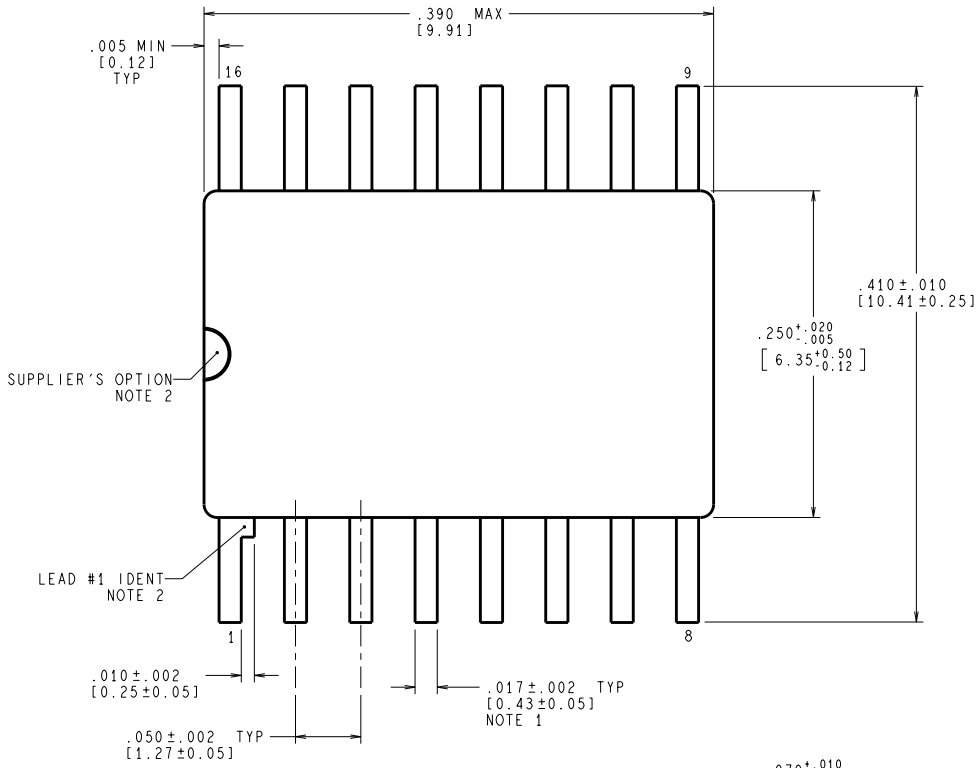
National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

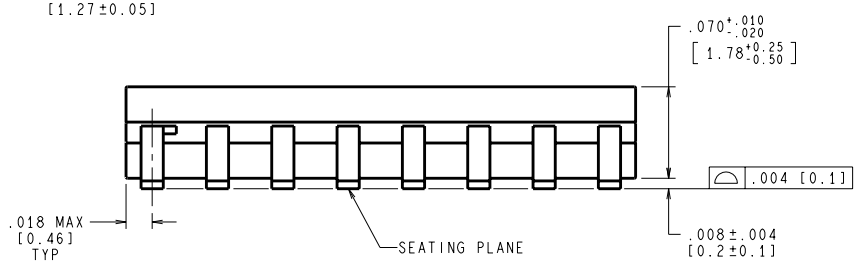


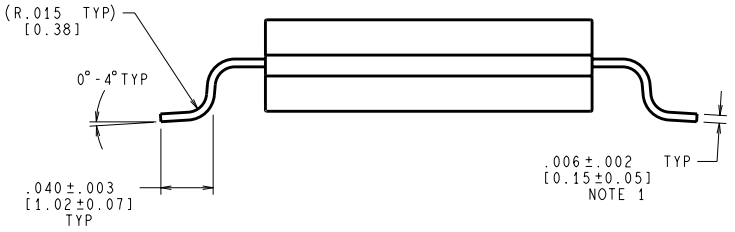
LM2990WG
16 - LEAD CERAMIC SOIC
CONNECTION DIAGRAM
TOP VIEW
P000383A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	11376	02/29/1996	MS/KH
B	LD PITCH TOL WAS ±.005; CHANGE LD RADIUS TO REF DIM; REMOVE THE OTHER R.006±.002; DIM .040±.003 WAS .037±.003	11443	04/19/1996	MS/KH
C	R .015[0.38] WAS R .006[0.15]	11840	10/08/1997	TL/







NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-PRF-38535 TO A MINIMUM THICKNESS OF 200 MICROINCHES/ 5.08 MICROMETERS. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE. MAXIMUM LIMIT MAY BE INCREASED BY .003 IN/ 0.08mm AFTER LEAD FINISH APPLIED.
2. LEAD 1 IDENTIFICATION SHALL BE:
   a) A NOTCH OR OTHER MARK WITHIN THIS AREA
   b) A TAB ON LEAD 1, EITHER SIDE
3. NO JEDEC REGISTRATION AS OF FEBRUARY 1996.

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

MIL-PRF-38535
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: MARTA SUCHY	02/29/96
DFTG. CHK.	
ENGR. CHK.	

National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

CERPACK, 16 LEAD, GULL WING

PROJECTION — INCH [MM]

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	(SC)MKT-WG16A	C

DO NOT SCALE DRAWING — SHEET 1 of 1

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0A0	M0000593	09/17/99	Barbara Lopez	Initial Release of: MNLM2990-12-X Rev. 0A0. Added note for power dissipation and reference to thermal resistance for Aluminum Nitride package.
0B0	M0003561	09/17/99	Rose Malone	Update MDS: MNLM2990-12-X, Rev. 0A0 to MNLM2990-12-X, Rev. 0B0. Moved reference to Controlling Document to Features Section. Added graphic's reference to WG Pkg to Main Table and Absolute Section and Package Weight heading.