silicon systems®
A TDK Group Company

SSI 32P3013
Pulse Detector with Programmable Filter

September 1994

DESCRIPTION

The SSI 32P3013 is a bipolar integrated circuit that provides all the data processing for pulse detection and four-burst servo capture from encoded read signals. This device can handle a NRZ data rate of 64 Mbit/s.

The SSI 32P3013 includes an AGC amplifier with AGC charge pump, a programmable 7-pole Bessel low pass filter, a pulse qualification circuit, and a 4-burst servo capture circuit. Automatic AGC control maintains a constant signal level into the pulse qualifier, and achieves fast write-to-read recovery. A time differentiator is included in the servo signal path, if so needed.

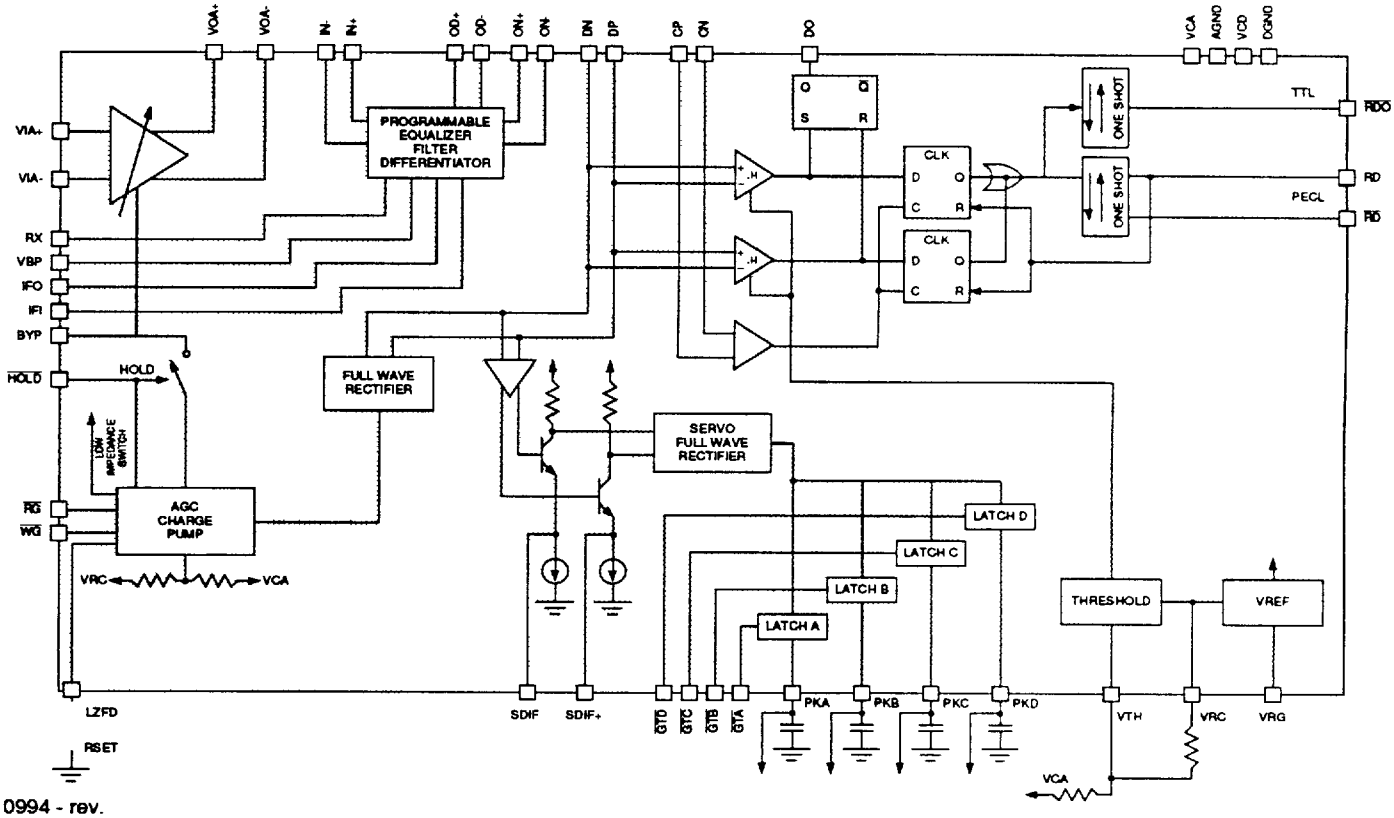
Ideal for constant density recording applications, the SSI 32P3013 low pass filter has a programmable 9-27 MHz bandwidth and 0-13 dB boost for pulse slimming. A time derivative of the read signal is also provided by the filter for time qualification in peak detection.

The SSI 32P3013 requires only a +5V power supply and is available in a 44-lead SOM package.

FEATURES

- **Compatible with 64 Mbit/s data rate operation**
- **Fast Attack/Decay modes for rapid AGC recovery**
- **Automatic AGC actions: Low Drift AGC hold, fast AGC recovery, and low AGC input impedance control signals**
- **Includes programmable pulse slimming equalization and programmable channel filter and differentiator with no external filter components**
- **±0.5 ns filter group delay variation from 0.3 FC to FC, FC = 27 MHz**
- **Independent positive and negative threshold qualification to suppress error propagation**
- **0.5 ns max pulse pairing**
- **Servo differentiator and 4-burst servo capture**
- **+5V only operation**
- **44-lead SOM package**

BLOCK DIAGRAM



0994 - rev.

FUNCTIONAL DESCRIPTION

The SSI 32P3013 Pulse Detector/Filter with 4-Burst Servo Capture is designed to support a 64 Mbit/s NRZ data rate. The signal processing circuits include a wide band variable gain amplifier, a sophisticated dual-rate AGC charge pump, a programmable electronic filter, a pulse qualifier, a servo differentiator and a 4-burst servo capture circuit.

Modes of Operation

The SSI 32P3013 can operate in one of three modes as controlled by $\overline{RG}$ and $\overline{WG}$.

Normal Read Mode $\overline{RG}$ = 0, $\overline{WG}$ = 1

In the normal Read Mode, the AGC actions are active. The AGC amplifier processes the input signal pulses; one-shot pulses are generated at the RD and $\overline{RD}$ outputs for each qualified signal peak. The $\overline{RDO}$ output buffer, which is a TTL buffer of the RD/$\overline{RD}$, is disabled and its output is pulled up high to reduce jitter and noise.

Servo Read Mode $\overline{RG}$ = 1, $\overline{WG}$ = 1

In the servo Read Mode, the AGC actions remain active (See note 1). The servo signal is amplified, fullwave rectified, differentiated and gated to the proper peak capture capacitor. The pulse qualifier remains active, and the $\overline{RDO}$ output is active to aid in servo decode.

Write Mode $\overline{RG}$ = X, $\overline{WG}$ = 0

In the Write Mode, the AGC actions are suspended. The AGC amplifier input impedance is clamped low to facilitate fast recovery. The $\overline{RDO}$ output is disabled and pulled up high to reduce jitter and noise.

AGC Amplifier

The wide band AGC amplifier amplifies the read signal from the read/write pre-amp to a signal level acceptable at the pulse qualifier. The AGC amplifier gain is an exponential function of the BYP voltage when referenced to VR.

$$Av = Ao \exp[\frac{(V_{BYP} - VR)}{K}] \quad \text{(See note 2)}$$

AGC Actions

The AGC loop maintains a constant DP/DN signal level at a nominal level, ~1 Vppd. The AGC actions are current charging and discharging to/from the external BYP integrating capacitor, and are classified into the following modes:

Normal Read and Servo Read Mode ($\overline{RG}$ = X, $\overline{WG}$ = 1)

Slow Decay: When the DP/DN signal is below 1 Vppd, a slow decay current, Id, charges the BYP capacitor. The AGC amplifier gain is increased slowly. This slow decay current tracks with the bandwidth of the filter. Id = 0.008 x IFI. At T = 27°C, the typical Id is 4.8 µA when the filter cutoff frequency is 27 MHz.

Slow Attack: When the DP/DN signal exceeds 1 Vppd, but is below 1.25 Vppd, a slow attack current, Ich, discharges the BYP capacitor. The AGC amplifier gain is decreased. The slow attack current is 20 times that of the slow decay current. Thus, for a given BYP capacitor, the slow attack response time is quicker than the slow decay response.

Fast Attack: When the DP/DN signal exceeds 1.25 Vppd, the device enters a Fast Attack mode. A fast attack current, Ichf, discharges the BYP capacitor. The AGC amplifier gain is quickly lowered. The fast attack current is seven times that of the slow attack current.

In servo Read Mode, constant AGC amplifier gain is generally desirable. Without an external AGC hold control, the servo data amplitude should be made lower than that of the data signal prior to the servo read mode. The SSI 32P3013 then enters the slow decay mode, which has a very slow effect on the AGC amplifier gain.

Write Mode ($\overline{RG}$ = X, $\overline{WG}$ = 0)

In the Write mode, the AGC charge pump is disabled. This holds the AGC amplifier gain at its previous value.

Notes:

1. The servo signal should have a lower amplitude than the data signal prior to the servo Read mode. Servo read should be completed before and significant change in AGC amplifier gain is resulted from the slow decay AGC mode.

2. In a closed AGC loop, the sensitivity of Ao and K to typical process variations is irrelevant. The typical values of Ao and K are provided for reference only, and not tested in production. Ao = 11, K = 0.22, VR = 3.6.

Write-to-Read Transition
($\overline{RG}$ = X, $\overline{WG}$ = 0-to-1)

When the SSI 32P3013 switches from the write to Read mode, i.e., $\overline{WG}$ 0-to-1 transition, the device remains in the low input impedance state for a preset time period, TLZ. For the next time period, TFD, the device then enters either the fast decay or Attack mode depending on the signal level at the DP/DN pins. The time periods are determined by an external resistor, RT, from the LZ/FD pin to ground.

TLZ (μs) = RT/78-0.26

TFD (μs) = RT/37-0.85, where RT is in kΩ.

RT must be greater than 45 kΩ.

Programmable Filter

The SSI 32P3013 includes a programmable low pass filter following the AGC amplifier for (1) 2X voltage gain from the AGC amplifier output to the pulse qualifier input, (2) noise limiting, (3) pulse slimming, and (4) provision of a time differentiated signal. The low pass filter is of a 7-pole 2-zero Bessel type. The filter's unboosted -3 dB bandwidth, defined as the cutoff frequency, is programmable from 9-27 MHz; the high frequency equalization is programmable from 0-13 dB at the cutoff frequency.

The filter input is ac-coupled from the AGC amplifier output. The filter's normal low pass output is ac-coupled to the data channel of the pulse qualifier. The differentiated low pass output is ac-coupled to the time channel of the pulse qualifier.

The normalized 7-pole 2-zero Bessel filter transfer function is given in Figure 1.

The cutoff frequency, fc, is programmable with 3 pins: RX, IFO and IFI. At the RX pin, an external resistor to ground establishes a reference current:

$$IFO = \frac{0.75}{Rx}, \text{at } T = 27°C$$

IFI should be made proportional to IFO for fc temperature stability. The cutoff frequency is related to the RX resistor, IFO and IFI currents as the following:

$$fc(MHz) = 27 \cdot \frac{IFI}{IFO} \cdot \frac{1.25}{Rx(k\Omega)}$$

For a fixed cutoff frequency setting, IFO and IFI can be tied together. The cutoff frequency equation then reduces to:

$$fc(MHz) = 27 \cdot \frac{1.25}{Rx(k\Omega)}$$

For programmable cutoff frequency, an external current DAC can be used. IFO should be the reference current into the DAC. The DAC output current drives IFI, which is then proportional to the IFO. The DACF in the SSI 32D4661 Time Base Generator is designed to control fc of the Silicon Systems programmable filters. When the DACF, which has a 4X current gain from its reference to fullscale output, is used, 5 kΩ RX is used. The fc is then given by:

$$fc(MHz) = 27 \cdot \frac{F\_Code}{127}$$

where F_Code is the decimal code equivalent to the 7-bit input into the DACF.

The high frequency equalization is programmable with two pins: VRG and VBP. The VRG is a bandgap reference voltage, 2.3V typically. The voltage at the VBP pin determines the amount of high frequency boost at the cutoff frequency. The boost function is as follows:

$$Boost(dB) = 20\log_{10}[(\frac{Kb \cdot VBP}{VRG}) + 1]$$

$$Kb = 3.041 + 0.0276 \cdot fci$$

where fci is the ideal cutoff frequency in MHz.

For a fixed boost setting, a resistor divider between VRG to ground can be used with the divided voltage at the VBP pin. For programmable equalization, an external voltage DAC can be used. VRG should be the reference voltage to the DAC. The DAC output voltage is then proportional to the VRG. The DAC in the SSI 32D4661 is designed to control the magnitude equalization of Silicon Systems programmable filters.

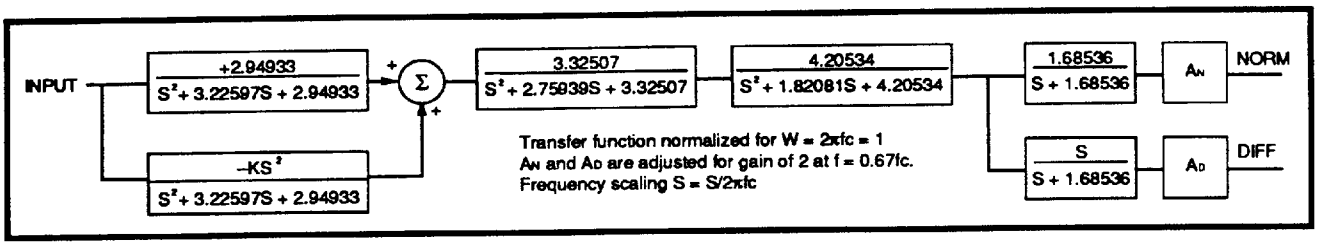


FIGURE 1: Bessel Filter Transfer Function

TABLE 1: Typical Change in f - 3 dB Point with Boost – $K = 2.94933\,(10^{\frac{BOOST(dB)}{20}} - 1)$

Boost (dB)	Gain@*f*c (dB)	Gain@peak (dB)	*f*Peak/fc	*f*-3dB/fc	K
0	-3	0.00	no peak	1.00	0
1	-2	0.00	no peak	1.20	0.36
2	-1	0.00	no peak	1.47	0.76
3	0	0.15	0.62	1.74	1.22
4	1	1.00	1.08	1.96	1.73
5	2	2.12	1.24	2.13	2.30
6	3	3.35	1.24	2.28	2.94
7	4	4.56	1.39	2.42	3.65
8	5	5.82	1.39	2.54	4.46
9	6	7.04	1.39	2.66	5.36
10	7	8.24	1.39	2.77	6.38
11	8	9.41	1.39	2.88	7.52
12	9	10.55	1.39	2.98	8.79
13	10	11.70	1.55	3.08	10.22

Notes: 1. *f*c is the original programmed cutoff frequency with no boost.
2. *f* - 3 dB is the new -3 dB value with boost implemented.
3. *f*peak is the frequency where the magnitude peaks with boost implemented.
e.g., *f*c = MHz when boost = 0 dB
if boost is programmed to 5 x dB then *f* - 3 dB = 27.69 MHz
*f*peak = 16.12 MHz

When DACs are used, the boost relation then reduces to:

$$\text{Boost(dB)} = 20\log_{10}[(Kb \bullet \frac{S\_Code}{127}) + 1]$$

Pulse Qualification

The SSI 32P3013 validates each DP/DN peak by a combination of level qualification and time qualification. In level qualification, a dual-comparator threshold detection eliminates errors due to low level additive noise. In time qualification, the filter's differentiated output is used to locate signal peaks.

Level Qualification

The dual-comparator architecture allows independent detection for positive and negative peaks. One comparator detects a positive peak by comparing the data signal with a positive threshold. The other comparator detects a negative peak by comparing the data signal with a negative threshold. Each comparator has a small hysteresis, 20% of the set threshold, to help qualify signals which just clear the set threshold.

The SSI 32P3013 comparator thresholds are set by a DC voltage at the VTH pin, such as from a resistor divider from VCA to VRC (see note 3). The threshold at each comparator can be computed as: Hysteresis Gain x (VTH - VRC). The thresholds at the two comparators are of the same magnitude, but of opposite polarity.

The SSI 32P3013 has three sets of pulse detector outputs: RD/$\overline{RD}$, $\overline{RDO}$, and DO. RD/$\overline{RD}$ output is the pseudo-ECL differential output. Corresponding to each validated peak of the DP/DN signal, a one-shot pulse occurs at the RD/$\overline{RD}$ output. The pulse width of the one-shot pulse is determined by an internal timing circuit, and specified in the electrical specification.

$\overline{RDO}$ is the TTL output of the pulse detector, logically equivalent to RD/$\overline{RD}$. Again, a one-shot pulse occurs at the $\overline{RDO}$ output for each validated peak of the DP/DN signal. The pulse width of this one-shot pulse is also specified in the electrical specification. The DO output is a test point used to monitor the output of the internal comparators, it is an open-emitter output requiring a 5 kΩ external resistor pull-down to ground.

Four-Burst Servo Differentiator and Capture

The SSI 32P3013 supports advanced embedded 4-burst servo technique. The signal at the DP/DN input can be time differentiated, fullwave rectified, and gated onto the selected peak capture output. A peak capture output is selected by pulling its corresponding $\overline{GT}$ x to logic '0.'

The transfer function from the DP/DN to the servo fullwave rectifier input is:

$$Av = \frac{1190Cs}{LCs^2 + (R+48.1)Cs + 1}$$

where: R, L, and C are external passive components across SDIF±

$$15\ pF < C < 125\ pF$$
$$s = jw$$

When the time differentiation function is not desired, a 2 kΩ resistor should be used across the SDIF± pins.

The transfer function from the servo fullwave rectifier input to the peak capture output is set so that a 1 Vppd DP/DN signal produces 0.95 Vpeak output. With no signal input, the outputs are set close to ground, with a finite offset common to all four channels.

Note 3: VCA is the +5V supply. VRC is the bandgap voltage referenced from VCA, i.e., VRC = VCA - VRG.

PIN DESCRIPTION

INPUT PINS

NAME	TYPE	DESCRIPTION
VIA+, VIA-	I	AGC Amplifier input pins.
IN+, IN-	I	Equalizer/filter input pins.
DP, DN	I	Data inputs to data comparators and fullwave rectifier.
CP, CN	I	Differentiated data inputs to the clock comparator.
VTH	I	Threshold level setting input for the data comparators.
$\overline{WG}$	I	TTL compatible input. When low the device is in Write Mode.

PIN DESCRIPTION (continued)

INPUT PINS

NAME	TYPE	DESCRIPTION
$\overline{RG}$	I	TTL compatible input. When low, the device is in normal Read Mode.
$\overline{WG}$	I	TTL compatible input. When low, the device is in Write Mode. When both $\overline{RG}$ and $\overline{WG}$ are high, the device is in Servo Mode.
$\overline{GTA}$, $\overline{GTB}$, $\overline{GTC}$, $\overline{GTD}$	I	TTL compatible input. When low the corresponding servo gate channel is enabled.
$\overline{HOLD}$	I	TTL compatible input. When low the AGC action is suspended.
OUTPUT PINS		
VOA+, VOA-	O	AGC amplifier output pins.
ON+, ON-	O	Equalizer/filter normal output pins.
OD+, OD-	O	Equalizer/filter differentiated output pins.
DO	O	ECL compatible data comparator latch output pin.
RD, $\overline{RD}$	O	ECL compatible read data output pins.
$\overline{RDO}$	O	TTL compatible read data output.
SDIF+, SDIF-	-	Pins for external differentiating network for servo data.
PKA, PKB PKC, PKD	O	Open non emitter outputs that provide a fullwave rectified signal from the servo differentiator. These outputs are referenced to AGND. These outputs are high impedance when not enabled by $\overline{GTX}$
ANALOG PINS		
VRC	-	Reference voltage pin for SERVO and LEVEL. VRC is referenced to VCA.
VRG	-	Reference voltage pin for the programmable filter.VRG is referenced to ground.
VBP	-	The equalizer high frequency boost is set by an external voltage applied to this pin. VBP must be proportional to VRG. Programmable boost is implemented by using a DAC that uses VRG as its reference. A fixed amount of boost can be set by an external resistor divide network connected from VBP to VRG and GND.
RX	-	Pin to set filter reference current. External resistor Rx from this pin to ground sets the filter reference current IFO.
IFO	-	Reference current output pin. The reference current is normally supplied as the reference current to a current DAC which generates the programmable input current for the IFI pin.
IFI	-	Programmable filter input current pin. The filter cutoff frequency is proportional to the current into this pin. The current must be proportional to the reference current out of IFO. A fixed filter cutoff frequency is generated by connecting IFO to IFI and selecting Rx to set the desired frequency.
LZ/FD	-	Pin for external resistor to set timing for both Low-Z input and Fast Decay modes.
BYP	-	The AGC integrating capacitor C_A is connected between BYP and VCA.
VCA, VCD	-	Analog and Digital +5 volts.
AGND, DGND	-	Analog and Digital grounds.

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, 4.5V < VCC < 5.5V, 0°C < Ta < 70°C

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

PARAMETER	RATING
Storage Temperature	-65 to +150°C
Junction Operating Temperature,Tj	+130°C
Supply Voltage, VCA, VCD	-0.7 to 7V
Voltage Applied to Inputs	-0.7 to VCA + 0.7V, -0.7 to VCD + 0.7V

RECOMMENDED OPERATING CONDITIONS

PARAMETER	RATING
Supply Voltage VCA = VCD = VCC	4.5V < VCC < 5.5V
Ambient Temperature, Ta	0°C < Ta < 70°C

POWER SUPPLY

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
PD	Power Dissipation	Outputs unloaded 4.5V < VCA, VCD < 5.5V		490	600	mW

LOGIC SIGNALS

VIL	TTL Input Low Voltage		-0.3		0.8	V
VIH	TTL Input High Voltage		2.0		VCC + 0.3	V
IIL	TTL Input Low Current	VIL = 0.4V	-0.4			mA
IIH	TTL Input High Current	VIH = 2.7V			0.1	mA
VOHE	ECL Output High Voltage		VCC -1.02		VCC -0.4	V
VES	ECL Differential Output Swing		0.3		0.6	V
TRF	EC1 Output Rise and Fall Time	CL ≤ 10 pF			3.5	ns
TS	Control Input Switching Times				0.1	µs
VOLT	TTL Output Low Voltage	IOL = 4 mA			0.5	V
VOHT	TTL Output High Voltage	IOH = -400 mA	2.4			V

ELECTRICAL SPECIFICATIONS (continued)

AGC AMPLIFIER

The input signals are AC coupled to VIA+ and VIA-. VOA+ and VOA- are AC coupled to IN+ and IN-. ON+ and ON- are AC coupled to DP and DN. Ca = 1000 pF. Fin = 4 MHz. Unless otherwise specified, the output is measured differentially at VOA+ and VOA-.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VIB	Input Range	Filter boost at fc = 0 dB	24		240	mVppd
		Filter boost at fc = 11 dB	20		100	mVppd
VD	DP-DN Voltage	VIA± = 0.1 Vppd	0.90		1.10	Vppd
VDV	DP-DN Voltage Variation	24 mVppd < VIA± < 240 mVppd			8.0	%
AV	Gain Range		2.0		28	V/V
AVPV	Gain Sensitivity w.r.t. BYP Voltage			38		dB/V
DR	VOA+ VOA- Dynamic Range	THD = 1% max, Vin = 24 mVp-p	0.75			Vppd
		THD = 2% max, Vin = 240 mVp-p				
RINDA	Differential Input Impedance	$\overline{WG}$ = 1	3.7	5.2	7.4	kΩ
RINSA	Single Ended Input Impedance	$\overline{WG}$ = 1		2.7		kΩ
VOS	Differential Output Offset Variation	$\overline{WG}$ = 0 from min. gain to max. gain	-200	108	+200	Ω mV
VIN	Input Referred Noise Voltage	gain = max, Rs = 0Ω filter not connected to VOA+ and VOA-, BW = 15 MHz		14	20	nV/√Hz
BW	Bandwidth	No AGC action, Gain = 22	50	70		MHz
CMRR	Common Mode Rejection Ratio	gain = max, Vin = 0 VDC + 100 mVpp @ 5 MHz	40	65		dB
PSRR	Power Supply Rejection Ratio	gain = max, 100 mVpp @ 5 MHz on VCA, VCD	45	55		dB
GDT	Gain Decay Time	VIA± = 240 mV to 120 mV VOA± > 0.9 Final Value IFI = 600 µA		44		µs
GAT	Gain Attack Time	VIA± = 120 mV to 240 mV VOA± < 1.1 Final Value IFI = 600 µA		2		µs

AGC CONTROL

The input signals are AC coupled to DP and DN. Ca = 1000 pF, 110 µA < IFI < 600 µA.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
ID	Discharge Current	$\overline{WG}$ = 1, DP - DN = 0V		0.008 x IFI		A
IDF	Fast Discharge Current			20 x Id		A
ICH	Charge Pump Attack Current	$\overline{WG}$ = 1, DP - DN = 0.55V		40 x Id		A
ICHF	Charge Pump Fast Attack Current, Ichf	$\overline{WG}$ = 1, DP - DN = 0.675V		7 x Ich		A
IK	BYP Pin Leakage Current	$\overline{WG}$ or $\overline{HOLD}$ = 0, VBYP = VCC - 1.5V	-0.1		+0.1	µA
VRC	VRC Reference Voltage			VCA -VRG		V
IVRC	VRC Output Drive		-0.75		+0.75	mA
VRG	VRG Reference Voltage	Isource 0 mA to 1 mA	2.2		2.45	V
TLZ	Low-Z Timing Accuracy	TLZ (µs) = RT(kΩ)/78-0.26, RT > 45 kΩ	-30		+30	%
TFD	Fast Decay Timing Accuracy	TFD (µs) = RT(kΩ)/37-0.85, RT > 45 kΩ	-30		+30	%

EQUALIZER/FILTER

The input signals are AC coupled to IN+ and IN-.

fc	Filter Cutoff Frequency	RX = 5 kΩ *fc* = 27 x IFI/(4 x IFO) MHz 4 ≥ IFO/IFI ≥ 4/3	9		27	MHz
IFO	IFO Reference Current	IFO = 0.75/RX; Tj = 27°C 5 kΩ > RX > 1.25 kΩ	0.15		0.6	mA
IFI	IFI Program Current Range	Tj = 27°C, 27 MHz > *fc* > 9 MHz	0.2		0.6	mA
FCA	FCA Filter FC Accuracy	*fc* = 27 MHz	-13		13	%
RX	RX Range		1.25		5	kΩ
AO	Normal Low Pass Gain AO = (ON ±) / (IN±)	Fin = 0.67*fc*	1.4		2.2	V/V
AD	Differentiated Low Pass Gain AD = (OD ±) / (IN±)	Fin = 0.67*fc*	0.8AO		1.2AO	V/V
FBA	Frequency Boost Accuracy	VBP = VRG	-1.5		+1.5	dB
		VBP/VRG = 0.5	-1.0		+1.0	dB

EQUALIZER/FILTER (continued)
The input signals are AC coupled to IN+ and IN-.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TGD1	Group Delay Variation	fc = 27 MHz, VBP = 0 to VRG fc > Fin > 0.3 fc	-0.7		+0.7	ns
TGD2		fc = 9 to 27 MHz, VBP = 0 to VRG fc > Fin > 0.3 fc	-2.5		+2.5	%
VOSVF	Output Offset Voltage Variation	200 µA < IFI < 600 µA	-200		200	mV
DRF	VOF Filter Output Dynamic Range	Fin = 0.67 fc THD = 1.5% max, ON± THD = 2.5% max, OD±	1.2			Vpp
RINF	Filter Input Resistance		3.0	3.9		kΩ
CINF	Filter Input Capacitance				7	pF
ROF	Filter Output Resistance	IO+ = 1.0 mA		30	60	Ω
IOF	Filter Output Current		-1.0		1.0	mA
VNN	Eout Output Noise Voltage; ON+, ON-	BW = 100 MHz, RS = 50Ω VBP = 0, fc = 27 MHz		2.8	5.0	mVRms
		BW = 100 MHz, RS = 50Ω VBP = VRG, fc = 27 MHz		5.9	8.5	mVRms
VND	Eout Output Noise Voltage; OD+, OD-	BW = 100 MHz, RS = 50Ω VBP = 0, fc = 27 MHz		5.5	7.5	mVRms
		BW = 100 MHz, RS = 50Ω VBP = VRG, fc = 27 MHz		15.0	21.0	mVRms

DATA COMPARATOR
The input signals are AC coupled to DP and DN.

RIND	Differential Input Resistance		8	9.6	14	kΩ
CIND	Differential Input Capacitance			2	5	pF
VOSD	Comparator Offset Voltage	Not directly measurable			4	mV
HYS	Threshold Voltage Gain	VTH - VRC = 0.3V	0.40		0.52	V/V
		VTH - VRC = 0.9V	0.42		0.49	V/V
VSH	Threshold Voltage Hysteresis (Note 1)			0.20 x GHYS x (VTH -VRC)		V/V
TPDD	Propagation Delay	To DO		4		ns
IVTH	VTH Input Bias Current				2	µA

Note 1: Not directly measureable

CLOCKING

The input signals are AC coupled to CP and CN.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VOSC	Comparator Offset Voltage	Not directly measurable			4	mV
RINC	Differential Input Resistance		8	9.7	14	kΩ
CINC	Differential Input Capacitance			1.4	5	pF
TDS	D Flip-Flop Set Up Time	DP-DN threshold to CP-CN zero cross, CP-CN = 1 Vppd at 18 MHz		0.3	1	ns
PP	Pulse Pairing	Vs = 1 Vpp, F = 10 MHz		0.1	0.5	ns
TPDC	Propagation Delay from CP-CN zero crossing to RD	Vs = 20 mVpp square wave		7		ns
PWRD	RD Output Pulse Width		10		16	ns
PWRT	$\overline{RDO}$, TTL Output Pulse Width		25		45	ns

SERVO DIFFERENTIATOR/FULL-WAVE RECTIFIER

An external series network with R = 600Ω, C = 27 pF, L = 22 µF is connected between SDIF and $\overline{SDIF}$ to determine the servo differentiator transfer function. The input signals are AC coupled to DP and DN. Fin = 6.7 MHz at 1.0 Vppd.

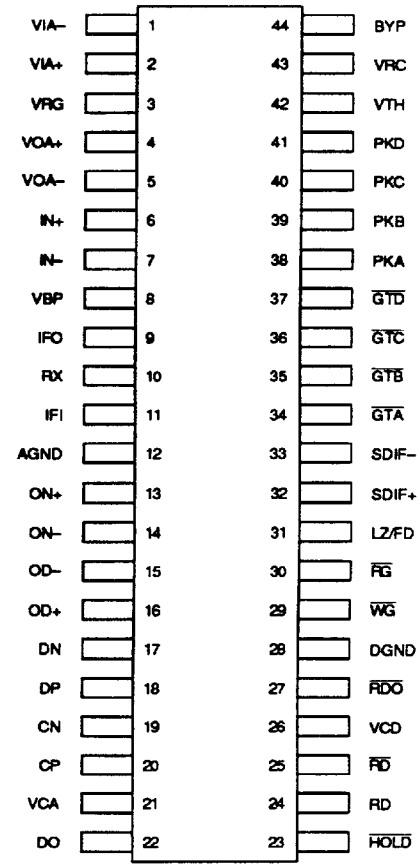
ISDIF	SDIF+ to SDIF- pin current	Differentiator impedance must be set so as not to dip the signal for this level	1.4	2.0	2.6	mA
RDIF	Internal differentiator pull-up resistors	Cannot be directly tested	0.4	0.6	0.8	kΩ
FWR	Input voltage range to maintain FWR voltage gain	Cannot be directly tested	0.1		2.0	Vppd
RERR	Rectification Error		-10		10	%
AFWR	FWR Voltage Gain from DP/DN Inputs to PKA-D Outputs	0.1 Vppd ≤ V(DP/DN) ≤ 1.0 Vppd V(PKx) = 0.09+ 0.96 V(DP/DN), Fin = 4 MHz	-20		20	%
ISL	Servo Output Leakage Current	Channel disabled		0.1	1	µA
VCOS	PKA-D Channel to Channel Offset	1 Vppd input to DP/DN PKA-PKB, PKC-PKD	-10		+10	mV
VAOS	PKA-D Absolute Offset Magnitude	1 Vppd input to DP/DN (across all channels)	0		20	mV

SSI 32P3013
Pulse Detector with Programmable Filter

PACKAGE PIN DESIGNATIONS
(Top View)

THERMAL CHARACTERISTICS: tjA

44-Lead SOM	70°C/W



44-Lead SOM

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGE MARK
SSI 32P3013 44-Lead SOM	32P3013-CM	32P3013-CM

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914