Data Sheet
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microelectronics group

Lucent Technologies
Bell Labs Innovations

TMPR28051 STS-1/AU-3 Mapper

Features

Overall Device:

- PLL-free receive operation when used with Lucent Technologies Microelectronics Group T7690 Line Interface Unit
- High-speed microprocessor interface configurable to operate with most commercial microprocessors
- Inserts valid B1, B2, and B3 bit interleaved parity (BIP) in the transmit direction
- Detects and counts B1, B2, and B3 BIP-8 errors on either a bit or block basis for performance monitoring in the receive direction
- Detects and counts BIP-2 errors on either a bit or block basis for performance monitoring
- Detects and counts far-end block errors (FEBE)
- Built-in test pattern insert and drop for setup and maintenance
- –40 °C to +85 °C temperature range
- 208-pin shrink quad flat pack (SQFP) package

28 DS1 to STS-1 Mapper Mode:

- Maps 28 asynchronous DS1 signals to SONET synchronous payload envelope (SPE)
- Configurable VT1.5 slot selection for DS1 insertion
- Configurable VT1.5 slot selection for DS1 drop
- Detects STS-1 loss of pointer (LOP-P), loss of H4 multiframe, path alarm indication signal (AIS-P), and path remote defect indication (RDI-P)
- Automatic receive monitor functions include VT remote defect indication (RDI-V), BIP-2 errors, VT AIS (AIS-V), and VT loss of pointer (LOP-V)
- User configurable for VT label, AIS-V, RDI-V, force BIP-2 errors, or unequipped tributary insertion

21 E1 to AU-3 Mapper Mode:

- Maps 21 asynchronous E1 signals to SDH AU-3
- Configurable TU-12 slot selection for E1 insertion
- Configurable TU-12 slot selection for E1 drop
- Detects AU-3 loss of H4 multiframe, AIS-P, and RDI-P
- Automatic receive monitor functions include TU RDI, BIP-2 errors, TU AIS, and TU loss of pointer
- User configurable for TU label, TU AIS, TU RDI, or force BIP-2
- User-provisionable AIS insertion on all TU-12

Applications DS1/E1 Modes

- SONET/SDH path termination multiplexers
- SONET/SDH add/drop multiplexers
- SONET/SDH cross connects
- Digital access cross connects
- DS1/E1 broadcast
- SONET/SDH test equipment

Description

The TMPR28051 device has two modes of operation: DS1 and E1. Pin 102 is the DS1/E1 mode select pin. This data sheet first describes the DS1 mode (Page 6) and then the E1 mode (Page 47).

In both modes of operation:

- Automatic receive monitoring functions can be configured to provide an interrupt to the control system, or the device can be operated in a polled mode.
- Built-in test pattern insertion and drop allows end-to-end testing for initial setup or maintenance without the need for external test equipment.

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Description DS1 Mode

The TMPR28051 device provides all of the functions necessary to insert and drop up to 28 asynchronous DS1 signals into a SONET SPE. On the STS-1 side, the device can be configured for either a serial bit stream or an 8-bit parallel input bus. This allows the device to drive an OC1 optical signal directly or to allow for modular growth in terminal or add/drop applications. On the DS1 side, the device is designed to interface with the Lucent T7690 Quad Line Transceiver, or equivalent, using the internal jitter attenuator buffer for PLL-free operation.

The device is designed such that a gapped, non 50% duty cycle clock is sent toward the DS1 line. This gapped clock must be smoothed by a device such as the T7690 before being sent to the line.

Built-in loopbacks at both the STS-1 and DS1 sides provide maximum flexibility for use in a number of SONET/DS1 products including terminal multiplexers, add/drop multiplexers, and digital cross connects.

A high-speed microprocessor interface and full user programmability on DS1 to VT1.5 slot insertion and drop provide maximum flexibility for DS1 I/O configuration.

Block Diagram DS1 Mode

The DS1 mode block diagram is shown in Figure 1. For illustration purposes, only two of the 28 DS1 bidirectional blocks are shown.

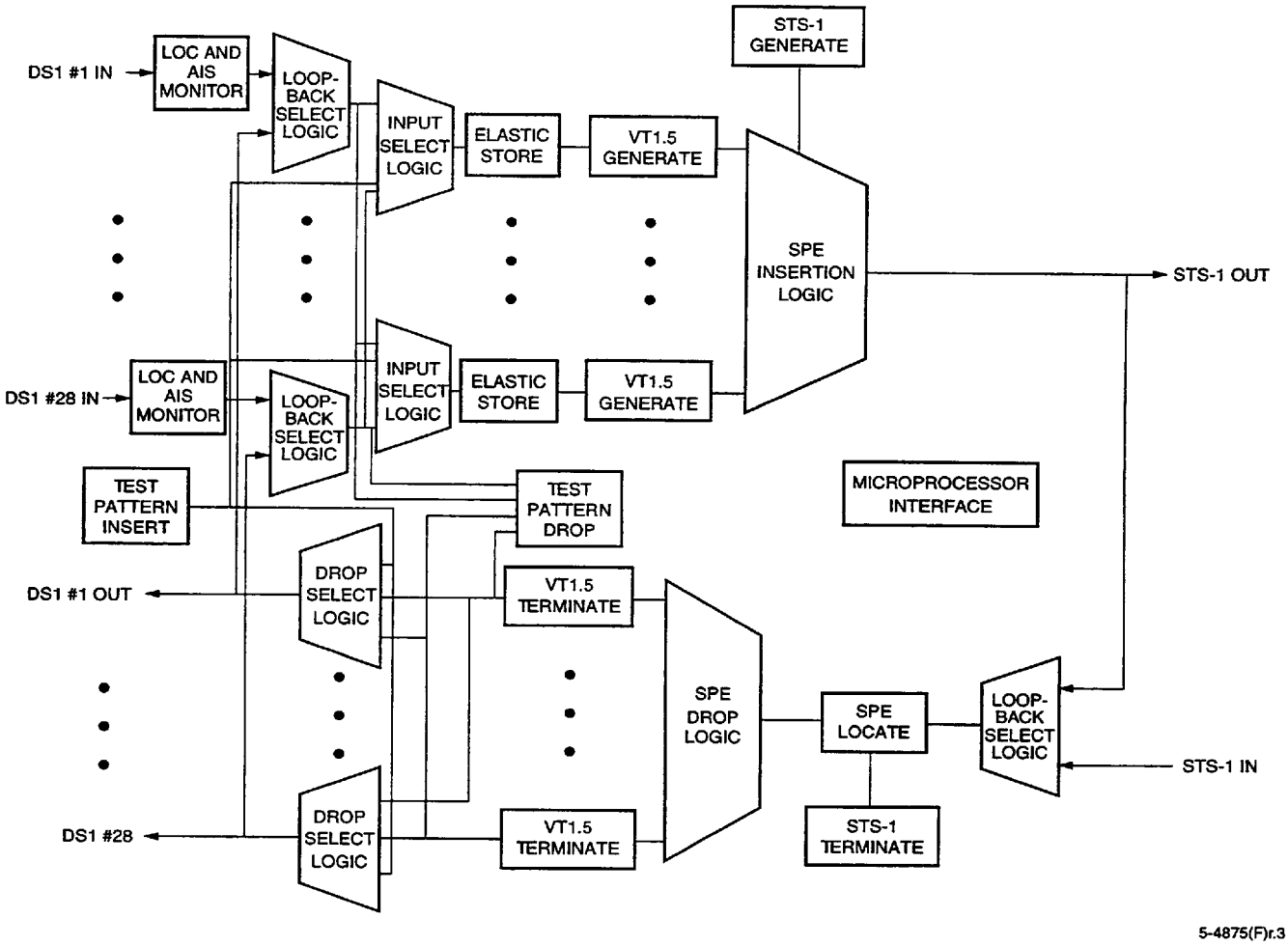

Figure 1. Block Diagram DS1 Mode

Pin Information DS1 Mode

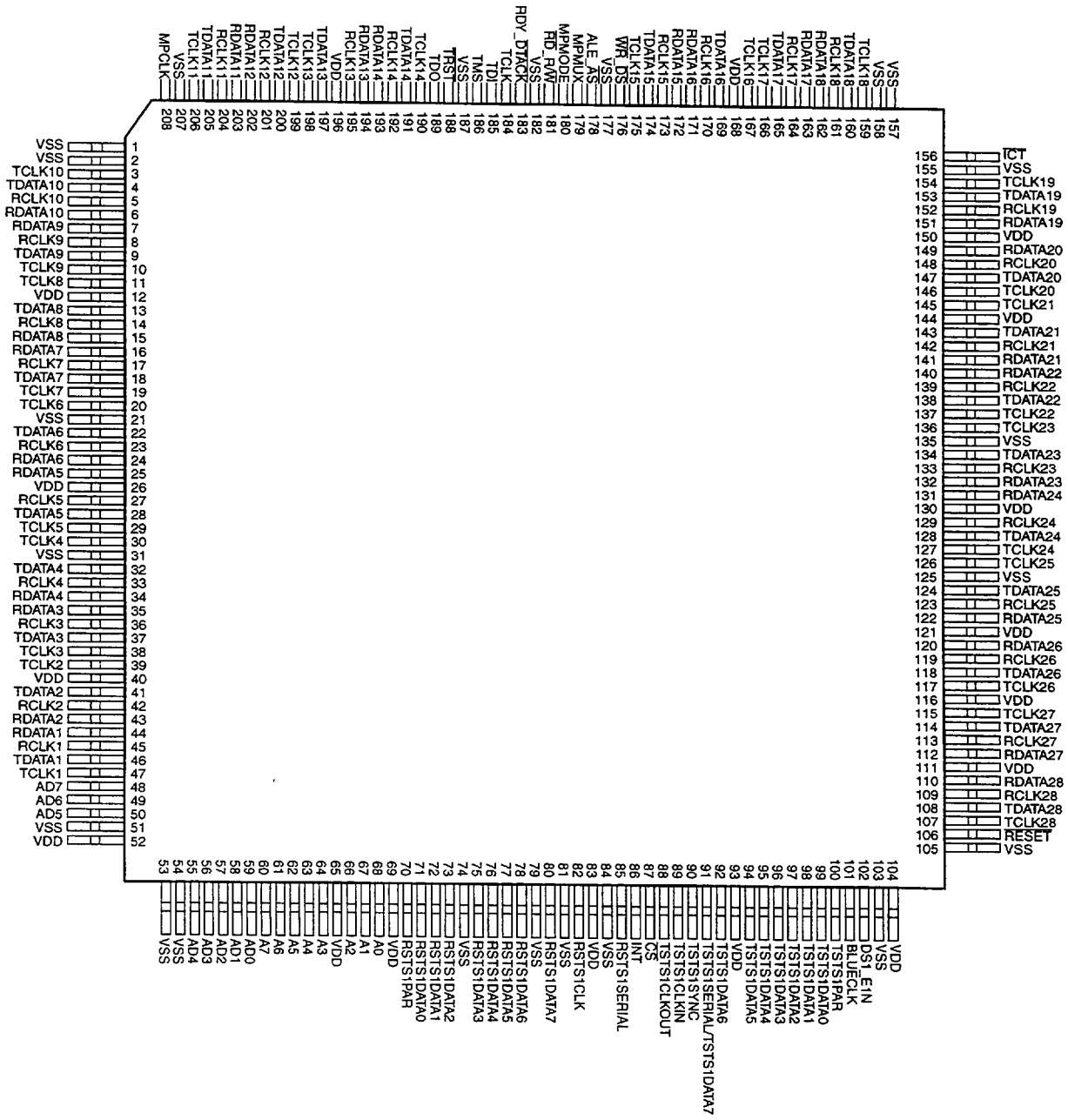

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Figure 2. Device Pinout DS1 Mode

Pin Information DS1 Mode (continued)

Table 1. Pin Descriptions DS1 Mode

Pin	Symbol	Type*	Name/Description
47, 39, 38, 30, 29, 20, 19, 11, 10, 3, 206, 199, 198, 190, 175, 167, 166, 159, 154, 146, 145, 137, 136, 127, 126, 117, 115, 107	TCLK[1:28]	O	**Transmit DS1 Clock.** Gapped DS1 clock (not 50% duty cycle).
46, 41, 37, 32, 28, 22, 18, 13, 9, 4, 205, 200, 197, 191, 174, 169, 165, 160, 153, 147, 143, 138, 134, 128, 124, 118, 114, 108	TDATA[1:28]	O	**Transmit DS1 Data.** Transmit data to the LIU.
45, 42, 36, 33, 27, 23, 17, 14, 8, 5, 204, 201, 195, 192, 173, 170, 164, 161, 152, 148, 142, 139, 133, 129, 123, 119, 113, 109	RCLK[1:28]	I^u	**Receive DS1 Clock.** Received clock from the LIU. An internal 100 kΩ pull-up is on these pins.
44, 43, 35, 34, 25, 24, 16, 15, 7, 6, 203, 202, 194, 193, 172, 171, 163, 162, 151, 149, 141, 140, 132, 131, 122, 120, 112, 110	RDATA[1:28]	I^u	**Receive DS1 Data.** Received data from the LIU. An internal 100 kΩ pull-up is on these pins.
102	DS1_E1N	I	**DS1/E1 Input Identifier.** If this pin is pulled high, the device acts as a DS1 to STS-1 mapping device. If pulled low, it acts as an E1 to AU-3 mapper.
101	BLUECLK	I	**Blue Signal Clock.** In the event of a loss of input DS1 clock or an unprovisioned DS1 output, this clock signal is used to generate the DS1 blue signal (all 1s). This clock must be 1.544 MHz ± 32 ppm or 16 times this rate.
176	$\overline{WR}\_\overline{DS}$	I	**Write (Active-Low).** If MPMODE = 1 (pin 180), this pin is asserted low by the microprocessor to initiate a write cycle. **Data Strobe (Active-Low).** If MPMODE = 0, this pin becomes the data strobe for the microprocessor. When R/$\overline{W}$ = 0 (write), a low applied to this pin latches the signal on the data bus into internal registers.

* I^u indicates an internal pull-up.

Pin Information DS1 Mode (continued)

Table 1. Pin Descriptions DS1 Mode (continued)

Pin	Symbol	Type*	Name/Description
179	MPMUX	I	**Microprocessor Multiplex Mode.** Setting MPMUX = 1 allows the microprocessor interface to accept the multiplexed address and data signals. Setting MPMUX = 0 allows the microprocessor interface to accept demultiplexed (separate) address and data signals.
180	MPMODE	I	**Microprocessor Mode.** When MPMODE = 1, the device uses the address latch enable type microprocessor read/write protocol with separate read and write controls. Setting MPMODE = 0 allows the device to use the address strobe type microprocessor read/write protocol with a separate data strobe and a combined read/write control.
181	$\overline{RD}$_R/$\overline{W}$	I	**Read (Active-Low).** If MPMODE = 1 (pin 180), this pin is asserted low by the microprocessor to initiate a read cycle. **Read/Write.** If MPMODE = 0, this pin is asserted high by the microprocessor to indicate a read cycle or asserted low to indicate a write cycle.
178	ALE_$\overline{AS}$	I	**Address Latch Enable.** If MPMODE = 1 (pin 180), this pin becomes the address latch enable for the microprocessor. When this pin transitions from high to low, the address bus inputs are latched into the internal registers. **Address Strobe (Active-Low).** If MPMODE = 0, this pin becomes the address strobe for the microprocessor. When this pin transitions from high to low, the address bus inputs are latched into the internal registers.
87	$\overline{CS}$	I^u	**Chip Select (Active-Low).** This pin is asserted low by the microprocessor to enable the microprocessor interface. If MPMUX = 1 (pin 179), $\overline{CS}$ can be externally tied low to use the internal chip selection function (see Microprocessor Configuration Modes section on page 20). An internal 100 kΩ pull-up is on this pin.
86	INT	O	**Interrupt.** This pin is asserted high to indicate an interrupt produced by an alarm condition in register 3 or 5. The activation of this pin can be masked by microprocessor registers 4 and 6.
183	RDY_$\overline{DTACK}$	O	**Ready.** If MPMODE = 1 (pin 180), this pin is asserted high to indicate the device has completed a read or write operation. This pin is in a high-impedance state when $\overline{CS}$ (pin 87) is high. **Data Transfer Acknowledge (Active-Low).** If MPMODE = 0, this pin is asserted low to indicate the device has completed a read or write operation.
106	$\overline{RESET}$	I^u	**Hardware Reset (Active-Low).** If $\overline{RESET}$ is forced low, all internal states in the transceiver paths are reset and data flow through each channel will be interrupted (see Device-Level Control, Alarm, and Mask Bits (0x00—0x16) section on page 34). An internal 100 kΩ pull-up is on this pin.
156	$\overline{ICT}$	I^u	**In-Circuit Test Control (Active-Low).** If $\overline{ICT}$ is forced low, all output pins are placed in the high-impedance state. An internal 100 kΩ pull-up is on this pin.
48—50, 55—59	AD[7:0]	I/O	**Microprocessor Interface Address/Data Bus.** If MPMUX = 0 (pin 180), these pins become the bidirectional, 3-statable data bus. If MPMUX = 1, these pins become the multiplexed address/data bus. In this mode, only the lower 7 bits (AD[6:0]) are used for the internal register addresses.
60—64, 66—68	A[7:0]	I	**Microprocessor Interface Address.** If MPMUX = 0 (pin 180), these pins become the address bus for the microprocessor interface registers.

* I^u indicates an internal pull-up.

Pin Information DS1 Mode (continued)

Table 1. Pin Descriptions DS1 Mode (continued)

Pin	Symbol	Type*	Name/Description
208	MPCLK	I^u	**Microprocessor Interface Clock.** Microprocessor interface clock rates from twice the DS1 line clock rate (3.088 MHz) to 16.384 MHz are supported. An internal 100 kΩ pull-up is on this pin.
184	TCLK	I^u	**JTAG Clock.** An internal 100 kΩ pull-up is on this pin.
185	TDI	I^u	**JTAG Input Data.** An internal 100 kΩ pull-up is on this pin.
186	TMS	I^u	**JTAG Mode Select.** An internal 100 kΩ pull-up is on this pin.
188	$\overline{\text{TRST}}$	I^u	**JTAG Reset (Active-Low).** An internal 100 kΩ pull-up is on this pin.
189	TDO	O	**JTAG Output Data.**
89	TSTS1CLKIN	I	**Transmit STS-1 Clock.** The STS-1 clock can be 51.84 MHz for serial input data or 6.48 MHz for byte wide data.
90	TSTS1SYNC	I	**Transmit STS-1 Sync.** The STS-1 sync pulse can be provisioned to be active on either the first or last clock of the STS-1 frame.
92, 94—99	TSTS1DATA[6:0]	O	**Transmit STS-1 Data.** In the byte wide output mode, this is bit 6—bit 0 of the data bus. TSTS1DATA7 as the most significant bit of the output byte.
100	TSTS1PAR	O	**Transmit STS-1 Parity.** The parity output is only defined for byte wide data. The device can be provisioned to source either an odd or even parity.
91	TSTS1SERIAL/ TSTS1DATA7	O	**Transmit STS-1 Serial Data/Transmit STS-1 Data Bit 7 (MSB).** In serial mode this pin provides 51.84 Mbits/s serial data. In parallel mode this pin provides TSTS1DATA7.
88	TSTS1CLKOUT	O	**Transmit STS-1 Output Clock.**
82	RSTS1CLK	I	**Receive STS-1 Clock.** The STS-1 clock can be 51.84 MHz for serial input data or 6.48 MHz for byte wide data.
80, 78—75, 73—71	RSTS1DATA[7:0]	I^u	**Receive STS-1 Data.** In the byte wide input mode, this is the data bus with RSTS1DATA7 as the most significant bit of the input byte. An internal 100 kΩ pull-up is on this pin.
70	RSTS1PAR	I^u	**Receive STS-1 Parity.** The parity input is only defined for byte wide data. The device can be provisioned to accept either an odd or even parity. An internal 100 kΩ pull-up is on this pin.
85	RSTS1SERIAL	I	**Receive STS-1 Serial Data.** If the device is operating in the serial mode, then RSTS1SERIAL is used as the input data pin.
1, 2, 21, 31, 51, 53, 54, 74, 79, 81, 84, 103, 105, 125, 135, 155, 157, 158, 177, 182, 187, 207	V_{SS}	I	**Ground Reference for Digital Circuitry.**
12, 26, 40, 52, 65, 69, 83, 93, 104, 111, 116, 121, 130, 144, 150, 168, 196	V_{DD}	I	**Power Supply for Digital Circuitry.**

* I^u indicates an internal pull-up.

DS1 to STS-1

In the descriptions below, some of the control bits exist for each of the DS1 or VT1.5 signals. These signals are indicated by x to show that there are actually 28 of them in the register map.

LOC and AIS Monitor

The incoming DS1 signal is first checked for loss of clock (LOC). AIS is reported to the microprocessor via the DS1LOCx bit (LOC = 1, 0 otherwise). If LOC is present, the device inserts DS1 AIS using the blue signal clock.

The incoming DS1 data (TDATA[28:1]) is retimed immediately by the associated DS1 clock (TCLK[28:1]). The edge of the clock that is used to retime the data is user provisionable at the device level to either the rising edge (TXDS1EDGE = 1) or falling edge (TXDS1EDGE = 0).

After being retimed, the incoming data stream is checked for AIS. The device will declare AIS if the input data is logic 1 for 3 ms. The device will withstand up to eight errors in the 3 ms period. AIS is reported to the microprocessor via the DS1AISx bit (AIS = 1, 0 otherwise).

The blue signal clock that is input to the device can be at the exact DS1 rate (1.544 MHz), or at 16 times the DS1 rate (24.704 MHz). This allows users of the Lucent Technologies T7690 devices to reuse the XCLK on the board. The TMPR28051 is provisioned to accept the exact DS1 rate by default (BLUECLKSEL = 0), but can be changed to perform the divide by 16 function (BLUECLKSEL = 1).

DS1 Loopback Select Logic

The first stage after retiming the signal into the device is selection of the received DS1 (DS1xLB = 0) or the looped back DS1 (DS1xLB = 1). This selection is provisionable per DS1 input (28 total).

Input Select Logic

Once the DS1 data sources have been selected, the DS1 for each VT1.5 tributary is selected. This selection requires 5 bits per slot to determine which DS1 input to use (DS1_xINS).

The numbering scheme for the five provisioned bits ranges from 00001 to 11100 where the binary value of the 5 bits corresponds to the DS1 input. For instance, the value 00001 corresponds to selecting DS1 #1.

The unused value of 00000 results in VT unequipped being transmitted. This is the default value for all the VT1.5 slots at powerup. VT unequipped is a valid pointer and all zero payload.

The unused values of 11101—11110 will cause AIS-V to be inserted for that VT1.5 slot. The value of 11111 will cause the internally generated test pattern to be inserted for that VT1.5 slot.

There are no restrictions on the number of VT1.5 slots that any given DS1 input can supply (i.e., up to 28 VT1.5 slots can select the same DS1 input).

This block can also be used to insert the test pattern (see Test Pattern DS1 Mode section on page 16).

Elastic Store

The selected DS1 clock and data signals are fed to an elastic store that is used to synchronize the incoming DS1 to the local STS-1 clock. This block determines the need for positive/zero/negative (P/Z/N) stuffing for each DS1. Data out of this block is synchronized to the local transmit STS-1 clock (TSTS1CLK).

This block allows the device to accept DS1 signals at 1.544 Mbits/s ± 130 ppm with up to ±5 unit intervals peak jitter.

VT1.5 Generate

This block generates the VT1.5 superframe. Unless AIS-V is being forced, the superframe is built with a fixed output pointer value of decimal 78 in all the VT1.5 slots. The VT size field is set to 11 and the new data flag is set to 0110. This corresponds to 0110110001001110 (0x6C4E) for the V1 and V2 bytes.

In this block, the DS1 data is placed into the VT1.5, and the VT1.5 overhead is generated. The format of the VT1.5 overhead byte, V5, is shown in Table 2.

Table 2. VT1.5 Overhead Byte Format (V5)

Bit #	1	2	3	4	5	6	7	8
	BIP-2		FEBE	RD1-V	Signal Label			RD1-V

Each VT1.5 can be provisioned to insert AIS-V (VTAISINSx = 1). AIS-V consists of overwriting the entire VT1.5 payload and overhead with ones.

DS1 to STS-1 (continued)

VT1.5 Generate (continued)

VTRDI-V (VTRDIx[1:0]INS) can be automatically inserted by the device or written into the V5 byte under control of the microprocessor. In the automatic mode, the value for bits 4 and 8 are defined in Table 3.

Table 3. RDI-V Description

Bit 4	Bit 8	Description
0	0	No alarm
0	1	AIS-V or LOP-V
1	0	VT payload mismatch
1	1	VT unequipped

The VT label for each VT1.5 is also provisionable (VTLAB[2:0]INSx) by the microprocessor.

This block also automatically generates the BIP-2 signal. Each VT1.5 can be configured to intentionally insert continuous BIP-2 errors for troubleshooting purposes (BIP2ERRINSx = 1). This control forces errors on both BIP-2 bits.

The device can be configured such that any detected BIP-2 errors in the VT1.5 receive side result in FEBE being written into the corresponding transmit VT1.5 slot (FEBE_EN = 1).

The resultant VT1.5 superframe is shown here:

V1
V5
RRRRRRIR
Byte 1
.
.
Byte 24
V2
RRRRRRRR
C1C2OOOOIR
Byte 1
.
.
Byte 24
V3
RRRRRRRR
C1C2OOOOIR
Byte 1
.
.
Byte 24
V4
RRRRRRRR
C1C2RRRS1S2R
Byte 1
.
.
Byte 24

Where:

I = information bit

O = overhead bit

R = fixed stuff

V1, V2, V3 = pointer and pointer action bytes

S1, S2 = stuff opportunity bits

V4 = reserved

C1, C2 = stuff indication bits

V5 = VT1.5 overhead byte

STS-1 Generate

The device generates an STS-1 signal based on an incoming clock (TSTS1CLK) and frame sync pulse (TSTS1SYNC). The relationship of the incoming frame sync pulse to the output frame can be provisioned such that the sync pulse occurs on either the first clock of the frame (TXFSYNC = 0) or the last clock of the frame (TXFSYNC = 1). In the absence of an incoming frame sync, the device will freewheel the output sync to the

DS1 to STS-1 (continued)

STS-1 Generate (continued)

last good frame sync pulse, or to the internal counter in the case that no sync pulses were supplied.

The SONET STS-1 frame is 9 rows x 90 columns that repeats at an 8 kHz rate. Each column is one byte wide. The SONET STS-1 frame contains three columns of transport overhead, one column of path overhead, and 86 columns of payload.

The 36 bytes of SONET overhead are allocated as shown in Table 4.

Table 4. STS-1 Overhead Byte Allocation

	Col. 1	Col. 2	Col. 3	Col. 4
Row 1	A1	A2	C1	J1
Row 2	B1	E1	F1	B3
Row 3	D1	D2	D3	C2
Row 4	H1	H2	H3	G1
Row 5	B2	K1	K2	F2
Row 6	D4	D5	D6	H4
Row 7	D7	D8	D9	Z3
Row 8	D10	D11	D12	Z4
Row 9	Z1	Z2	E2	Z5

The overhead bytes that are inserted by the device are described below. All of the remaining overhead bytes are given a fixed value of all zeros.

The device inserts the correct frame pattern of 0xF628 into the A1 and A2 bytes.

The device inserts a value of 0x01 into the C1 byte.

The device generates and inserts valid B1, B2, and B3 BIP-8 even parity bytes in the STS-1 overhead. These bytes are forced to odd parity when BxERRINS = 1.

The device will provide an STS-1 pointer with a fixed value of 522 with 0110 in the NDF bits and xx in the SS bits. This pointer value indicates that the J1 path overhead byte follows immediately after the C1 line overhead byte.

The J1 byte is used for path trace. This byte repetitively transmits a 64-byte fixed length sequence to verify end-to-end connectivity. These 64 bytes are programmable by the microprocessor (TJ1BYTEx). The method for programming these bits is described in detail in the Microprocessor Interface Register Architecture section on page 23.

The F2 byte can be provisioned by the microprocessor (F2INS[7:0]).

The device inserts a value of 0x02 into the C2 byte, indicating VT structured STS-1 SPE.

The 3 least significant bits of the K2 byte can be provisioned by the microprocessor (K2INS[2:0]).

The Z2 byte is used to report B2 FEBE when FEBE_EN = 1. These bits contain the number of errors seen by the current frames receive B2 BIP-8 when FEBE_EN = 1. Valid values for these 4 bits are 0000—1000.

The G1 byte is used to convey path condition and performance back to the far end. The format of the G1 byte is shown in Table 5.

Table 5. G1 Path Condition/Performance Byte Format

Bit #	1	2	3	4	5	6	7	8
	FEBE				RDI	Unused		

FEBE reports the number of far-end block errors. These bits contain the number of errors seen by the current frames receive B3 BIP-8 when FEBE_EN = 1. Valid values for these 4 bits are 0000—1000. The remote defect indicator (RDI-P) reports back such conditions as receive AIS-P, signal failure, and path trace mismatch.

The H4 byte is inserted using the reduced H4 coding sequence format where the 6 MSBs are ones and the 2 LSBs alternate between 00-01-10-11-00, etc. where the value of 00 indicates that the next STS-1 SPE contains the V1 overhead byte.

The STS-1 can be provisioned to send AIS-P (TXPAISINS = 1). Writing AIS-P consists of writing all ones into the H1—H3 bytes and the entire SPE.

The transmitted STS-1 can be configured to scramble the output data (STS1SCR = 1) or transmit the data without scrambling (STS1SCR = 0). It is useful to turn off SONET scrambling if the data is going to be immediately multiplexed into a higher rate SONET signal. When STS1SCR = 1, the device scrambles the outgoing STS-1 frame according to the SONET frame synchronous scrambling sequence $x^7 + x^6 + 1$. The sequence is reset to 1111111 at the beginning of the byte following the C1 byte and scrambles all of the STS-1 data except the A1, A2, and C1 bytes. When this bit is 0, then the transmit data is not scrambled by the device.

DS1 to STS-1 (continued)

SPE Insertion Logic

In addition to the one column of path overhead and 84 columns of VT1.5 payload, the STS-1 SPE also contains two columns of fixed stuff. The path overhead is located in column #1, while column #30 and column #59 contain the fixed stuff. The remaining columns contain the interleaved VT1.5 data as shown in Table 6.

Table 6. SPE Insertion Format

SPE Column #	1	2	3	4	5	6	7	8	9	10	11	•••	29	30	31	32	33	•••	57	58	59	60	61	•••	85	86	87	88	89	90	91	92	93
	PATH OH	VT1.5 #1	VT1.5 #2	VT1.5 #3	VT1.5 #4	VT1.5 #5	VT1.5 #6	VT1.5 #7	VT1.5 #8	VT1.5 #9	VT1.5 #10		VT1.5 #27	VT1.5 #28	FIXED	VT1.5 #1	VT1.5 #2		VT1.5 #27	VT1.5 #28	FIXED	VT1.5 #1	VT1.5 #2		VT1.5 #22	VT1.5 #23	VT1.5 #24	VT1.5 #25	VT1.5 #26	VT1.5 #27	VT1.5 #28

The mapping between the VT1.5 # listed above and the VT Group #, VT # listed in GR-253-CORE is:

Table 7. VT1.5 # to VT Group #, VT # Mapping

VT Group #, VT #	VT1.5 #	VT Group #, VT #	VT1.5 #	VT Group #, VT #	VT1.5 #	VT Group #, VT #	VT1.5 #
1, 1	1	1, 2	8	1, 3	15	1, 4	22
2, 1	2	2, 2	9	2, 3	16	2, 4	23
3, 1	3	3, 2	10	3, 3	17	3, 4	24
4, 1	4	4, 2	11	4, 3	18	4, 4	25
5, 1	5	5, 2	12	5, 3	19	5, 4	26
6, 1	6	6, 2	13	6, 3	20	6, 4	27
7, 1	7	7, 2	14	7, 3	21	7, 4	28

The SPE insertion logic block acts in conjunction with the STS-1 frame generate block to place the VT1.5 information in the transmitted data stream. The device can transmit the data as either a serial bit stream (TXSERIAL = 1) or as a parallel byte of data (TXSERIAL = 0). In the parallel mode, the device sends a parity bit with the data. This parity bit is configurable to be either odd (TXPARITY = 1) or even (TXPARITY = 0) parity.

STS-1 to DS1

Loopback Select Logic

The device can be configured to loopback the transmit STS-1 (STS1LB = 1) or accept the local STS-1 signal (STS1LB = 0). When the local STS-1 signal is selected, the user can configure which edge of the clock to use to retime the data (RXSTS1EDGE = 1 uses the rising edge; RXSTS1EDGE = 0 uses the falling edge).

STS-1 to DS1 (continued)

STS-1 Locate

The device can receive the data as either a serial bit stream (RXSERIAL = 1) or as a parallel byte of data (RXSERIAL = 0). In the parallel mode, the device receives a parity bit with the data. This bit is configurable to odd (RXPARITY = 1) or even (RXPARITY = 0) parity. Errors in this bit are reported to the microprocessor (RXPARERR). The bus mode of operation is the same as in the DS1 to STS-1 direction.

This block performs the functions necessary to locate the SPE. The device will frame on the incoming STS-1 signal, and indicate when it is in the out of frame (OOF) or loss of frame (LOF) conditions. Loss of frame is defined as being in the OOF condition for 3 ms or more. Both the OOF and LOF are latched conditions that hold their value until read. The indications will then reset if the condition is no longer true.

STS-1 Terminate

The received STS-1 can be configured to descramble the output data (STS1DSCR = 1) or receive the data without descrambling (STS1DSCR = 0). It is useful to turn off SONET descrambling if the data is received locally from a higher rate SONET signal where descrambling has already taken place.

For performance monitoring purposes, there are a number of BIP and FEBE error counters in the receive section. All of these internal counters are comprised of a running error counter and a hold register that presents stable results to the microprocessor. The counts in all of the running counters are latched to the hold registers when LATCH_CNT is written from a logic zero to a logic 1. This also zeros out all of the running counters. The results are then held to be read by the microprocessor. All of the internal counters have the ability to store more than one second worth of counts; as long as the LATCH_CNT occurs every second, or faster, no counts will be lost. In case this doesn't happen, all of the running counters will hold their maximum value rather than roll over to zero.

The device performs pointer interpretation on the incoming signal to locate the start of the SONET SPE. The pointer interpretation block will indicate when the device is in the loss of pointer (LOP-P) or path AIS (AIS-P) condition.

Loss of pointer condition is declared as the result of either of the following conditions:

1. Continuous NDF. If the device receives NDF (1001) for nine consecutive frames, then LOP-P is declared.
2. Invalid pointer values. If the device receives nine frames consecutively of a pointer that is not a normal value, NDF, AIS-P, increment, or decrement, then LOP-P is declared. The SS bits do not contribute to LOP-P.

AIS-P is declared on three consecutive frames with all ones in the H1 and H2 bytes.

AIS-P and LOP-P are mutually exclusive conditions. If neither STS1PAIS or STS1LOP is logic 1, then the pointer interpreter is declaring normal pointer. As part of the normal operation, the device will respond appropriately to valid NDF, increment and decrement indications. Increment and decrement operations will be counted by the device and presented to the microprocessor (INC[7:0], DEC[7:0]).

The B1, B2, and B3 BIP-8 values are recalculated and compared to the received values. Any differences are counted by the appropriate error counter (BxCNT[15:0]). In addition, B2 and B3 FEBE errors are also counted (BxFEBE[15:0]). The running and latched counts for both B1 and B2 counters are held at zero during OOF. The running and latched counts for B3 counters are held at zero during OOF as well as LOP-P.

The J1 byte is terminated within the device. This consists of writing the receive J1 value in a set of registers modulo 64. At start-up, the receive J1 byte register is all 0s. Whenever the received J1 byte value doesn't match the current J1 byte in the register, then the TRACE_MIS is set to logic 1. This allows the user to read the 64-byte register once, and then ignore it unless differences are received. TRACE_MIS is masked during AIS-P and LOP-P.

The F2 byte (F2[7:0]), the C2 byte (C2[7:0]), the three least significant bits of the K2 byte (K2[2:0]), and the four least significant bits of the G1 byte (G1[3:0]) are monitored by the microprocessor. The number of consistent, consecutive frames to update the values of all of these monitored bytes can be set by the user at anywhere between 3 and 15 frames (F2NxDET[3:0], C2NxDET[3:0], K2NxDET[3:0], G1NxDET[3:0]). None of these registers will update during OOF.

SPE Drop Logic

The SPE drop logic uses the H4 multiframe indicator to identify the V1 byte and drop the data to the correct VT1.5 termination blocks. Loss of multiframe synchronization will be reported to the microprocessor (H4LOMF).

STS-1 to DS1 (continued)

VT1.5 Terminate

The VT1.5 terminate block performs VT pointer interpretation on the received signal to locate the VT1.5 overhead. LOP-V (VTLOPx) and AIS-V (VTAISx) are reported to the microprocessor.

LOP-V is declared as a result of either of the following conditions:

1. Continuous NDF. If the device receives NDF (1001) for nine consecutive superframes, then LOP-V is declared.
2. Invalid pointer values. If the device receives nine frames consecutively of a pointer that is not a normal value, NDF, AIS-V, increment, or decrement, then LOP-V is declared. The SS bits **do** contribute to LOP-V.

AIS-V is declared on three consecutive frames with all ones in the V1 and V2 bytes.

AIS-V and LOP-V are mutually exclusive conditions. If neither VTAIS or VTLOP is logic 1, then the pointer interpreter is declaring normal pointer. As part of the normal operation, the device will respond appropriately to valid NDF, increment, and decrement indications. Increment and decrement operations will be counted by the device and presented to the microprocessor (VTx+[3:0], VTx–[3:0]).

Mismatches between the expected VT1.5 size bits, 11, and the actual received ss size bits are reported to the microprocessor (VTSIZEERx).

Once the V5 byte is located, the device checks for received BIP-2 errors (RXBIP2ERRx) and received FEBE (RXFEBEx). In addition to reporting the occurrence of BIP-2 errors and FEBE, the device also maintains a count of each of these on a per VT1.5 basis (FEBECNTx and BIP2CNTx). These running and latched counts for both BIP-2 and FEBE counters are held at zero during OOF, LOP-P, LOP-V, and AIS-V.

Additionally, the device checks for received RDI-V (VTRDIx[1:0]) and received VT label (VTLAB[2:0]x). Whenever the device receives three consecutive consistent values for these fields that are different from the current values, it latches the new value and reports the change to the microprocessor.

Output Select Logic

Once the VT1.5 has been terminated, the VT1.5 for each DS1 output is selected. This selection requires 5 bits per slot to determine which VT1.5 to use (VTx-DROP). The numbering scheme for the five provisioned bits ranges from 00001 to 11100; where the binary value of the 5 bits corresponds to the VT1.5 source. For instance, the value 00001 corresponds to selecting VT1.5 #1, group 1.

The unused values of 00000 and 11101—11110 will cause AIS to be inserted for that DS1 output. By default, on powerup all DS1 outputs reset to a value of 00000, which causes all of the DS1s to transmit AIS (all 1s) using the blue signal clock (BLUECLK).

The value of 11111 will insert the test pattern into the DS1 as described below.

Test Pattern DS1 Mode

The device contains a test pattern generator and a test pattern detector for use in maintenance and troubleshooting.

Test Pattern Generation

The test pattern generator is a QRSS sequence generator. The QRSS pattern is a $2^{20} - 1$ pseudorandom bit sequence defined by the equation $x^{20} + x^{17} + 1 = 0$, with a 14 zero limit. As can be seen in Figure 1 on page 6, this test pattern can be inserted in the place of any of the transmitted **or** received DS1 signals. Since the test pattern contains an unframed signal, it is only intended for use in maintenance and troubleshooting.

Test Pattern Detector

The test pattern detector contains a self-synchronizing detector using the identical QRSS sequence as found in the test pattern generator. When the detector is out of sync, the device continually monitors the input data signal for matches to the expected data signal. When the device detects 32 matches in a row, it declares itself in sync and the error detector is enabled. If the device detects eight consecutive mismatches, the test pattern detector declares itself out of sync and starts searching again.

While in sync, the device counts the number of times the input data differs from the expected data in a 7-bit counter that holds its count when it reaches the maximum value of 128. This counter is reset when read by the microprocessor, and is not affected by the LATCH_CNT bit that resets all of the other counters within the device.

Typical Uses DS1 Mode

Path Termination Multiplex

Using the device without internal loopbacks results in a SONET path terminating multiplex, as shown in Figure 3.

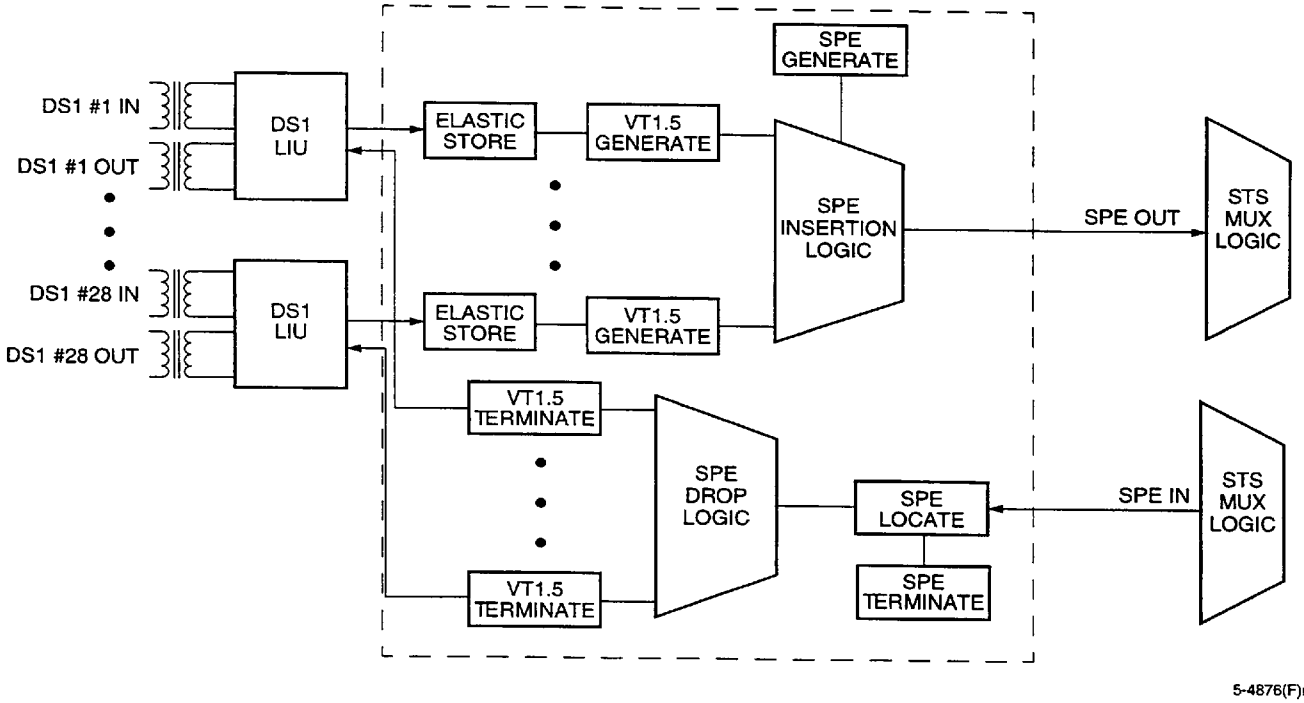

Figure 3. SONET Path Termination Multiplex Application

Typical Uses DS1 Mode (continued)

Add/Drop Multiplex

Using the device with DS1 internal loopbacks results in a SONET add/drop multiplex, as shown in Figure 4.

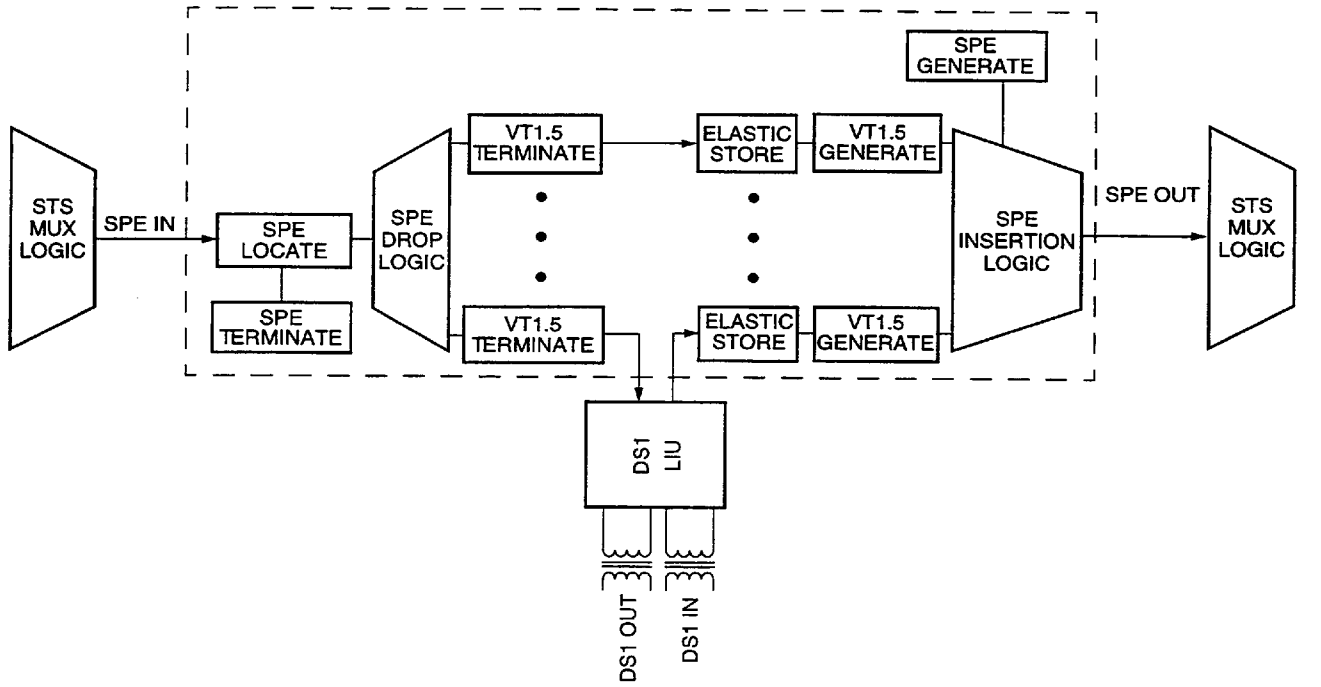

Figure 4. SONET Add/Drop Multiplex Application

Digital Cross Connect

Using the device with STS-1 internal loopbacks results in a digital cross connect, as shown in Figure 5.

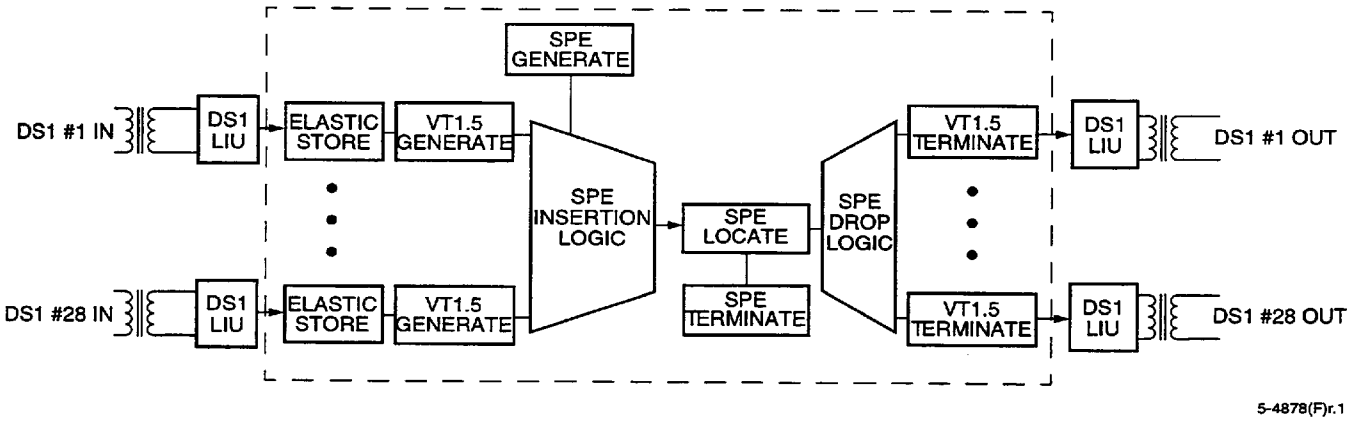

Figure 5. Digital Cross Connect Application

Typical Uses DS1 Mode (continued)

Test Pattern Use — Complete System

The internal test pattern generator can be used in conjunction with DS1 LIU devices that have built-in loopbacks (such as the Lucent T7690) to do a complete system test, as shown in Figure 6.

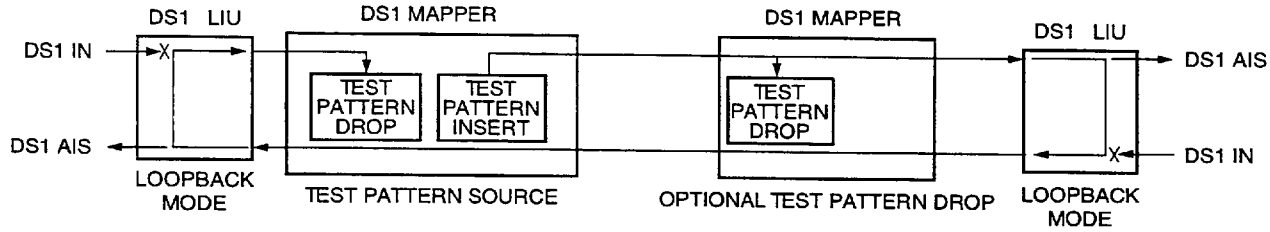

Figure 6. Test Pattern Usage for Complete System

Test Pattern Use — End to End

The internal test pattern generator can be used to test connectivity within a link by setting up a test pattern insert at one end and a drop at the other, as shown in Figure 7.

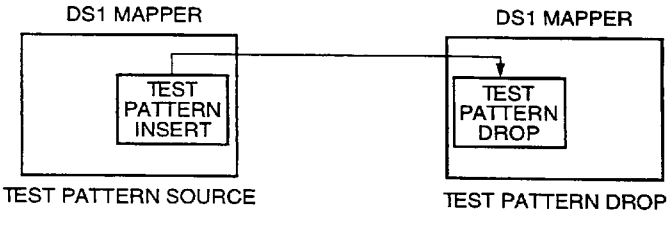

Figure 7. Test Pattern Usage for End-to-End Operation

Microprocessor Interface DS1 Mode

Overview

The device is equipped with an asynchronous microprocessor interface that allows operation with most commercially available microprocessors. Inputs MPMUX and MPMODE are used to configure this interface into one of four possible modes. The MPMUX setting selects either a multiplexed 8-bit address/data bus (AD[7:0]) or a demultiplexed 8-bit address bus (A[7:0]) and an 8-bit data bus (AD[7:0]). The MPMODE setting selects the associated set of registers within the device.

The microprocessor interface can operate at speeds up to 16.384 MHz in interrupt-driven or polled mode without requiring any wait-states. To conform to standards, there are a limited number of default powerup or reset states. All read/write registers must be written by the microprocessor on system start-up to guarantee proper device functionality.

Microprocessor Configuration Modes

Table 8 highlights the four microprocessor modes controlled by the MPMUX and MPMODE inputs.

Table 8. Microprocessor Configuration Modes

Mode	MPMODE	MPMUX	Address/Data Bus	Generic Control, Data, and Output Pin Names
Mode 1	0	0	DEMUXed	$\overline{CS}$, $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$, A[7:0], AD[7:0], INT, $\overline{DTACK}$
Mode 2	0	1	MUXed	$\overline{CS}$, $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$, AD[7:0], INT, $\overline{DTACK}$
Mode 3	1	0	DEMUXed	$\overline{CS}$, ALE, $\overline{RD}$, $\overline{WR}$, A[7:0], AD[7:0], INT, RDY
Mode 4	1	1	MUXed	$\overline{CS}$, ALE, $\overline{RD}$, $\overline{WR}$, AD[7:0], INT, RDY

Microprocessor Interface DS1 Mode (continued)

Microprocessor Interface Pinout Descriptions

The mode [1—4] specific pin definitions are given in Table 9. Note that the microprocessor interface uses the same set of pins in all modes.

Table 9. Mode [1—4] Microprocessor Pin Definitions

Configuration	Device Pin Name	Generic Pin Name	Pin Type	Assertion Sense	Function
Mode 1	$\overline{WR}\_\overline{DS}$	$\overline{DS}$	Input	Active-Low	Data Strobe
	$\overline{RD}\_R/\overline{W}$	$R/\overline{W}$	Input	—	Read/Write R/W = 1 for Read R/W = 0 for Write
	ALE_$\overline{AS}$	$\overline{AS}$	Input	—	Address Strobe
	$\overline{CS}$	$\overline{CS}$	Input	Active-Low	Chip Select
	INT	INT	Output	Active-High	Interrupt
	RDY_$\overline{DTACK}$	$\overline{DTACK}$	Output	Active-Low	Data Acknowledge
	AD[7:0)]	AD[7:0]	I/O	—	Data Bus
	A[7:0]	A[7:0]	Input	—	Address Bus
	MPCLK	MPCLK	Input	—	Microprocessor Clock
Mode 2	$\overline{WR}\_\overline{DS}$	$\overline{DS}$	Input	Active-Low	Data Strobe
	$\overline{RD}\_R/\overline{W}$	$R/\overline{W}$	Input	—	Read/Write R/W = 1 for Read R/W = 0 for Write
	ALE_$\overline{AS}$	$\overline{AS}$	Input	—	Address Strobe
	$\overline{CS}$	$\overline{CS}$	Input	Active-Low	Chip Select
	INT	INT	Output	Active-High	Interrupt
	RDY_$\overline{DTACK}$	$\overline{DTACK}$	Output	Active-Low	Data Acknowledge
	AD[7:0)]	AD[7:0]	I/O	—	Address/Data Bus
	MPCLK	MPCLK	Input	—	Microprocessor Clock

Microprocessor Interface DS1 Mode (continued)

Microprocessor Interface Pinout Descriptions (continued)

Table 9. Mode [1—4] Microprocessor Pin Definitions (continued)

Configuration	Device Pin Name	Generic Pin Name	Pin Type	Assertion Sense	Function
Mode 3	$\overline{WR}$_$\overline{DS}$	$\overline{WR}$	Input	Active-Low	Write
	$\overline{RD}$_R/$\overline{W}$	$\overline{RD}$	Input	—	Read
	ALE_$\overline{AS}$	ALE	Input	—	Address Latch Enable
	$\overline{CS}$	$\overline{CS}$	Input	Active-Low	Chip Select
	INT	INT	Output	Active-High	Interrupt
	RDY_$\overline{DTACK}$	RDY	Output	Active-Low	Ready
	AD[7:0)]	AD[7:0]	I/O	—	Data Bus
	A[7:0]	A[7:0]	Input	—	Address Bus
	MPCLK	MPCLK	Input	—	Microprocessor Clock
Mode 4	$\overline{WR}$_$\overline{DS}$	$\overline{WR}$	Input	Active-Low	Write
	$\overline{RD}$_R/$\overline{W}$	$\overline{RD}$	Input	—	Read
	ALE_$\overline{AS}$	ALE	Input	—	Address Latch Enable
	$\overline{CS}$	$\overline{CS}$	Input	Active-Low	Chip Select
	INT	INT	Output	Active-High	Interrupt
	RDY_$\overline{DTACK}$	RDY	Output	Active-Low	Ready
	AD[7:0)]	AD[7:0]	I/O	—	Address/Data Bus
	MPCLK	MPCLK	Input	—	Microprocessor Clock

Microprocessor Interface DS1 Mode (continued)

Microprocessor Interface Register Architecture

The register bank architecture of the microprocessor interface is shown in Table 10. All addresses referred to in this section are given in hexadecimal notation. Hexadecimal is the first column under Address.

Table 10. Device-Level Control, Alarm, and Mask Bits Register Set

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	00000000	TEST_CNT	B1ERRINS	B2ERRINS	B3ERRINS	LATCH_CNT	BLUECLKSEL	BIP2BLKCNT	RESET
01	00000001	FEBE_EN	0	TXPAISINS	0	TXFSYNC	STS1SCR	STS1DSCR	STS1LB
02	00000010	RXSERIAL	TXSERIAL	RXPARITY	TXPARITY	RXSTS1EDGE	TXSTS1EDGE	RXDS1EDGE	TXDS1EDGE
03	00000011	TRACEER	RXPARER	0	H4LOMF	STS1PAIS	STS1LOP	STS1LOF	STS1OOF
04	00000100	TRACEERMSK	RXPARERMSK	0	H4LOMFMSK	STS1PAISMSK	STS1LOPMSK	STS1LOFMSK	STS1OOFMSK
05	00000101	ESOFCOM	VTSIZECOM	VTLOPCOM	VTRDICOM	VTAISCOM	VTLABCOM	DS1LOCCOM	DS1AISCOM
06	00000110	ESOFMSK	VTSIZEMSK	VTLOPMSK	VTRDIMSK	VTAISMSK	VTLABMSK	DS1LOCMSK	DS1AISMSK
07	00000111	0	0	0	0	0	0	0	DS1_E1N
08	00001000	0	0	0	0	0	0	0	0
09	00001001	0	0	TPDROPSIDE	TPDROP4	TPDROP3	TPDROP2	TPDROP1	TPDROP0
0A	00001010	TPOOS	TPERR6	TPERR5	TPERR4	TPERR3	TPERR2	TPERR1	TPERR0
0B	00001011	F2-7	F2-6	F2-5	F2-4	F2-3	F2-2	F2-1	F2-0
0C	00001100	C2-7	C2-6	C2-5	C2-4	C2-3	C2-2	C2-1	C2-0
0D	00001101	G1-3	G1-2	G1-1	G1-0	0	K2-2	K2-1	K2-0
0E	00001110	C2NxDET3	C2NxDET2	C2NxDET1	C2NxDET0	F2NxDET3	F2NxDET2	F2NxDET1	F2NxDET0
0F	00001111	G1NxDET3	G1NxDET2	G1NxDET1	G1NxDET0	K2NxDET3	K2NxDET2	K2NxDET1	K2NxDET0
10	00010000	F2INS-7	F2INS-6	F2INS-5	F2INS-4	F2INS-3	F2INS-2	F2INS-1	F2INS-0
11	00010001	G1INS-3	G1INS-2	G1INS-1	G1INS-0	0	K2INS-2	K2INS-1	K2INS-0
12	00010010	0	0	0	0	0	0	0	0
13	00010011	0	0	0	0	0	0	0	0
14	00010100	0	0	0	0	0	0	0	0
15	00010101	0	0	0	0	0	0	0	0

Microprocessor Interface DS1 Mode (continued)

Microprocessor Interface Register Architecture (continued)

Table 10. Device-Level Control, Alarm, and Mask Bits Register Set (continued)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
16	00010110	0	0	0	0	0	0	0	0
17	00010111	DS1AIS1	DS1LOC1	DS11LB	DS1_1INS4	DS1_1INS3	DS1_1INS2	DS1_1INS1	DS1_1INS0
18	00011000	DS1AIS2	DS1LOC2	DS12LB	DS1_2INS4	DS1_2INS3	DS1_2INS2	DS1_2INS1	DS1_2INS0
19	00011001	DS1AIS3	DS1LOC3	DS13LB	DS1_3INS4	DS1_3INS3	DS1_3INS2	DS1_3INS1	DS1_3INS0
1A	00011010	DS1AIS4	DS1LOC4	DS14LB	DS1_4INS4	DS1_4INS3	DS1_4INS2	DS1_4INS1	DS1_4INS0
1B	00011011	DS1AIS5	DS1LOC5	DS15LB	DS1_5INS4	DS1_5INS3	DS1_5INS2	DS1_5INS1	DS1_5INS0
1C	00011100	DS1AIS6	DS1LOC6	DS16LB	DS1_6INS4	DS1_6INS3	DS1_6INS2	DS1_6INS1	DS1_6INS0
1D	00011101	DS1AIS7	DS1LOC7	DS17LB	DS1_7INS4	DS1_7INS3	DS1_7INS2	DS1_7INS1	DS1_7INS0
1E	00011110	DS1AIS8	DS1LOC8	DS18LB	DS1_8INS4	DS1_8INS3	DS1_8INS2	DS1_8INS1	DS1_8INS0
1F	00011111	DS1AIS9	DS1LOC9	DS19LB	DS1_9INS4	DS1_9INS3	DS1_9INS2	DS1_9INS1	DS1_9INS0
20	00100000	DS1AIS10	DS1LOC10	DS110LB	DS1_10INS4	DS1_10INS3	DS1_10INS2	DS1_10INS1	DS1_10INS0
21	00100001	DS1AIS11	DS1LOC11	DS111LB	DS1_11INS4	DS1_11INS3	DS1_11INS2	DS1_11INS1	DS1_11INS0
22	00100010	DS1AIS12	DS1LOC12	DS112LB	DS1_12INS4	DS1_12INS3	DS1_12INS2	DS1_12INS1	DS1_12INS0
23	00100011	DS1AIS13	DS1LOC13	DS113LB	DS1_13INS4	DS1_13INS3	DS1_13INS2	DS1_13INS1	DS1_13INS0
24	00100100	DS1AIS14	DS1LOC14	DS114LB	DS1_14INS4	DS1_14INS3	DS1_14INS2	DS1_14INS1	DS1_14INS0
25	00100101	DS1AIS15	DS1LOC15	DS115LB	DS1_15INS4	DS1_15INS3	DS1_15INS2	DS1_15INS1	DS1_15INS0
26	00100110	DS1AIS16	DS1LOC16	DS116LB	DS1_16INS4	DS1_16INS3	DS1_16INS2	DS1_16INS1	DS1_16INS0
27	00100111	DS1AIS17	DS1LOC17	DS117LB	DS1_17INS4	DS1_17INS3	DS1_17INS2	DS1_17INS1	DS1_17INS0
28	00101000	DS1AIS18	DS1LOC18	DS118LB	DS1_18INS4	DS1_18INS3	DS1_18INS2	DS1_18INS1	DS1_18INS0
29	00101001	DS1AIS19	DS1LOC19	DS119LB	DS1_19INS4	DS1_19INS3	DS1_19INS2	DS1_19INS1	DS1_19INS0
2A	00101010	DS1AIS20	DS1LOC20	DS120LB	DS1_20INS4	DS1_20INS3	DS1_20INS2	DS1_20INS1	DS1_20INS0
2B	00101011	DS1AIS21	DS1LOC21	DS121LB	DS1_21INS4	DS1_21INS3	DS1_21INS2	DS1_21INS1	DS1_21INS0
2C	00101100	DS1AIS22	DS1LOC22	DS122LB	DS1_22INS4	DS1_22INS3	DS1_22INS2	DS1_22INS1	DS1_22INS0
2D	00101101	DS1AIS23	DS1LOC23	DS123LB	DS1_23INS4	DS1_23INS3	DS1_23INS2	DS1_23INS1	DS1_23INS0
2E	00101110	DS1AIS24	DS1LOC24	DS124LB	DS1_24INS4	DS1_24INS3	DS1_24INS2	DS1_24INS1	DS1_24INS0
2F	00101111	DS1AIS25	DS1LOC25	DS125LB	DS1_25INS4	DS1_25INS3	DS1_25INS2	DS1_25INS1	DS1_25INS0
30	00110000	DS1AIS26	DS1LOC26	DS126LB	DS1_26INS4	DS1_26INS3	DS1_26INS2	DS1_26INS1	DS1_26INS0
31	00110001	DS1AIS27	DS1LOC27	DS127LB	DS1_27INS4	DS1_27INS3	DS1_27INS2	DS1_27INS1	DS1_27INS0
32	00110010	DS1AIS28	DS1LOC28	DS128LB	DS1_28INS4	DS1_28INS3	DS1_28INS2	DS1_28INS1	DS1_28INS0
33	00110011	0	RXESOF1	TXESOF1	VT_1DROP4	VT_1DROP3	VT_1DROP2	VT_1DROP1	VT_1DROP0
34	00110100	0	RXESOF2	TXESOF2	VT_2DROP4	VT_2DROP3	VT_2DROP2	VT_2DROP1	VT_2DROP0
35	00110101	0	RXESOF3	TXESOF3	VT_3DROP4	VT_3DROP3	VT_3DROP2	VT_3DROP1	VT_3DROP0
36	00110110	0	RXESOF4	TXESOF4	VT_4DROP4	VT_4DROP3	VT_4DROP2	VT_4DROP1	VT_4DROP0
37	00110111	0	RXESOF5	TXESOF5	VT_5DROP4	VT_5DROP3	VT_5DROP2	VT_5DROP1	VT_5DROP0
38	00111000	0	RXESOF6	TXESOF6	VT_6DROP4	VT_6DROP3	VT_6DROP2	VT_6DROP1	VT_6DROP0
39	00111001	0	RXESOF7	TXESOF7	VT_7DROP4	VT_7DROP3	VT_7DROP2	VT_7DROP1	VT_7DROP0
3A	00111010	0	RXESOF8	TXESOF8	VT_8DROP4	VT_8DROP3	VT_8DROP2	VT_8DROP1	VT_8DROP0
3B	00111011	0	RXESOF9	TXESOF9	VT_9DROP4	VT_9DROP3	VT_9DROP2	VT_9DROP1	VT_9DROP0
3C	00111100	0	RXESOF10	TXESOF10	VT_10DROP4	VT_10DROP3	VT_10DROP2	VT_10DROP1	VT_10DROP0
3D	00111101	0	RXESOF11	TXESOF11	VT_11DROP4	VT_11DROP3	VT_11DROP2	VT_11DROP1	VT_11DROP0
3E	00111110	0	RXESOF12	TXESOF12	VT_12DROP4	VT_12DROP3	VT_12DROP2	VT_12DROP1	VT_12DROP0
3F	00111111	0	RXESOF14	TXESOF13	VT_13DROP4	VT_13DROP3	VT_13DROP2	VT_13DROP1	VT_13DROP0

Microprocessor Interface DS1 Mode (continued)

Microprocessor Interface Register Architecture (continued)

Table 10. Device-Level Control, Alarm, and Mask Bits Register Set (continued)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
40	01000000	0	RXESOF14	TXESOF14	VT_14DROP4	VT_14DROP3	VT_14DROP2	VT_14DROP1	VT_14DROP0
41	01000001	0	RXESOF15	TXESOF15	VT_15DROP4	VT_15DROP3	VT_15DROP2	VT_15DROP1	VT_15DROP0
42	01000010	0	RXESOF16	TXESOF16	VT_16DROP4	VT_16DROP3	VT_16DROP2	VT_16DROP1	VT_16DROP0
43	01000011	0	RXESOF17	TXESOF17	VT_17DROP4	VT_17DROP3	VT_17DROP2	VT_17DROP1	VT_17DROP0
44	01000100	0	RXESOF18	TXESOF18	VT_18DROP4	VT_18DROP3	VT_18DROP2	VT_18DROP1	VT_18DROP0
45	01000101	0	RXESOF19	TXESOF19	VT_19DROP4	VT_19DROP3	VT_19DROP2	VT_19DROP1	VT_19DROP0
46	01000110	0	RXESOF20	TXESOF20	VT_20DROP4	VT_20DROP3	VT_20DROP2	VT_20DROP1	VT_20DROP0
47	01000111	0	RXESOF21	TXESOF21	VT_21DROP4	VT_21DROP3	VT_21DROP2	VT_21DROP1	VT_21DROP0
48	01001000	0	RXESOF22	TXESOF22	VT_22DROP4	VT_22DROP3	VT_22DROP2	VT_22DROP1	VT_22DROP0
49	01001001	0	RXESOF23	TXESOF23	VT_23DROP4	VT_23DROP3	VT_23DROP2	VT_23DROP1	VT_23DROP0
4A	01001010	0	RXESOF24	TXESOF24	VT_24DROP4	VT_24DROP3	VT_24DROP2	VT_24DROP1	VT_24DROP0
4B	01001011	0	RXESOF25	TXESOF25	VT_25DROP4	VT_25DROP3	VT_25DROP2	VT_25DROP1	VT_25DROP0
4C	01001100	0	RXESOF26	TXESOF26	VT_26DROP4	VT_26DROP3	VT_26DROP2	VT_26DROP1	VT_26DROP0
4D	01001101	0	RXESOF27	TXESOF27	VT_27DROP4	VT_27DROP3	VT_27DROP2	VT_27DROP1	VT_27DROP0
4E	01001110	0	RXESOF28	TXESOF28	VT_28DROP4	VT_28DROP3	VT_28DROP2	VT_28DROP1	VT_28DROP0
4F	01001111	BIP2ERINS1	VTRDI1_EN	VTRDI1_INS1	VTRDI1_INS0	VTAISINS1	VTLAB2INS1	VTLAB1INS1	VTLAB0INS1
50	01010000	BIP2ERINS2	VTRDI2_EN	VTRDI2_INS1	VTRDI2_INS0	VTAISINS2	VTLAB2INS2	VTLAB1INS2	VTLAB0INS2
51	01010001	BIP2ERINS3	VTRDI3_EN	VTRDI3_INS1	VTRDI3_INS0	VTAISINS3	VTLAB2INS3	VTLAB1INS3	VTLAB0INS3
52	01010010	BIP2ERINS4	VTRDI4_EN	VTRDI4_INS1	VTRDI4_INS0	VTAISINS4	VTLAB2INS4	VTLAB1INS4	VTLAB0INS4
53	01010011	BIP2ERINS5	VTRDI5_EN	VTRDI5_INS1	VTRDI5_INS0	VTAISINS5	VTLAB2INS5	VTLAB1INS5	VTLAB0INS5
54	01010100	BIP2ERINS6	VTRDI6_EN	VTRDI6_INS1	VTRDI6_INS0	VTAISINS6	VTLAB2INS6	VTLAB1INS6	VTLAB0INS6
55	01010101	BIP2ERINS7	VTRDI7_EN	VTRDI7_INS1	VTRDI7_INS0	VTAISINS7	VTLAB2INS7	VTLAB1INS7	VTLAB0INS7
56	01010110	BIP2ERINS8	VTRDI8_EN	VTRDI8_INS1	VTRDI8_INS0	VTAISINS8	VTLAB2INS8	VTLAB1INS8	VTLAB0INS8
57	01010111	BIP2ERINS9	VTRDI9_EN	VTRDI9_INS1	VTRDI9_INS0	VTAISINS9	VTLAB2INS9	VTLAB1INS9	VTLAB0INS9
58	01011000	BIP2ERINS10	VTRDI10_EN	VTRDI10_INS1	VTRDI10_INS0	VTAISINS10	VTLAB2INS10	VTLAB1INS10	VTLAB0INS10
59	01011001	BIP2ERINS11	VTRDI11_EN	VTRDI11_INS1	VTRDI11_INS0	VTAISINS11	VTLAB2INS11	VTLAB1INS11	VTLAB0INS11
5A	01011010	BIP2ERINS12	VTRDI12_EN	VTRDI12_INS1	VTRDI12_INS0	VTAISINS12	VTLAB2INS12	VTLAB1INS12	VTLAB0INS12
5B	01011011	BIP2ERINS13	VTRDI13_EN	VTRDI13_INS1	VTRDI13_INS0	VTAISINS13	VTLAB2INS13	VTLAB1INS13	VTLAB0INS13
5C	01011100	BIP2ERINS14	VTRDI14_EN	VTRDI14_INS1	VTRDI14_INS0	VTAISINS14	VTLAB2INS14	VTLAB1INS14	VTLAB0INS14
5D	01011101	BIP2ERINS15	VTRDI15_EN	VTRDI15_INS1	VTRDI15_INS0	VTAISINS15	VTLAB2INS15	VTLAB1INS15	VTLAB0INS15
5E	01011110	BIP2ERINS16	VTRDI16_EN	VTRDI16_INS1	VTRDI16_INS0	VTAISINS16	VTLAB2INS16	VTLAB1INS16	VTLAB0INS16
5F	01011111	BIP2ERINS17	VTRDI17_EN	VTRDI17_INS1	VTRDI17_INS0	VTAISINS17	VTLAB2INS17	VTLAB1INS17	VTLAB0INS17
60	01100000	BIP2ERINS18	VTRDI18_EN	VTRDI18_INS1	VTRDI18_INS0	VTAISINS18	VTLAB2INS18	VTLAB1INS18	VTLAB0INS18
61	01100001	BIP2ERINS19	VTRDI19_EN	VTRDI19_INS1	VTRDI19_INS0	VTAISINS19	VTLAB2INS19	VTLAB1INS19	VTLAB0INS19
62	01100010	BIP2ERINS20	VTRDI20_EN	VTRDI20_INS1	VTRDI20_INS0	VTAISINS20	VTLAB2INS20	VTLAB1INS20	VTLAB0INS20
63	01100011	BIP2ERINS21	VTRDI21_EN	VTRDI21_INS1	VTRDI21_INS0	VTAISINS21	VTLAB2INS21	VTLAB1INS21	VTLAB0INS21
64	01100100	BIP2ERINS22	VTRDI22_EN	VTRDI22_INS1	VTRDI22_INS0	VTAISINS22	VTLAB2INS22	VTLAB1INS22	VTLAB0INS22
65	01100101	BIP2ERINS23	VTRDI23_EN	VTRDI23_INS1	VTRDI23_INS0	VTAISINS23	VTLAB2INS23	VTLAB1INS23	VTLAB0INS23
66	01100110	BIP2ERINS24	VTRDI24_EN	VTRDI24_INS1	VTRDI24_INS0	VTAISINS24	VTLAB2INS24	VTLAB1INS24	VTLAB0INS24
67	01100111	BIP2ERINS25	VTRDI25_EN	VTRDI25_INS1	VTRDI25_INS0	VTAISINS25	VTLAB2INS25	VTLAB1INS25	VTLAB0INS25
68	01101000	BIP2ERINS26	VTRDI26_EN	VTRDI26_INS1	VTRDI26_INS0	VTAISINS26	VTLAB2INS26	VTLAB1INS26	VTLAB0INS26
69	01101001	BIP2ERINS27	VTRDI27_EN	VTRDI27_INS1	VTRDI27_INS0	VTAISINS27	VTLAB2INS27	VTLAB1INS27	VTLAB0INS27

Microprocessor Interface DS1 Mode (continued)

Microprocessor Interface Register Architecture (continued)

Table 10. Device-Level Control, Alarm, and Mask Bits Register Set (continued)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
6A	01101010	BIP2ERINS28	VTRDI28_EN	VTRDI28_INS1	VTRDI28_INS0	VTAISINS28	VTLAB2INS28	VTLAB1INS28	VTLAB0INS28
6B	01101011	VTSIZEER1	VTLOP1	VTRDI11	VTRDI10	VTAIS1	VTLAB21	VTLAB11	VTLAB01
6C	01101100	VTSIZEER2	VTLOP2	VTRDI21	VTRDI20	VTAIS2	VTLAB22	VTLAB12	VTLAB02
6D	01101101	VTSIZEER3	VTLOP3	VTRDI31	VTRDI30	VTAIS3	VTLAB23	VTLAB13	VTLAB03
6E	01101110	VTSIZEER4	VTLOP4	VTRDI41	VTRDI40	VTAIS4	VTLAB24	VTLAB14	VTLAB04
6F	01101111	VTSIZEER5	VTLOP5	VTRDI51	VTRDI50	VTAIS5	VTLAB25	VTLAB15	VTLAB05
70	01110000	VTSIZEER6	VTLOP6	VTRDI61	VTRDI60	VTAIS6	VTLAB26	VTLAB16	VTLAB06
71	01110001	VTSIZEER7	VTLOP7	VTRDI71	VTRDI70	VTAIS7	VTLAB27	VTLAB17	VTLAB07
72	01110010	VTSIZEER8	VTLOP8	VTRDI81	VTRDI80	VTAIS8	VTLAB28	VTLAB18	VTLAB08
73	01110011	VTSIZEER9	VTLOP9	VTRDI91	VTRDI90	VTAIS9	VTLAB29	VTLAB19	VTLAB09
74	01110100	VTSIZEER10	VTLOP10	VTRDI101	VTRDI100	VTAIS10	VTLAB210	VTLAB110	VTLAB010
75	01110101	VTSIZEER11	VTLOP11	VTRDI111	VTRDI110	VTAIS11	VTLAB211	VTLAB111	VTLAB011
76	01110110	VTSIZEER12	VTLOP12	VTRDI121	VTRDI120	VTAIS12	VTLAB212	VTLAB112	VTLAB012
77	01110111	VTSIZEER13	VTLOP13	VTRDI131	VTRDI130	VTAIS13	VTLAB213	VTLAB113	VTLAB013
78	01111000	VTSIZEER14	VTLOP14	VTRDI141	VTRDI140	VTAIS14	VTLAB214	VTLAB114	VTLAB014
79	01111001	VTSIZEER15	VTLOP15	VTRDI151	VTRDI150	VTAIS15	VTLAB215	VTLAB115	VTLAB015
7A	01111010	VTSIZEER16	VTLOP16	VTRDI161	VTRDI160	VTAIS16	VTLAB216	VTLAB116	VTLAB016
7B	01111011	VTSIZEER17	VTLOP17	VTRDI171	VTRDI170	VTAIS17	VTLAB217	VTLAB117	VTLAB017
7C	01111100	VTSIZEER18	VTLOP18	VTRDI181	VTRDI180	VTAIS18	VTLAB218	VTLAB118	VTLAB018
7D	01111101	VTSIZEER19	VTLOP19	VTRDI191	VTRDI190	VTAIS19	VTLAB219	VTLAB119	VTLAB019
7E	01111110	VTSIZEER20	VTLOP20	VTRDI201	VTRDI200	VTAIS20	VTLAB220	VTLAB120	VTLAB020
7F	01111111	VTSIZEER21	VTLOP21	VTRDI211	VTRDI210	VTAIS21	VTLAB221	VTLAB121	VTLAB021
80	10000000	VTSIZEER22	VTLOP22	VTRDI221	VTRDI220	VTAIS22	VTLAB222	VTLAB122	VTLAB022
81	10000001	VTSIZEER23	VTLOP23	VTRDI231	VTRDI230	VTAIS23	VTLAB223	VTLAB123	VTLAB023
82	10000010	VTSIZEER24	VTLOP24	VTRDI241	VTRDI240	VTAIS24	VTLAB224	VTLAB124	VTLAB024
83	10001000	VTSIZEER25	VTLOP25	VTRDI251	VTRDI250	VTAIS25	VTLAB225	VTLAB125	VTLAB025
84	10000100	VTSIZEER26	VTLOP26	VTRDI261	VTRDI260	VTAIS26	VTLAB226	VTLAB126	VTLAB026
85	10000101	VTSIZEER27	VTLOP27	VTRDI271	VTRDI270	VTAIS27	VTLAB227	VTLAB127	VTLAB027
86	10000110	VTSIZEER28	VTLOP28	VTRDI281	VTRDI280	VTAIS28	VTLAB228	VTLAB128	VTLAB028
87	10000111	0	0	0	0	0	0	0	0
88	10001000	0	0	0	0	0	0	0	0
89	10001001	0	0	0	0	0	0	0	0
8A	10001010	0	0	0	0	0	0	0	0
8B	10001011	0	0	0	0	0	0	0	0
8C	10001100	0	0	0	0	0	0	0	0
8D	10001101	0	0	0	0	0	0	0	0
8E	10001110	0	0	0	0	0	0	0	0
8F	10001111	0	0	0	0	0	0	0	0

Microprocessor Interface DS1 Mode (continued)

Microprocessor Interface Register Architecture (continued)

Table 10. Device-Level Control, Alarm, and Mask Bits Register Set (continued)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
90	10010000	0	0	0	0	0	0	0	0
91	10010001	0	0	0	0	0	0	0	0
92	10010010	0	0	0	0	0	0	0	0
93	10010011	0	0	0	0	0	0	0	0
94	10010100	0	0	0	0	0	0	0	0
95	10010101	0	0	0	0	0	0	0	0
96	10010110	0	0	0	0	0	0	0	0
97	10010111	0	0	0	0	0	0	0	0
98	10011000	0	0	0	0	0	0	0	0
99	10011001	0	0	0	0	0	0	0	0
9A	10011010	0	0	0	0	0	0	0	0
9B	10011011	0	0	0	0	0	0	0	0
9C	10011100	0	0	0	0	0	0	0	0
9D	10011101	0	0	0	0	0	0	0	0
9E	10011110	0	0	0	0	0	0	0	0
9F	10011111	0	0	0	0	0	0	0	0
A0	10100000	0	0	0	0	0	0	0	0
A1	10100001	0	0	0	0	0	0	0	0
A2	10100010	0	0	0	0	0	0	0	0
A3	10100011	0	0	0	0	0	0	0	0
A4	10100100	0	0	0	0	0	0	0	0
A5	10100101	0	0	0	0	0	0	0	0
A6	10100110	0	0	0	0	0	0	0	0
A7	10100111	0	0	0	0	0	0	0	0
A8	10101000	0	0	0	0	0	0	0	0
A9	10101001	0	0	0	0	0	0	0	0
AA	10101010	0	0	0	0	0	0	0	0
AB	10101011	0	0	0	0	0	0	0	0
AC	10101100	0	0	0	0	0	0	0	0
AD	10101101	0	0	0	0	0	0	0	0
AE	10101110	0	0	0	0	0	0	0	0
AF	10101111	0	0	0	0	0	0	0	0
B0	10110000	0	0	0	0	0	0	0	0
B1	10110001	0	0	0	0	0	0	0	0
B2	10110010	0	0	0	0	0	0	0	0
B3	10110011	0	0	0	0	0	0	0	0
B4	10110100	0	0	0	0	0	0	0	0
B5	10110101	0	0	0	0	0	0	0	0
B6	10110110	0	0	0	0	0	0	0	0
B7	10110111	0	0	0	0	0	0	0	0
B8	10111000	0	0	0	0	0	0	0	0
B9	10111001	0	0	0	0	0	0	0	0

Microprocessor Interface DS1 Mode (continued)

Microprocessor Interface Register Architecture (continued)

Table 10. Device-Level Control, Alarm, and Mask Bits Register Set (continued)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BA	10111010	0	0	0	0	0	0	0	0
BB	10111011	0	0	0	0	0	0	0	0
BC	10111100	0	0	0	0	0	0	0	0
BD	10111101	0	0	0	0	0	0	0	0
BE	10111110	0	0	0	0	0	0	0	0
BF	10111111	0	0	0		TJ1BYTE	RJ1BYTE	FEBE_CNTS	BIP_CNTS
When BIP_CNTS = 1									
C0	11000000	B1BIPCNT15	B1BIPCNT14	B1BIPCNT13	B1BIPCNT12	B1BIPCNT11	B1BIPCNT10	B1BIPCNT9	B1BIPCNT8
C1	11000001	B1BIPCNT7	B1BIPCNT6	B1BIPCNT5	B1BIPCNT4	B1BIPCNT3	B1BIPCNT2	B1BIPCNT1	B1BIPCNT0
C2	11000010	B2BIPCNT15	B2BIPCNT14	B2BIPCNT13	B2BIPCNT12	B2BIPCNT11	B2BIPCNT10	B2BIPCNT9	B2BIPCNT8
C3	11000011	B2BIPCNT7	B2BIPCNT6	B2BIPCNT5	B2BIPCNT4	B2BIPCNT3	B2BIPCNT2	B2BIPCNT1	B2BIPCNT0
C4	11000100	B3BIPCNT15	B3BIPCNT14	B3BIPCNT13	B3BIPCNT12	B3BIPCNT11	B3BIPCNT10	B3BIPCNT9	B3BIPCNT8
C5	11000101	B3BIPCNT7	B3BIPCNT6	B3BIPCNT5	B3BIPCNT4	B3BIPCNT3	B3BIPCNT2	B3BIPCNT1	B3BIPCNT0
C6	11000110	VT1PTR+3	VT1PTR+2	VT1PTR+1	VT1PTR+0	BIP2CNT111	BIP2CNT101	BIP2CNT91	BIP2CNT81
C7	11000111	BIP2CNT71	BIP2CNT61	BIP2CNT51	BIP2CNT41	BIP2CNT31	BIP2CNT21	BIP2CNT11	BIP2CNT01
C8	11001000	VT2PTR+3	VT2PTR+2	VT2PTR+1	VT2PTR+0	BIP2CNT112	BIP2CNT102	BIP2CNT92	BIP2CNT82
C9	11001001	BIP2CNT72	BIP2CNT62	BIP2CNT52	BIP2CNT42	BIP2CNT32	BIP2CNT22	BIP2CNT12	BIP2CNT02
CA	11001010	VT3PTR+3	VT3PTR+2	VT3PTR+1	VT3PTR+0	BIP2CNT113	BIP2CNT103	BIP2CNT93	BIP2CNT83
CB	11001011	BIP2CNT73	BIP2CNT63	BIP2CNT53	BIP2CNT43	BIP2CNT33	BIP2CNT23	BIP2CNT13	BIP2CNT03
CC	11001100	VT4PTR+3	VT4PTR+2	VT4PTR+1	VT4PTR+0	BIP2CNT114	BIP2CNT104	BIP2CNT94	BIP2CNT84
CD	11001101	BIP2CNT74	BIP2CNT64	BIP2CNT54	BIP2CNT44	BIP2CNT34	BIP2CNT24	BIP2CNT14	BIP2CNT04
CE	11001110	VT5PTR+3	VT5PTR+2	VT5PTR+1	VT5PTR+0	BIP2CNT115	BIP2CNT105	BIP2CNT95	BIP2CNT85
CF	11001111	BIP2CNT75	BIP2CNT65	BIP2CNT55	BIP2CNT45	BIP2CNT35	BIP2CNT25	BIP2CNT15	BIP2CNT05
D0	11010000	VT6PTR+3	VT6PTR+2	VT6PTR+1	VT6PTR+0	BIP2CNT116	BIP2CNT106	BIP2CNT96	BIP2CNT86
D1	11010001	BIP2CNT76	BIP2CNT66	BIP2CNT56	BIP2CNT46	BIP2CNT36	BIP2CNT26	BIP2CNT16	BIP2CNT06
D2	11010010	VT7PTR+3	VT7PTR+2	VT7PTR+1	VT7PTR+0	BIP2CNT117	BIP2CNT107	BIP2CNT97	BIP2CNT87
D3	11010011	BIP2CNT77	BIP2CNT67	BIP2CNT57	BIP2CNT47	BIP2CNT37	BIP2CNT27	BIP2CNT17	BIP2CNT07
D4	11010100	VT8PTR+3	VT8PTR+2	VT8PTR+1	VT8PTR+0	BIP2CNT118	BIP2CNT108	BIP2CNT98	BIP2CNT88
D5	11010101	BIP2CNT78	BIP2CNT68	BIP2CNT58	BIP2CNT48	BIP2CNT38	BIP2CNT28	BIP2CNT18	BIP2CNT08
D6	11010110	VT9PTR+3	VT9PTR+2	VT9PTR+1	VT9PTR+0	BIP2CNT119	BIP2CNT109	BIP2CNT99	BIP2CNT89
D7	11010111	BIP2CNT79	BIP2CNT69	BIP2CNT59	BIP2CNT49	BIP2CNT39	BIP2CNT29	BIP2CNT19	BIP2CNT09
D8	11011000	VT10PTR+3	VT10PTR+2	VT10PTR+1	VT10PTR+0	BIP2CNT1110	BIP2CNT1010	BIP2CNT910	BIP2CNT810
D9	11011001	BIP2CNT710	BIP2CNT610	BIP2CNT510	BIP2CNT410	BIP2CNT310	BIP2CNT210	BIP2CNT101	BIP2CNT010
DA	11011010	VT11PTR+3	VT11PTR+2	VT11PTR+1	VT11PTR+0	BIP2CNT1111	BIP2CNT1011	BIP2CNT911	BIP2CNT811
DB	11011011	BIP2CNT711	BIP2CNT611	BIP2CNT511	BIP2CNT411	BIP2CNT311	BIP2CNT211	BIP2CNT111	BIP2CNT011
DC	11011100	VT12PTR+3	VT12PTR+2	VT12PTR+1	VT12PTR+0	BIP2CNT1112	BIP2CNT1012	BIP2CNT912	BIP2CNT812
DD	11011101	BIP2CNT712	BIP2CNT612	BIP2CNT512	BIP2CNT412	BIP2CNT312	BIP2CNT212	BIP2CNT112	BIP2CNT012
DE	11011110	VT13PTR+3	VT13PTR+2	VT13PTR+1	VT13PTR+0	BIP2CNT1113	BIP2CNT1013	BIP2CNT913	BIP2CNT813
DF	11011111	BIP2CNT713	BIP2CNT613	BIP2CNT513	BIP2CNT413	BIP2CNT313	BIP2CNT213	BIP2CNT113	BIP2CNT013
E0	11100000	VT14PTR+3	VT14PTR+2	VT14PTR+1	VT14PTR+0	BIP2CNT1114	BIP2CNT1014	BIP2CNT914	BIP2CNT814
E1	11100001	BIP2CNT714	BIP2CNT614	BIP2CNT514	BIP2CNT414	BIP2CNT314	BIP2CNT214	BIP2CNT114	BIP2CNT014
E2	11100010	VT15PTR+3	VT15PTR+2	VT15PTR+1	VT15PTR+0	BIP2CNT1115	BIP2CNT1015	BIP2CNT915	BIP2CNT815
E3	11100011	BIP2CNT715	BIP2CNT615	BIP2CNT515	BIP2CNT415	BIP2CNT315	BIP2CNT215	BIP2CNT115	BIP2CNT015
E4	11100100	VT16PTR+3	VT16PTR+2	VT16PTR+1	VT16PTR+0	BIP2CNT1116	BIP2CNT1016	BIP2CNT916	BIP2CNT816

Microprocessor Interface DS1 Mode (continued)

Microprocessor Interface Register Architecture (continued)

Table 10. Device-Level Control, Alarm, and Mask Bits Register Set (continued)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
E5	11100101	BIP2CNT716	BIP2CNT616	BIP2CNT516	BIP2CNT416	BIP2CNT316	BIP2CNT216	BIP2CNT116	BIP2CNT016
E6	11100110	VT17PTR+3	VT17PTR+2	VT17PTR+1	VT17PTR+0	BIP2CNT1117	BIP2CNT1017	BIP2CNT917	BIP2CNT817
E7	11100111	BIP2CNT717	BIP2CNT617	BIP2CNT517	BIP2CNT417	BIP2CNT317	BIP2CNT217	BIP2CNT117	BIP2CNT017
E8	11101000	VT18PTR+3	VT18PTR+2	VT18PTR+1	VT188PTR+0	BIP2CNT1118	BIP2CNT1018	BIP2CNT918	BIP2CNT818
E9	11101001	BIP2CNT718	BIP2CNT618	BIP2CNT518	BIP2CNT418	BIP2CNT318	BIP2CNT218	BIP2CNT118	BIP2CNT018
EA	11101010	VT19PTR+3	VT19PTR+2	VT19PTR+1	VT19PTR+0	BIP2CNT1119	BIP2CNT1019	BIP2CNT919	BIP2CNT819
EB	11101011	BIP2CNT719	BIP2CNT619	BIP2CNT519	BIP2CNT419	BIP2CNT319	BIP2CNT219	BIP2CNT119	BIP2CNT019
EC	11101100	VT20PTR+3	VT20PTR+2	VT20PTR+1	VT20PTR+0	BIP2CNT1120	BIP2CNT1020	BIP2CNT920	BIP2CNT820
ED	11101101	BIP2CNT720	BIP2CNT620	BIP2CNT520	BIP2CNT420	BIP2CNT320	BIP2CNT220	BIP2CNT120	BIP2CNT020
EE	11101110	VT21PTR+3	VT21PTR+2	VT21PTR+1	VT21PTR+0	BIP2CNT1121	BIP2CNT1021	BIP2CNT921	BIP2CNT821
EF	11101111	BIP2CNT721	BIP2CNT621	BIP2CNT521	BIP2CNT421	BIP2CNT321	BIP2CNT221	BIP2CNT121	BIP2CNT021
F0	11110000	VT22PTR+3	VT22PTR+2	VT22PTR+1	VT22PTR+0	BIP2CNT1122	BIP2CNT1022	BIP2CNT922	BIP2CNT822
F1	11110001	BIP2CNT722	BIP2CNT622	BIP2CNT522	BIP2CNT422	BIP2CNT322	BIP2CNT222	BIP2CNT122	BIP2CNT022
F2	11110010	VT23PTR+3	VT23PTR+2	VT23PTR+1	VT23PTR+0	BIP2CNT1123	BIP2CNT1023	BIP2CNT923	BIP2CNT823
F3	11110011	BIP2CNT723	BIP2CNT623	BIP2CNT523	BIP2CNT423	BIP2CNT323	BIP2CNT223	BIP2CNT123	BIP2CNT023
F4	11110100	VT24PTR+3	VT24PTR+2	VT24PTR+1	VT24PTR+0	BIP2CNT1124	BIP2CNT1024	BIP2CNT924	BIP2CNT824
F5	11110101	BIP2CNT724	BIP2CNT624	BIP2CNT524	BIP2CNT424	BIP2CNT324	BIP2CNT224	BIP2CNT124	BIP2CNT024
F6	11110110	VT25PTR+3	VT25PTR+2	VT25PTR+1	VT25PTR+0	BIP2CNT1125	BIP2CNT1025	BIP2CNT925	BIP2CNT825
F7	11110111	BIP2CNT725	BIP2CNT625	BIP2CNT525	BIP2CNT425	BIP2CNT325	BIP2CNT225	BIP2CNT125	BIP2CNT025
F8	11111000	VT26PTR+3	VT26PTR+2	VT26PTR+1	VT26PTR+0	BIP2CNT1126	BIP2CNT1026	BIP2CNT926	BIP2CNT826
F9	11111001	BIP2CNT726	BIP2CNT626	BIP2CNT526	BIP2CNT426	BIP2CNT326	BIP2CNT226	BIP2CNT126	BIP2CNT026
FA	11111010	VT27PTR+3	VT27PTR+2	VT27PTR+1	VT27PTR+0	BIP2CNT1127	BIP2CNT1027	BIP2CNT927	BIP2CNT827
FB	11111011	BIP2CNT727	BIP2CNT627	BIP2CNT527	BIP2CNT427	BIP2CNT327	BIP2CNT227	BIP2CNT127	BIP2CNT027
FC	11111100	VT28PTR+3	VT28PTR+2	VT28PTR+1	VT28PTR+0	BIP2CNT1128	BIP2CNT1028	BIP2CNT928	BIP2CNT828
FD	11111101	BIP2CNT728	BIP2CNT628	BIP2CNT528	BIP2CNT428	BIP2CNT328	BIP2CNT228	BIP2CNT128	BIP2CNT028
FE	11111110	SPTR+7	SPTR+6	SPTR+5	SPTR+4	SPTR+3	SPTR+2	SPTR+1	SPTR+0
FF	11111111	SPTR–7	SPTR–6	SPTR–5	SPTR–4	SPTR–3	SPTR–2	SPTR–1	SPTR–0
When FEBE_CNTS = 1									
C0	11000000	0	0	0	0	0	0	0	0
C1	11000001	0	0	0	0	0	0	0	0
C2	11000010	B2FEBE15	B2FEBE14	B2FEBE13	B2FEBE12	B2FEBE11	B2FEBE10	B2FEBE9	B2FEBE8
C3	11000011	B2FEBE7	B2FEBE6	B2FEBE5	B2FEBE4	B2FEBE3	B2FEBE2	B2FEBE1	B2FEBE0
C4	11000100	B3FEBE15	B3FEBE14	B3FEBE13	B3FEBE12	B3FEBE11	B3FEBE10	B3FEBE9	B3FEBE8
C5	11000101	B3FEBE7	B3FEBE6	B3FEBE5	B3FEBE4	B3FEBE3	B3FEBE2	B3FEBE1	B3FEBE0
C6	11000110	VT1PTR-3	VT1PTR-2	VT1PTR-1	VT1PTR-0	0	VTFEBE101	VTFEBE91	VTFEBE81
C7	11000111	VTFEBE71	VTFEBE61	VTFEBE51	VTFEBE41	VTFEBE31	VTFEBE21	VTFEBE11	VTFEBE01
C8	11001000	VT2PTR-3	VT2PTR-2	VT2PTR-1	VT2PTR-0	0	VTFEBE102	VTFEBE92	VTFEBE82
C9	11001001	VTFEBE72	VTFEBE62	VTFEBE52	VTFEBE42	VTFEBE32	VTFEBE22	VTFEBE12	VTFEBE02
CA	11001010	VT3PTR-3	VT3PTR-2	VT3PTR-1	VT3PTR-0	0	VTFEBE103	VTFEBE93	VTFEBE83
CB	11001011	VTFEBE73	VTFEBE63	VTFEBE53	VTFEBE43	VTFEBE33	VTFEBE23	VTFEBE13	VTFEBE03
CC	11001100	VT4PTR-3	VT4PTR-2	VT4PTR-1	VT4PTR-0	0	VTFEBE104	VTFEBE94	VTFEBE84
CD	11001101	VTFEBE74	VTFEBE64	VTFEBE54	VTFEBE44	VTFEBE34	VTFEBE24	VTFEBE14	VTFEBE04
CE	11001110	VT5PTR-3	VT5PTR-2	VT5PTR-1	VT5PTR-0	0	VTFEBE105	VTFEBE95	VTFEBE85
CF	11001111	VTFEBE75	VTFEBE65	VTFEBE55	VTFEBE45	VTFEBE35	VTFEBE25	VTFEBE15	VTFEBE05
D0	11010000	VT6PTR-3	VT6PTR-2	VT6PTR-1	VT6PTR-0	0	VTFEBE106	VTFEBE96	VTFEBE86

Microprocessor Interface DS1 Mode (continued)

Microprocessor Interface Register Architecture (continued)

Table 10. Device-Level Control, Alarm, and Mask Bits Register Set (continued)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D1	11010001	VTFEBE76	VTFEBE66	VTFEBE56	VTFEBE46	VTFEBE36	VTFEBE26	VTFEBE16	VTFEBE06
D2	11010010	VT7PTR-3	VT7PTR-2	VT7PTR-1	VT7PTR-0	0	VTFEBE107	VTFEBE97	VTFEBE87
D3	11010011	VTFEBE77	VTFEBE67	VTFEBE57	VTFEBE47	VTFEBE37	VTFEBE27	VTFEBE17	VTFEBE07
D4	11010100	VT8PTR-3	VT8PTR-2	VT8PTR-1	VT8PTR-0	0	VTFEBE108	VTFEBE98	VTFEBE88
D5	11010101	VTFEBE78	VTFEBE68	VTFEBE58	VTFEBE48	VTFEBE38	VTFEBE28	VTFEBE18	VTFEBE08
D6	11010110	VT9PTR-3	VT9PTR-2	VT9PTR-1	VT9PTR-0	0	VTFEBE109	VTFEBE99	VTFEBE89
D7	11010111	VTFEBE79	VTFEBE69	VTFEBE59	VTFEBE49	VTFEBE39	VTFEBE29	VTFEBE19	VTFEBE09
D8	11011000	VT10PTR-3	VT10PTR-2	VT10PTR-1	VT10PTR-0	0	VTFEBE1010	VTFEBE910	VTFEBE810
D9	11011001	VTFEBE710	VTFEBE610	VTFEBE510	VTFEBE410	VTFEBE310	VTFEBE210	VTFEBE101	VTFEBE010
DA	11011010	VT11PTR-3	VT11PTR-2	VT11PTR-1	VT11PTR-0	0	VTFEBE1011	VTFEBE911	VTFEBE811
DB	11011011	VTFEBE711	VTFEBE611	VTFEBE511	VTFEBE411	VTFEBE311	VTFEBE211	VTFEBE111	VTFEBE011
DC	11011100	VT12PTR-3	VT12PTR-2	VT12PTR-1	VT12PTR-0	0	VTFEBE1012	VTFEBE912	VTFEBE812
DD	11011101	VTFEBE712	VTFEBE612	VTFEBE512	VTFEBE412	VTFEBE312	VTFEBE212	VTFEBE112	VTFEBE012
DE	11011110	VT13PTR-3	VT13PTR-2	VT13PTR-1	VT13PTR-0	0	VTFEBE1013	VTFEBE913	VTFEBE813
DF	11011111	VTFEBE713	VTFEBE613	VTFEBE513	VTFEBE413	VTFEBE313	VTFEBE213	VTFEBE113	VTFEBE013
E0	11100000	VT14PTR-3	VT14PTR-2	VT14PTR-1	VT14PTR-0	0	VTFEBE1014	VTFEBE914	VTFEBE814
E1	11100001	VTFEBE714	VTFEBE614	VTFEBE514	VTFEBE414	VTFEBE314	VTFEBE214	VTFEBE114	VTFEBE014
E2	11100010	VT15PTR-3	VT15PTR-2	VT15PTR-1	VT15PTR-0	0	VTFEBE1015	VTFEBE915	VTFEBE815
E3	11100011	VTFEBE715	VTFEBE615	VTFEBE515	VTFEBE415	VTFEBE315	VTFEBE215	VTFEBE115	VTFEBE015
E4	11100100	VT16PTR-3	VT16PTR-2	VT16PTR-1	VT16PTR-0	0	VTFEBE1016	VTFEBE916	VTFEBE816
E5	11100101	VTFEBE716	VTFEBE616	VTFEBE516	VTFEBE416	VTFEBE316	VTFEBE216	VTFEBE116	VTFEBE016
E6	11100110	VT17PTR-3	VT17PTR-2	VT17PTR-1	VT17PTR-0	0	VTFEBE1017	VTFEBE917	VTFEBE817
E7	11100111	VTFEBE717	VTFEBE617	VTFEBE517	VTFEBE417	VTFEBE317	VTFEBE217	VTFEBE117	VTFEBE017
E8	11101000	VT18PTR-3	VT18PTR-2	VT18PTR-1	VT188PTR-0	0	VTFEBE1018	VTFEBE918	VTFEBE818
E9	11101001	VTFEBE718	VTFEBE618	VTFEBE518	VTFEBE418	VTFEBE318	VTFEBE218	VTFEBE118	VTFEBE018
EA	11101010	VT19PTR-3	VT19PTR-2	VT19PTR-1	VT19PTR-0	0	VTFEBE1019	VTFEBE919	VTFEBE819
EB	11101011	VTFEBE719	VTFEBE619	VTFEBE519	VTFEBE419	VTFEBE319	VTFEBE219	VTFEBE119	VTFEBE019
EC	11101100	VT20PTR-3	VT20PTR-2	VT20PTR-1	VT20PTR-0	0	VTFEBE1020	VTFEBE920	VTFEBE820
ED	11101101	VTFEBE720	VTFEBE620	VTFEBE520	VTFEBE420	VTFEBE320	VTFEBE220	VTFEBE120	VTFEBE020
EE	11101110	VT21PTR-3	VT21PTR-2	VT21PTR-1	VT21PTR-0	0	VTFEBE1021	VTFEBE921	VTFEBE821
EF	11101111	VTFEBE721	VTFEBE621	VTFEBE521	VTFEBE421	VTFEBE321	VTFEBE221	VTFEBE121	VTFEBE021
F0	11110000	VT22PTR-3	VT22PTR-2	VT22PTR-1	VT22PTR-0	0	VTFEBE1022	VTFEBE922	VTFEBE822
F1	11110001	VTFEBE722	VTFEBE622	VTFEBE522	VTFEBE422	VTFEBE322	VTFEBE222	VTFEBE122	VTFEBE022
F2	11110010	VT23PTR-3	VT23PTR-2	VT23PTR-1	VT23PTR-0	0	VTFEBE1023	VTFEBE923	VTFEBE823
F3	11110011	VTFEBE723	VTFEBE623	VTFEBE523	VTFEBE423	VTFEBE323	VTFEBE223	VTFEBE123	VTFEBE023
F4	11110100	VT24PTR-3	VT24PTR-2	VT24PTR-1	VT24PTR-0	0	VTFEBE1024	VTFEBE924	VTFEBE824
F5	11110101	VTFEBE724	VTFEBE624	VTFEBE524	VTFEBE424	VTFEBE324	VTFEBE224	VTFEBE124	VTFEBE024
F6	11110110	VT25PTR-3	VT25PTR-2	VT25PTR-1	VT25PTR-0	0	VTFEBE1025	VTFEBE925	VTFEBE825
F7	11110111	VTFEBE725	VTFEBE625	VTFEBE525	VTFEBE425	VTFEBE325	VTFEBE225	VTFEBE125	VTFEBE025
F8	11111000	VT26PTR-3	VT26PTR-2	VT26PTR-1	VT26PTR-0	0	VTFEBE1026	VTFEBE926	VTFEBE826
F9	11111001	VTFEBE726	VTFEBE626	VTFEBE526	VTFEBE426	VTFEBE326	VTFEBE226	VTFEBE126	VTFEBE026
FA	11111010	VT27PTR-3	VT27PTR-2	VT27PTR-1	VT27PTR-0	0	VTFEBE1027	VTFEBE927	VTFEBE827
FB	11111011	VTFEBE727	VTFEBE627	VTFEBE527	VTFEBE427	VTFEBE327	VTFEBE227	VTFEBE127	VTFEBE027
FC	11111100	VT28PTR-3	VT28PTR-2	VT28PTR-1	VT28PTR-0	0	VTFEBE1028	VTFEBE928	VTFEBE828

Microprocessor Interface DS1 Mode (continued)

Microprocessor Interface Register Architecture (continued)

Table 10. Device-Level Control, Alarm, and Mask Bits Register Set (continued)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FD	11111101	VTFEBE728	VTFEBE628	VTFEBE528	VTFEBE428	VTFEBE328	VTFEBE228	VTFEBE128	VTFEBE028
FE	11111110	0	0	0	0	0	0	0	0
FF	11111111	0	0	0	0	0	0	0	0
					When RJ1BYTE = 1				
C0	11000000	RJ1BYTE647	RJ1BYTE646	RJ1BYTE645	RJ1BYTE644	RJ1BYTE643	RJ1BYTE642	RJ1BYTE641	RJ1BYTE640
C1	11000001	RJ1BYTE637	RJ1BYTE636	RJ1BYTE635	RJ1BYTE634	RJ1BYTE633	RJ1BYTE632	RJ1BYTE631	RJ1BYTE630
C2	11000010	RJ1BYTE627	RJ1BYTE626	RJ1BYTE625	RJ1BYTE624	RJ1BYTE623	RJ1BYTE622	RJ1BYTE621	RJ1BYTE620
C3	11000011	RJ1BYTE617	RJ1BYTE616	RJ1BYTE615	RJ1BYTE614	RJ1BYTE613	RJ1BYTE612	RJ1BYTE611	RJ1BYTE610
C4	11000100	RJ1BYTE607	RJ1BYTE606	RJ1BYTE605	RJ1BYTE604	RJ1BYTE603	RJ1BYTE602	RJ1BYTE601	RJ1BYTE600
C5	11000101	RJ1BYTE597	RJ1BYTE596	RJ1BYTE595	RJ1BYTE594	RJ1BYTE593	RJ1BYTE592	RJ1BYTE591	RJ1BYTE590
C6	11000110	RJ1BYTE587	RJ1BYTE586	RJ1BYTE585	RJ1BYTE584	RJ1BYTE583	RJ1BYTE582	RJ1BYTE581	RJ1BYTE580
C7	11000111	RJ1BYTE577	RJ1BYTE576	RJ1BYTE575	RJ1BYTE574	RJ1BYTE573	RJ1BYTE572	RJ1BYTE571	RJ1BYTE570
C8	11001000	RJ1BYTE567	RJ1BYTE566	RJ1BYTE565	RJ1BYTE564	RJ1BYTE563	RJ1BYTE562	RJ1BYTE561	RJ1BYTE560
C9	11001001	RJ1BYTE557	RJ1BYTE556	RJ1BYTE555	RJ1BYTE554	RJ1BYTE553	RJ1BYTE552	RJ1BYTE551	RJ1BYTE550
CA	11001010	RJ1BYTE547	RJ1BYTE546	RJ1BYTE545	RJ1BYTE544	RJ1BYTE543	RJ1BYTE542	RJ1BYTE541	RJ1BYTE540
CB	11001011	RJ1BYTE537	RJ1BYTE536	RJ1BYTE535	RJ1BYTE534	RJ1BYTE533	RJ1BYTE532	RJ1BYTE531	RJ1BYTE530
CC	11001100	RJ1BYTE527	RJ1BYTE526	RJ1BYTE525	RJ1BYTE524	RJ1BYTE523	RJ1BYTE522	RJ1BYTE521	RJ1BYTE520
CD	11001101	RJ1BYTE517	RJ1BYTE516	RJ1BYTE515	RJ1BYTE514	RJ1BYTE513	RJ1BYTE512	RJ1BYTE511	RJ1BYTE510
CE	11001110	RJ1BYTE507	RJ1BYTE506	RJ1BYTE505	RJ1BYTE504	RJ1BYTE503	RJ1BYTE502	RJ1BYTE501	RJ1BYTE500
CF	11001111	RJ1BYTE497	RJ1BYTE496	RJ1BYTE495	RJ1BYTE494	RJ1BYTE493	RJ1BYTE492	RJ1BYTE491	RJ1BYTE490
D0	11010000	RJ1BYTE487	RJ1BYTE486	RJ1BYTE485	RJ1BYTE484	RJ1BYTE483	RJ1BYTE482	RJ1BYTE481	RJ1BYTE480
D1	11010001	RJ1BYTE477	RJ1BYTE476	RJ1BYTE475	RJ1BYTE474	RJ1BYTE473	RJ1BYTE472	RJ1BYTE471	RJ1BYTE470
D2	11010010	RJ1BYTE467	RJ1BYTE466	RJ1BYTE465	RJ1BYTE464	RJ1BYTE463	RJ1BYTE462	RJ1BYTE461	RJ1BYTE460
D3	11010011	RJ1BYTE457	RJ1BYTE456	RJ1BYTE455	RJ1BYTE454	RJ1BYTE453	RJ1BYTE452	RJ1BYTE451	RJ1BYTE450
D4	11010100	RJ1BYTE447	RJ1BYTE446	RJ1BYTE445	RJ1BYTE444	RJ1BYTE443	RJ1BYTE442	RJ1BYTE441	RJ1BYTE440
D5	11010101	RJ1BYTE437	RJ1BYTE436	RJ1BYTE435	RJ1BYTE434	RJ1BYTE433	RJ1BYTE432	RJ1BYTE431	RJ1BYTE430
D6	11010110	RJ1BYTE427	RJ1BYTE426	RJ1BYTE425	RJ1BYTE424	RJ1BYTE423	RJ1BYTE422	RJ1BYTE421	RJ1BYTE420
D7	11010111	RJ1BYTE417	RJ1BYTE416	RJ1BYTE415	RJ1BYTE414	RJ1BYTE413	RJ1BYTE412	RJ1BYTE411	RJ1BYTE410
D8	11011000	RJ1BYTE407	RJ1BYTE406	RJ1BYTE405	RJ1BYTE404	RJ1BYTE403	RJ1BYTE402	RJ1BYTE401	RJ1BYTE400
D9	11011001	RJ1BYTE397	RJ1BYTE396	RJ1BYTE395	RJ1BYTE394	RJ1BYTE393	RJ1BYTE392	RJ1BYTE391	RJ1BYTE390
DA	11011010	RJ1BYTE387	RJ1BYTE386	RJ1BYTE385	RJ1BYTE384	RJ1BYTE383	RJ1BYTE382	RJ1BYTE381	RJ1BYTE380
DB	11011011	RJ1BYTE377	RJ1BYTE376	RJ1BYTE375	RJ1BYTE374	RJ1BYTE373	RJ1BYTE372	RJ1BYTE371	RJ1BYTE370
DC	11011100	RJ1BYTE367	RJ1BYTE366	RJ1BYTE365	RJ1BYTE364	RJ1BYTE363	RJ1BYTE362	RJ1BYTE361	RJ1BYTE360
DD	11011101	RJ1BYTE357	RJ1BYTE356	RJ1BYTE355	RJ1BYTE354	RJ1BYTE353	RJ1BYTE352	RJ1BYTE351	RJ1BYTE350
DE	11011110	RJ1BYTE347	RJ1BYTE346	RJ1BYTE345	RJ1BYTE344	RJ1BYTE343	RJ1BYTE342	RJ1BYTE341	RJ1BYTE340
DF	11011111	RJ1BYTE337	RJ1BYTE336	RJ1BYTE335	RJ1BYTE334	RJ1BYTE333	RJ1BYTE332	RJ1BYTE331	RJ1BYTE330
E0	11100000	RJ1BYTE327	RJ1BYTE326	RJ1BYTE325	RJ1BYTE324	RJ1BYTE323	RJ1BYTE322	RJ1BYTE321	RJ1BYTE320
E1	11100001	RJ1BYTE317	RJ1BYTE316	RJ1BYTE315	RJ1BYTE314	RJ1BYTE313	RJ1BYTE312	RJ1BYTE311	RJ1BYTE310
E2	11100010	RJ1BYTE307	RJ1BYTE306	RJ1BYTE305	RJ1BYTE304	RJ1BYTE303	RJ1BYTE302	RJ1BYTE301	RJ1BYTE300
E3	11100011	RJ1BYTE297	RJ1BYTE296	RJ1BYTE295	RJ1BYTE294	RJ1BYTE293	RJ1BYTE292	RJ1BYTE291	RJ1BYTE290
E4	11100100	RJ1BYTE287	RJ1BYTE286	RJ1BYTE285	RJ1BYTE284	RJ1BYTE283	RJ1BYTE282	RJ1BYTE281	RJ1BYTE280
E5	11100101	RJ1BYTE277	RJ1BYTE276	RJ1BYTE275	RJ1BYTE274	RJ1BYTE273	RJ1BYTE272	RJ1BYTE271	RJ1BYTE270
E6	11100110	RJ1BYTE267	RJ1BYTE266	RJ1BYTE265	RJ1BYTE264	RJ1BYTE263	RJ1BYTE262	RJ1BYTE261	RJ1BYTE260
E7	11100111	RJ1BYTE257	RJ1BYTE256	RJ1BYTE255	RJ1BYTE254	RJ1BYTE253	RJ1BYTE252	RJ1BYTE251	RJ1BYTE250

Microprocessor Interface DS1 Mode (continued)

Microprocessor Interface Register Architecture (continued)

Table 10. Device-Level Control, Alarm, and Mask Bits Register Set (continued)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
E8	11101000	RJ1BYTE247	RJ1BYTE246	RJ1BYTE245	RJ1BYTE244	RJ1BYTE243	RJ1BYTE242	RJ1BYTE241	RJ1BYTE240
E9	11101001	RJ1BYTE237	RJ1BYTE236	RJ1BYTE235	RJ1BYTE234	RJ1BYTE233	RJ1BYTE232	RJ1BYTE231	RJ1BYTE230
EA	11101010	RJ1BYTE227	RJ1BYTE226	RJ1BYTE225	RJ1BYTE224	RJ1BYTE223	RJ1BYTE222	RJ1BYTE221	RJ1BYTE220
EB	11101011	RJ1BYTE217	RJ1BYTE216	RJ1BYTE215	RJ1BYTE214	RJ1BYTE213	RJ1BYTE212	RJ1BYTE211	RJ1BYTE210
EC	11101100	RJ1BYTE207	RJ1BYTE206	RJ1BYTE205	RJ1BYTE204	RJ1BYTE203	RJ1BYTE202	RJ1BYTE201	RJ1BYTE200
ED	11101101	RJ1BYTE197	RJ1BYTE196	RJ1BYTE195	RJ1BYTE194	RJ1BYTE193	RJ1BYTE192	RJ1BYTE191	RJ1BYTE190
EE	11101110	RJ1BYTE187	RJ1BYTE186	RJ1BYTE185	RJ1BYTE184	RJ1BYTE183	RJ1BYTE182	RJ1BYTE181	RJ1BYTE180
EF	11101111	RJ1BYTE177	RJ1BYTE176	RJ1BYTE175	RJ1BYTE174	RJ1BYTE173	RJ1BYTE172	RJ1BYTE171	RJ1BYTE170
F0	11110000	RJ1BYTE167	RJ1BYTE166	RJ1BYTE165	RJ1BYTE164	RJ1BYTE163	RJ1BYTE162	RJ1BYTE161	RJ1BYTE160
F1	11110001	RJ1BYTE157	RJ1BYTE156	RJ1BYTE155	RJ1BYTE154	RJ1BYTE153	RJ1BYTE152	RJ1BYTE151	RJ1BYTE150
F2	11110010	RJ1BYTE147	RJ1BYTE146	RJ1BYTE145	RJ1BYTE144	RJ1BYTE143	RJ1BYTE142	RJ1BYTE141	RJ1BYTE140
F3	11110011	RJ1BYTE137	RJ1BYTE136	RJ1BYTE135	RJ1BYTE134	RJ1BYTE133	RJ1BYTE132	RJ1BYTE131	RJ1BYTE130
F4	11110100	RJ1BYTE127	RJ1BYTE126	RJ1BYTE125	RJ1BYTE124	RJ1BYTE123	RJ1BYTE122	RJ1BYTE121	RJ1BYTE120
F5	11110101	RJ1BYTE117	RJ1BYTE116	RJ1BYTE115	RJ1BYTE114	RJ1BYTE113	RJ1BYTE112	RJ1BYTE111	RJ1BYTE110
F6	11110110	RJ1BYTE107	RJ1BYTE106	RJ1BYTE105	RJ1BYTE104	RJ1BYTE103	RJ1BYTE102	RJ1BYTE101	RJ1BYTE100
F7	11110111	RJ1BYTE97	RJ1BYTE96	RJ1BYTE95	RJ1BYTE94	RJ1BYTE93	RJ1BYTE92	RJ1BYTE91	RJ1BYTE90
F8	11111000	RJ1BYTE87	RJ1BYTE86	RJ1BYTE85	RJ1BYTE84	RJ1BYTE83	RJ1BYTE82	RJ1BYTE81	RJ1BYTE80
F9	11111001	RJ1BYTE77	RJ1BYTE76	RJ1BYTE75	RJ1BYTE74	RJ1BYTE73	RJ1BYTE72	RJ1BYTE71	RJ1BYTE70
FA	11111010	RJ1BYTE67	RJ1BYTE66	RJ1BYTE65	RJ1BYTE64	RJ1BYTE63	RJ1BYTE62	RJ1BYTE61	RJ1BYTE60
FB	11111011	RJ1BYTE57	RJ1BYTE56	RJ1BYTE55	RJ1BYTE54	RJ1BYTE53	RJ1BYTE52	RJ1BYTE51	RJ1BYTE50
FC	11111100	RJ1BYTE47	RJ1BYTE46	RJ1BYTE45	RJ1BYTE44	RJ1BYTE43	RJ1BYTE42	RJ1BYTE41	RJ1BYTE40
FD	11111101	RJ1BYTE37	RJ1BYTE36	RJ1BYTE35	RJ1BYTE34	RJ1BYTE33	RJ1BYTE32	RJ1BYTE31	RJ1BYTE30
FE	11111110	RJ1BYTE27	RJ1BYTE26	RJ1BYTE25	RJ1BYTE24	RJ1BYTE23	RJ1BYTE22	RJ1BYTE21	RJ1BYTE20
FF	11111111	RJ1BYTE17	RJ1BYTE16	RJ1BYTE15	RJ1BYTE14	RJ1BYTE13	RJ1BYTE12	RJ1BYTE11	RJ1BYTE10
When TJ1BYTE_RD = 1									
C0	11000000	TJ1BYTE647	TJ1BYTE646	TJ1BYTE645	TJ1BYTE644	TJ1BYTE643	TJ1BYTE642	TJ1BYTE641	TJ1BYTE640
C1	11000001	TJ1BYTE637	TJ1BYTE636	TJ1BYTE635	TJ1BYTE634	TJ1BYTE633	TJ1BYTE632	TJ1BYTE631	TJ1BYTE630
C2	11000010	TJ1BYTE627	TJ1BYTE626	TJ1BYTE625	TJ1BYTE624	TJ1BYTE623	TJ1BYTE622	TJ1BYTE621	TJ1BYTE620
C3	11000011	TJ1BYTE617	TJ1BYTE616	TJ1BYTE615	TJ1BYTE614	TJ1BYTE613	TJ1BYTE612	TJ1BYTE611	TJ1BYTE610
C4	11000100	TJ1BYTE607	TJ1BYTE606	TJ1BYTE605	TJ1BYTE604	TJ1BYTE603	TJ1BYTE602	TJ1BYTE601	TJ1BYTE600
C5	11000101	TJ1BYTE597	TJ1BYTE596	TJ1BYTE595	TJ1BYTE594	TJ1BYTE593	TJ1BYTE592	TJ1BYTE591	TJ1BYTE590
C6	11000110	TJ1BYTE587	TJ1BYTE586	TJ1BYTE585	TJ1BYTE584	TJ1BYTE583	TJ1BYTE582	TJ1BYTE581	TJ1BYTE580
C7	11000111	TJ1BYTE577	TJ1BYTE576	TJ1BYTE575	TJ1BYTE574	TJ1BYTE573	TJ1BYTE572	TJ1BYTE571	TJ1BYTE570
C8	11001000	TJ1BYTE567	TJ1BYTE566	TJ1BYTE565	TJ1BYTE564	TJ1BYTE563	TJ1BYTE562	TJ1BYTE561	TJ1BYTE560
C9	11001001	TJ1BYTE557	TJ1BYTE556	TJ1BYTE555	TJ1BYTE554	TJ1BYTE553	TJ1BYTE552	TJ1BYTE551	TJ1BYTE550
CA	11001010	TJ1BYTE547	TJ1BYTE546	TJ1BYTE545	TJ1BYTE544	TJ1BYTE543	TJ1BYTE542	TJ1BYTE541	TJ1BYTE540
CB	11001011	TJ1BYTE537	TJ1BYTE536	TJ1BYTE535	TJ1BYTE534	TJ1BYTE533	TJ1BYTE532	TJ1BYTE531	TJ1BYTE530
CC	11001100	TJ1BYTE527	TJ1BYTE526	TJ1BYTE525	TJ1BYTE524	TJ1BYTE523	TJ1BYTE522	TJ1BYTE521	TJ1BYTE520
CD	11001101	TJ1BYTE517	TJ1BYTE516	TJ1BYTE515	TJ1BYTE514	TJ1BYTE513	TJ1BYTE512	TJ1BYTE511	TJ1BYTE510
CE	11001110	TJ1BYTE507	TJ1BYTE506	TJ1BYTE505	TJ1BYTE504	TJ1BYTE503	TJ1BYTE502	TJ1BYTE501	TJ1BYTE500
CF	11001111	TJ1BYTE497	TJ1BYTE496	TJ1BYTE495	TJ1BYTE494	TJ1BYTE493	TJ1BYTE492	TJ1BYTE491	TJ1BYTE490
D0	11010000	TJ1BYTE487	TJ1BYTE486	TJ1BYTE485	TJ1BYTE484	TJ1BYTE483	TJ1BYTE482	TJ1BYTE481	TJ1BYTE480
D1	11010001	TJ1BYTE477	TJ1BYTE476	TJ1BYTE475	TJ1BYTE474	TJ1BYTE473	TJ1BYTE472	TJ1BYTE471	TJ1BYTE470
D2	11010010	TJ1BYTE467	TJ1BYTE466	TJ1BYTE465	TJ1BYTE464	TJ1BYTE463	TJ1BYTE462	TJ1BYTE461	TJ1BYTE460

Microprocessor Interface DS1 Mode (continued)

Microprocessor Interface Register Architecture (continued)

Table 10. Device-Level Control, Alarm, and Mask Bits Register Set (continued)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D3	11010011	TJ1BYTE457	TJ1BYTE456	TJ1BYTE455	TJ1BYTE454	TJ1BYTE453	TJ1BYTE452	TJ1BYTE451	TJ1BYTE450
D4	11010100	TJ1BYTE447	TJ1BYTE446	TJ1BYTE445	TJ1BYTE444	TJ1BYTE443	TJ1BYTE442	TJ1BYTE441	TJ1BYTE440
D5	11010101	TJ1BYTE437	TJ1BYTE436	TJ1BYTE435	TJ1BYTE434	TJ1BYTE433	TJ1BYTE432	TJ1BYTE431	TJ1BYTE430
D6	11010110	TJ1BYTE427	TJ1BYTE426	TJ1BYTE425	TJ1BYTE424	TJ1BYTE423	TJ1BYTE422	TJ1BYTE421	TJ1BYTE420
D7	11010111	TJ1BYTE417	TJ1BYTE416	TJ1BYTE415	TJ1BYTE414	TJ1BYTE413	TJ1BYTE412	TJ1BYTE411	TJ1BYTE410
D8	11011000	TJ1BYTE407	TJ1BYTE406	TJ1BYTE405	TJ1BYTE404	TJ1BYTE403	TJ1BYTE402	TJ1BYTE401	TJ1BYTE400
D9	11011001	TJ1BYTE397	TJ1BYTE396	TJ1BYTE395	TJ1BYTE394	TJ1BYTE393	TJ1BYTE392	TJ1BYTE391	TJ1BYTE390
DA	11011010	TJ1BYTE387	TJ1BYTE386	TJ1BYTE385	TJ1BYTE384	TJ1BYTE383	TJ1BYTE382	TJ1BYTE381	TJ1BYTE380
DB	11011011	TJ1BYTE377	TJ1BYTE376	TJ1BYTE375	TJ1BYTE374	TJ1BYTE373	TJ1BYTE372	TJ1BYTE371	TJ1BYTE370
DC	11011100	TJ1BYTE367	TJ1BYTE366	TJ1BYTE365	TJ1BYTE364	TJ1BYTE363	TJ1BYTE362	TJ1BYTE361	TJ1BYTE360
DD	11011101	TJ1BYTE357	TJ1BYTE356	TJ1BYTE355	TJ1BYTE354	TJ1BYTE353	TJ1BYTE352	TJ1BYTE351	TJ1BYTE350
DE	11011110	TJ1BYTE347	TJ1BYTE346	TJ1BYTE345	TJ1BYTE344	TJ1BYTE343	TJ1BYTE342	TJ1BYTE341	TJ1BYTE340
DF	11011111	TJ1BYTE337	TJ1BYTE336	TJ1BYTE335	TJ1BYTE334	TJ1BYTE333	TJ1BYTE332	TJ1BYTE331	TJ1BYTE330
E0	11100000	TJ1BYTE327	TJ1BYTE326	TJ1BYTE325	TJ1BYTE324	TJ1BYTE323	TJ1BYTE322	TJ1BYTE321	TJ1BYTE320
E1	11100001	TJ1BYTE317	TJ1BYTE316	TJ1BYTE315	TJ1BYTE314	TJ1BYTE313	TJ1BYTE312	TJ1BYTE311	TJ1BYTE310
E2	11100010	TJ1BYTE307	TJ1BYTE306	TJ1BYTE305	TJ1BYTE304	TJ1BYTE303	TJ1BYTE302	TJ1BYTE301	TJ1BYTE300
E3	11100011	TJ1BYTE297	TJ1BYTE296	TJ1BYTE295	TJ1BYTE294	TJ1BYTE293	TJ1BYTE292	TJ1BYTE291	TJ1BYTE290
E4	11100100	TJ1BYTE287	TJ1BYTE286	TJ1BYTE285	TJ1BYTE284	TJ1BYTE283	TJ1BYTE282	TJ1BYTE281	TJ1BYTE280
E5	11100101	TJ1BYTE277	TJ1BYTE276	TJ1BYTE275	TJ1BYTE274	TJ1BYTE273	TJ1BYTE272	TJ1BYTE271	TJ1BYTE270
E6	11100110	TJ1BYTE267	TJ1BYTE266	TJ1BYTE265	TJ1BYTE264	TJ1BYTE263	TJ1BYTE262	TJ1BYTE261	TJ1BYTE260
E7	11100111	TJ1BYTE257	TJ1BYTE256	TJ1BYTE255	TJ1BYTE254	TJ1BYTE253	TJ1BYTE252	TJ1BYTE251	TJ1BYTE250
E8	11101000	TJ1BYTE247	TJ1BYTE246	TJ1BYTE245	TJ1BYTE244	TJ1BYTE243	TJ1BYTE242	TJ1BYTE241	TJ1BYTE240
E9	11101001	TJ1BYTE237	TJ1BYTE236	TJ1BYTE235	TJ1BYTE234	TJ1BYTE233	TJ1BYTE232	TJ1BYTE231	TJ1BYTE230
EA	11101010	TJ1BYTE227	TJ1BYTE226	TJ1BYTE225	TJ1BYTE224	TJ1BYTE223	TJ1BYTE222	TJ1BYTE221	TJ1BYTE220
EB	11101011	TJ1BYTE217	TJ1BYTE216	TJ1BYTE215	TJ1BYTE214	TJ1BYTE213	TJ1BYTE212	TJ1BYTE211	TJ1BYTE210
EC	11101100	TJ1BYTE207	TJ1BYTE206	TJ1BYTE205	TJ1BYTE204	TJ1BYTE203	TJ1BYTE202	TJ1BYTE201	TJ1BYTE200
ED	11101101	TJ1BYTE197	TJ1BYTE196	TJ1BYTE195	TJ1BYTE194	TJ1BYTE193	TJ1BYTE192	TJ1BYTE191	TJ1BYTE190
EE	11101110	TJ1BYTE187	TJ1BYTE186	TJ1BYTE185	TJ1BYTE184	TJ1BYTE183	TJ1BYTE182	TJ1BYTE181	TJ1BYTE180
EF	11101111	TJ1BYTE177	TJ1BYTE176	TJ1BYTE175	TJ1BYTE174	TJ1BYTE173	TJ1BYTE172	TJ1BYTE171	TJ1BYTE170
F0	11110000	TJ1BYTE167	TJ1BYTE166	TJ1BYTE165	TJ1BYTE164	TJ1BYTE163	TJ1BYTE162	TJ1BYTE161	TJ1BYTE160
F1	11110001	TJ1BYTE157	TJ1BYTE156	TJ1BYTE155	TJ1BYTE154	TJ1BYTE153	TJ1BYTE152	TJ1BYTE151	TJ1BYTE150
F2	11110010	TJ1BYTE147	TJ1BYTE146	TJ1BYTE145	TJ1BYTE144	TJ1BYTE143	TJ1BYTE142	TJ1BYTE141	TJ1BYTE140
F3	11110011	TJ1BYTE137	TJ1BYTE136	TJ1BYTE135	TJ1BYTE134	TJ1BYTE133	TJ1BYTE132	TJ1BYTE131	TJ1BYTE130
F4	11110100	TJ1BYTE127	TJ1BYTE126	TJ1BYTE125	TJ1BYTE124	TJ1BYTE123	TJ1BYTE122	TJ1BYTE121	TJ1BYTE120
F5	11110101	TJ1BYTE117	TJ1BYTE116	TJ1BYTE115	TJ1BYTE114	TJ1BYTE113	TJ1BYTE112	TJ1BYTE111	TJ1BYTE110
F6	11110110	TJ1BYTE107	TJ1BYTE106	TJ1BYTE105	TJ1BYTE104	TJ1BYTE103	TJ1BYTE102	TJ1BYTE101	TJ1BYTE100
F7	11110111	TJ1BYTE97	TJ1BYTE96	TJ1BYTE95	TJ1BYTE94	TJ1BYTE93	TJ1BYTE92	TJ1BYTE91	TJ1BYTE90
F8	11111000	TJ1BYTE87	TJ1BYTE86	TJ1BYTE85	TJ1BYTE84	TJ1BYTE83	TJ1BYTE82	TJ1BYTE81	TJ1BYTE80
F9	11111001	TJ1BYTE77	TJ1BYTE76	TJ1BYTE75	TJ1BYTE74	TJ1BYTE73	TJ1BYTE72	TJ1BYTE71	TJ1BYTE70
FA	11111010	TJ1BYTE67	TJ1BYTE66	TJ1BYTE65	TJ1BYTE64	TJ1BYTE63	TJ1BYTE62	TJ1BYTE61	TJ1BYTE60
FB	11111011	TJ1BYTE57	TJ1BYTE56	TJ1BYTE55	TJ1BYTE54	TJ1BYTE53	TJ1BYTE52	TJ1BYTE51	TJ1BYTE50
FC	11111100	TJ1BYTE47	TJ1BYTE46	TJ1BYTE45	TJ1BYTE44	TJ1BYTE43	TJ1BYTE42	TJ1BYTE41	TJ1BYTE40
FD	11111101	TJ1BYTE37	TJ1BYTE36	TJ1BYTE35	TJ1BYTE34	TJ1BYTE33	TJ1BYTE32	TJ1BYTE31	TJ1BYTE30
FE	11111110	TJ1BYTE27	TJ1BYTE26	TJ1BYTE25	TJ1BYTE24	TJ1BYTE23	TJ1BYTE22	TJ1BYTE21	TJ1BYTE20
FF	11111111	TJ1BYTE17	TJ1BYTE16	TJ1BYTE15	TJ1BYTE14	TJ1BYTE13	TJ1BYTE12	TJ1BYTE11	TJ1BYTE10

Microprocessor Interface DS1 Mode (continued)

Microprocessor Interface Register Architecture (continued)

Device-Level Control, Alarm, and Mask Bits (0x00—0x16)

Register 0x00. The reset bit in register 0x00 is used to reset all registers in the microprocessor interface as well as all of the state machines within the device. Activating this bit has the same effect as applying a logic 0 to the device input pin $\overline{\text{RESET}}$. Activating this bit **will** interrupt service. This bit must be written to a logic 1 to activate.

- The BIP2BLKCNT bit is used to determine whether the BIP2CNT counters count the number of BIP-2 errors (BIP2BLKCNT = 0) or the number of BIP-2 blocks that contain errors (BIP2BLKCNT = 1).
- The device can accept a blue signal clock at either the exact DS1 rate (BLUECLKSEL = 0), or at 16 times the DS1 rate (BLUECLKSEL = 1).
- The device has a number of BIP, FEBE, and pointer adjustment counters that are all updated when the LATCH_CNT bit is written from a 0 to a 1. Nothing happens when the bit is written from a 1 to a 0. The only internal counter that is not updated by this bit is the test pattern counter.
- B1ERRINS, B2ERRINS, and B3ERRINS all cause continuous BIP-8 errors to be transmitted in their respective BIP-8 values.
- TEST_CNT forces all internal counters to test mode.

The reset default value for this register is 00000000.

Register 0x01. The bits in register 0x01 are used to provision device-level control bits. The reset default for this register is 00000000. The functions of these bits are described below:

- When FEBE_EN = 1, the device will automatically insert the appropriate FEBE into the transmitted Z2, G1, V5 overhead bytes whenever it receives BIP errors. If FEBE_EN = 0, then the automatic insertion of FEBE is disabled.
- When TXPAISINS = 1, the device will write all ones into the pointer bytes (H1—H3) and all of the synchronous payload envelope (SPE).
- The TXFSYNC is used to identify where the frame sync pulse is active. When TXFSYNC = 0, the device places the output frame sync on the first clock of the frame; otherwise, the frame sync pulse is active on the last clock of the frame.
- When STS1SCR = 1, the device scrambles the outgoing STS-1 frame according to the SONET frame synchronous scrambling sequence $x^7 + x^6 + 1$. The sequence is reset to 1111111 at the beginning of the byte following the C1 byte and scrambles all of the STS-1 data except the A1, A2, and C1 bytes. When this bit is 0, then the transmit data is not scrambled by the device.
- When STS1DSCR = 1, the device scrambles the incoming STS-1 frame according to the SONET frame synchronous descrambling sequence $x^7 + x^6 + 1$. The sequence is reset to 1111111 at the beginning of the byte following the C1 byte and descrambles all of the STS-1 data except the A1, A2, and C1 bytes. When this bit is 0, then the receive data is not descrambled by the device.
- When STS1LB = 1, the transmitted data is looped back to the receive side. When this bit is 0, the device uses the received data.

Register 0x02. The bits in register 0x02 are used to set the edges that retime data into and out of the device. The reset default for this register is 00000000.

- All of the edge registers act such that a logic 1 means that the data is retimed (either in or out) by the rising clock edge; a logic 0 means that the data is retimed by the falling edge.
- Both the TXPARITY and RXPARITY bits determine the type of parity for data buses. When these bits are written with a logic 1, then odd parity is used; even parity otherwise.
- Both the TXSERIAL and RXSERIAL bits are used to set the type of STS-1 data. When either serial bit is written to a logic 1, then the STS-1 rail is run serially; parallel mode is used otherwise.

Register 0x03. The bits in register 0x03 are used to report problems at the receive STS-1 level. The reset default for this register is 00000000.

- STS1OOF = 1 reports an out of frame condition on the receive STS-1 signal.
- STS1LOF = 1 reports an out of frame condition that persists for more than 3 ms.
- STS1LOP = 1 reports a loss of STS-1 pointer.
- STS1PAIS = 1 reports path AIS as detected by the receive pointer interpreter.
- RXPARER = 1 reports a parity violation on the receive STS-1 data bus when in parallel mode.

Microprocessor Interface DS1 Mode
(continued)

Microprocessor Interface Register Architecture (continued)

- The device monitors the incoming H4 byte for loss of multiframe indication (H4LOMF = 1).
- The device monitors the received J1 byte for path trace mismatches. When the received J1 byte pattern doesn't match the previously received pattern, then TRACEER = 1.
- The device monitors the received G1 byte for path RDI. The PATHRDI bit reflects the current state of this bit.

Register 0x04. The bits in register 0x04 are used to mask the contributions of the bits in register 0x03 to the microprocessor interrupt output, INT. The reset default for this register is 11111111. When any of these bits are at a logic 1 level, the corresponding bit in register 0x03 is masked from contributing to the output interrupt. The reset default for this register masks all of the bits in register 0x03.

Register 0x05. The bits in register 0x05 are used to report problems at the receive VT1.5 level. The bits in this register are actually composite bits. The bits that report the problems at the VT1.5 level are actually located in 28 separate registers (one for each VT1.5) as described below. These composite bits are placed in the register map as a convenience to determine which type of error was detected. Any time any of the 28 VT1.5 bits reports an error, the corresponding composite bit will report an error. The reset default for this register is 00000000.

- DS1AISCOM = 1 reports an AIS condition on DS1.
- DS1LOCCOM = 1 reports a loss of input DS1 clock.
- VTLABCOM = 1 reports change of state of the VT1.5 label. In order for this bit to be set, the device must detect three consecutive consistent new values for the VT1.5 label.
- VTAISCOM = 1 reports the fact that the V1 and V2 pointer bytes are all ones for three consecutive superframes.
- VTRDICOM = 1 reports the fact that the VT RDI bits have been received as a new consistent value for three consecutive superframes.
- VTLOPCOM = 1 reports LOP-V.
- VTSIZECOM = 1 reports incorrect VT1.5 size bits. The valid VT size bits for VT1.5 are 11.
- ESOFCOM = 1 reports that the device has experienced either a receive or a transmit elastic store overflow.

Register 0x06. The bits in register 0x06 are used to mask the contributions of the bits in register 0x05 to the microprocessor interrupt output, INT. The reset default for this register is 11111111. When any of these bits are at a logic 1 level, the corresponding bit in register 0x05 is masked from contributing to the output interrupt. The reset default for this register masks all of the bits in register 0x05.

Register 0x07. Bit 0 of register 7 reports the DS1_E1N value from the device input pin.

Register 0x08. The bits in register 0x08 are not currently used.

Register 0x09. The bits in register 0x09 are used to determine which DS1 is selected to drop the test pattern. When TPDROPSIDE = 1, the test pattern is dropped from the SPE drop logic, and the DS1 output that is dropped is the same as described in VT Drop Selection (0x33—0x4E) section on page 36. When TPDROPSIDE = 0, the DS1 that is dropped is the same as described in DS1 Insertion Selection (0x17—0x32) section on page 36.

Register 0x0A. The bits in register 0x0A indicate the condition of the test pattern detector. If the test pattern detector has been able to sync on the dropped signal, then TPOOS = 0. When TPOOS = 0, then the TPERR bits are used to keep a count of the number of bit errors that the test pattern detector has seen. This error count is cleared when the register is read by the microprocessor. This byte defaults to 10000000.

Register 0x0B. The bits in register 0x0B are used to report the F2 receive byte in the path overhead. The default value for this register is 00000000.

Register 0x0C. The bits in register 0x0C are used to report the received C2 label byte in the path overhead. The default value for this register is 00000000 which indicates path unequipped.

Register 0x0D. The bits in register 0x0D are used to report the four least significant bits of the G1 path overhead byte and the three least significant bits of the K2 section overhead bye. The default value for this register is 00000000.

Register 0x0E—0x0F. The bits in register 0x0E—0x0F are used to set the number of consecutive, consistent values required by the previous three registers before updating their values. Valid values for these registers range from 3 to 15. Any value less than 3 defaults to 3 inside the device. These two registers default to 00110011.

Microprocessor Interface DS1 Mode (continued)

Microprocessor Interface Register Architecture (continued)

Register 0x10—0x11. The bits in registers 0x10—0x11 are used to set the transmitted values in the F2 byte, the three least significant bits of the K2 byte, and the four least significant bits of the G1 byte. The G1 byte is written by the microprocessor when G1INS_EN = 1; otherwise, the automatic values described in the STS-1 Generate section on page 12 are inserted.

Register 0x12—0x16. The bits in registers 0x12—0x16 are not currently used.

DS1 Insertion Selection (0x17—0x32)

The DS1AISx bits in bit 7 report the received DS1 AIS condition. When any of these bits are 1, then the corresponding DS1 input has an AIS condition. This value represents the current received state, and the AIS condition is not latched by these bits.

The DS1LOCx bits in bit 6 report the received DS1 loss of clock condition. When any of these bits are 1, then the corresponding DS1 input has a received loss of clock condition. This value represents the current received state, and the loss of clock condition is not latched by these bits.

The DS1xLB bits in bit 5 are used to force DS1 loopback from output to input. When any of these bits are 1, then the corresponding DS1 input is overwritten by the outgoing DS1 signal for that location.

The DS1 selected corresponds to the decimal value of the programmed 5 bits. If these bits contain 00000, then the device will insert unequipped into the corresponding VT1.5 slot. If these bits contain 11101—11110, then the device will insert AIS-V into the corresponding VT1.5 slot. Since the device defaults all 28 of these registers to the value 00000, then all of the 28 VT1.5 slots start off transmitting unequipped following reset. The value 11111 inserts the test pattern.

The DS1_xINS[4:0] bits in registers 0x17—0x32 are used to select the DS1 input for the transmit VT1.5 slots. The reset default for these registers is 00000000. Addresses 0x17—0x32 correspond to VT1.5s as shown in Table 11.

Table 11. DS1 Insertion Selection Format

				5 Programmed Data Bits				
VT1.5 #	VT Group #	VT #	Address	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	1	1	17	0	0	0	0	1
2	2	1	18	0	0	0	1	0
3	3	1	19	0	0	0	1	1
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
26	5	4	30	1	1	0	1	0
27	6	4	31	1	1	0	1	1
28	7	4	32	1	1	1	0	0

VT Drop Selection (0x33—0x4E)

The RXESOFx bits in bit 6 report the receive elastic store overflow condition. When any of these bits are 1, then the corresponding DS1 output has experienced an elastic store overflow. This value is latched by these bits until read by the microprocessor.

The TXESOFx bits in bit 5 report the transmit elastic store overflow condition. When any of these bits are 1, then the corresponding DS1 input has experienced an elastic store overflow. This value is latched by these bits until read by the microprocessor.

The VT1.5 selected corresponds to the decimal value of the programmed 5 bits. If these bits contain 00000 or 11101—11110, then the device will insert AIS into the corresponding DS1 slot. Since the device defaults all 28 of

Microprocessor Interface DS1 Mode (continued)

Microprocessor Interface Register Architecture (continued)

these registers to the value 00000, then all of the 28 DS1 slots start off transmitting AIS following reset. The value 11111 inserts the test pattern.

The bits in registers 0x33—0x4E are used to select the VT1.5 slot for the DS1 outputs. The reset default for these registers is 00000000. VTxDROP 00001—11100 correspond to VT1.5 #'s as shown in Table 12.

Table 12. MVT Drop Selection Format

			5 Programmed Data Bits				
VT1.5 #	VT Group #	VT #	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	1	1	0	0	0	0	1
2	2	1	0	0	0	1	0
3	3	1	0	0	0	1	1
• •	• •	• •	• •	• •	• •	• •	• •
26	5	4	1	1	0	1	0
27	6	4	1	1	0	1	1
28	7	4	1	1	1	0	0

Address 0x33—0x4E correspond to DS1s as shown in Table 13.

Table 13. VT to DS1 Mapping

DS1 #	Address
1	33
2	34
3	35
• •	• •
26	4C
27	4D
28	4E

TX VT Overhead Insertion Control (0x4F—0x6A)

The bits in registers 0x4F—0x6A are used to select the VT1.5 slot for the insertion control bits in the same way as described in DS1 Insertion Selection (0x17—0x32) section on page 36. The reset default for these registers is 00000000.

The bits in these registers provision the transmitted VT1.5 overhead byte, V5. The reset default for this register is 00000000.

- BIP2ERINSx = 1 forces the selected VT1.5 to transmit inverted BIP-2 bits which causes the downstream receiver to declare continuous BIP-2 errors.
- VTRDIx_EN controls whether the RDI-V bits are inserted automatically by the device (VTRDIx_EN = 0) or manually by the microprocessor (VTRDIx_EN = 1).
- VTRDIx_INS[1:0] directly program the transmitted RDI-V bits (i.e., a logic 10 in this position causes a logic 1 to be inserted in bit 4 and a 0 to be inserted in bit 8) when VTRDIx_EN = 1.

Microprocessor Interface DS1 Mode (continued)

Microprocessor Interface Register Architecture (continued)

- VTAISINSx = 1 forces AIS-V to be written into the corresponding VT1.5 slot. This consists of writing all ones into the selected VT1.5 slot.
- VTLAB[2:0]INSx directly program the transmitted VT label bits. These bits are used to carry unequipped information (VTLAB[2:0] = 000) as well as specific payload mappings and AIS-V.

RX VT Drop Monitoring (0x6B—0x86)

The bits in register 0x6B—0x86 are used to report the VT1.5 slot status. The reset default for these registers is 00000000.

The bits in these registers correspond to the received VT1.5 slot in the same way as described in DS1 Insertion Selection (0x17—0x32) section on page 36. The conditions that these bits report are described in Device-Level Control, Alarm, and Mask Bits (0x00—0x16) section on page 34 for the composite bits.

Block Control Register (0xBF)

The bits in register 0xBF control the information presented to the microprocessor from the registers 0xC0—0xFF. These last 64 bytes will display different results depending on the value programmed into this byte. There is a hierarchy of evaluation of these bytes; if BIP_CNTS = 1, then the data in these registers is BIP error information regardless of the values of the other bits in this register. Otherwise, if FEBE_CNTS = 1 the information displayed is the FEBE error information. Otherwise, if RJ1BYTE = 1 then the received J1 bytes are presented. All three of these previous sets of values are read only. The last setting, TJ1BYTE = 1, presents the transmit J1 byte values. These registers are read/write. Any values written into these registers will change the J1 byte values that are transmitted.

BIP_Cnts (0xC0—0xFF)

The bytes in registers 0xC0—0xFF are used to count the number of BIP errors detected by the device when BIP_CNTS = 1. The first six registers, 0xC0—0xC5, are the BIP errors detected by B1, B2, and B3. The remaining registers in the block are the errors seen by the BIP-2 error detectors in the individual VT1.5 slots. In addition, since the BIP-2 errors only require 12 bits, the VT pointer increment counts are presented here. The values in all of these counters is latched by the LATCH_CNTS bit in register 0x00.

FEBE_Cnts (0xC0—0xFF)

The bytes in registers 0xC0—0xFF are used to count the number of FEBE errors detected by the device when FEBE_CNTS = 1 **and** BIP_CNTS = 0. The registers, 0xC2—0xC5, are the FEBE errors detected by B2, and B3. The remaining registers in the block are the errors seen by the FEBE error detectors in the individual VT1.5 slots. In addition, since the VT FEBE errors only require 11 bits, the VT pointer decrement counts are presented here. The values in all of these counters is latched by the LATCH_CNTS bit in register 0x00.

Receive J1 Path Trace Bytes (0xC0—0xFF)

The bits in registers 0xC0—0xFE are used to read the received 64 path trace bytes when RJ1BYTE = 1 **and** BIP_CNTS = 0 **and** FEBE_CNTS = 0. The receive J1 path trace byte RJ1BYTE63[7:0] corresponds to the first byte in the 64-byte sequence, while the J1 path trace byte RJ1BYTE0[7:0] corresponds to the last byte in the 64-byte sequence. The default value for the 64-byte sequence is all zeros. These receive J1 byte values are continuously written into these registers modulo 64. If any received byte doesn't match the previously received byte for its location, TRACEER is set to 1.

Transmit J1 Path Trace Bytes (0xC0—0xFF)

The bits in registers 0xC0—0xFE are used to provision the transmit 64 path trace bytes when TJ1BYTE = 1 **and** RJ1BYTE = 0 **and** BIP_CNTS = 0 **and** FEBE_CNTS = 0. The transmit J1 path trace byte TJ1BYTE63[7:0] corresponds to the first byte in the 64-byte sequence, while the J1 path trace byte TJ1BYTE0[7:0] corresponds to the last byte in the 64-byte sequence. The default value for the 64-byte sequence is all zeros. These registers can be written by the microprocessor.

Microprocessor Interface DS1 Mode (continued)

I/O Timing

The I/O timing specifications for the microprocessor interface are given in Table 14. The microprocessor interface pins use CMOS I/O levels. All outputs, except the address/data bus AD[7:0], are rated for a capacitive load of 50 pF. The AD[7:0] outputs are rated for a 100 pF load. The minimum read and write cycle time is 200 ns for all device configurations.

Table 14. Microprocessor Interface I/O Timing Specifications

Symbol	Configuration	Parameter	Setup (ns) (Min)	Hold (ns) (Min)	Delay (ns) (Max)
t1	Modes 1 & 2	Address Valid to $\overline{AS}$ Asserted (Read, Write)	5	—	—
t2		$\overline{AS}$ Asserted to Address Invalid (Read, Write)	—	10	—
t3		$\overline{AS}$ Asserted to $\overline{DS}$ Asserted	0	—	—
t4		R/$\overline{W}$ High (Read) to $\overline{DS}$ Asserted	25	—	—
t5		$\overline{DS}$ Asserted (Read, Write) to $\overline{DTACK}$ Asserted	—	—	20
t6		$\overline{DTACK}$ Asserted to Data Valid (Read)	—	—	24
t7		$\overline{DS}$ Asserted (Read) to Data Valid	—	—	44
t8		$\overline{DS}$ Negated (Read, Write) to $\overline{AS}$ Negated	—	—	—
t9		$\overline{DS}$ Negated (Read) to Data Invalid	—	—	15
t10		$\overline{DS}$ Negated (Read) to $\overline{DTACK}$ Negated	—	—	15
t11		$\overline{AS}$ (Read, Write) Asserted Width	—	75	—
t12		$\overline{DS}$ (Read) Asserted Width	—	35	—
t13		$\overline{AS}$ Asserted to R/$\overline{W}$ Low (Write)	7	—	—
t14		R/$\overline{W}$ Low (Write) to $\overline{DS}$ Asserted	20	—	—
t15		Data Valid to $\overline{DS}$ Asserted (Write)	7.5	—	—
t16		$\overline{DS}$ Negated to $\overline{DTACK}$ Negated (Write)	—	—	20
t17		$\overline{DS}$ Negated to Data Invalid (Write)	—	—	7.5
t18		$\overline{DS}$ (Write) Asserted Width	—	35	—
t19	Modes 3 & 4	Address Valid to ALE Asserted Low (Read, Write)	15	—	—
t20		ALE Asserted Low (Read, Write) to Address Invalid	—	10	—
t21		ALE Asserted Low to $\overline{RD}$ Asserted (Read)	30	—	—
t22		$\overline{RD}$ Asserted (Read) to Data Valid	—	—	90
t23		$\overline{RD}$ Asserted (Read) to RDY Asserted	—	—	75
t24		$\overline{RD}$ Negated to Data Invalid (Read)	—	—	25
t25		$\overline{RD}$ Negated to RDY Negated (Read)	—	—	25
t26		ALE Asserted Low to $\overline{WR}$ Asserted (Write)	35	—	—
t27		$\overline{CS}$ Asserted to RDY Asserted Low	—	—	16
t28		Data Valid to $\overline{WR}$ Asserted (Write)	25	—	—
t29		$\overline{WR}$ Asserted (Write) to RDY Asserted	—	—	73
t30		$\overline{WR}$ Negated to RDY Negated (Write)	—	—	22
t31		$\overline{WR}$ Negated to Data Invalid	—	25	—
t32		ALE Asserted (Read, Write) Width	—	150	—
t33		$\overline{RD}$ Asserted (Read) Width	—	100	—
t34		$\overline{WR}$ Asserted (Write) Width	—	100	—

The read and write timing diagrams for all four microprocessor interface modes are shown in Figures 8—15.

Microprocessor Interface DS1 Mode (continued)

I/O Timing (continued)

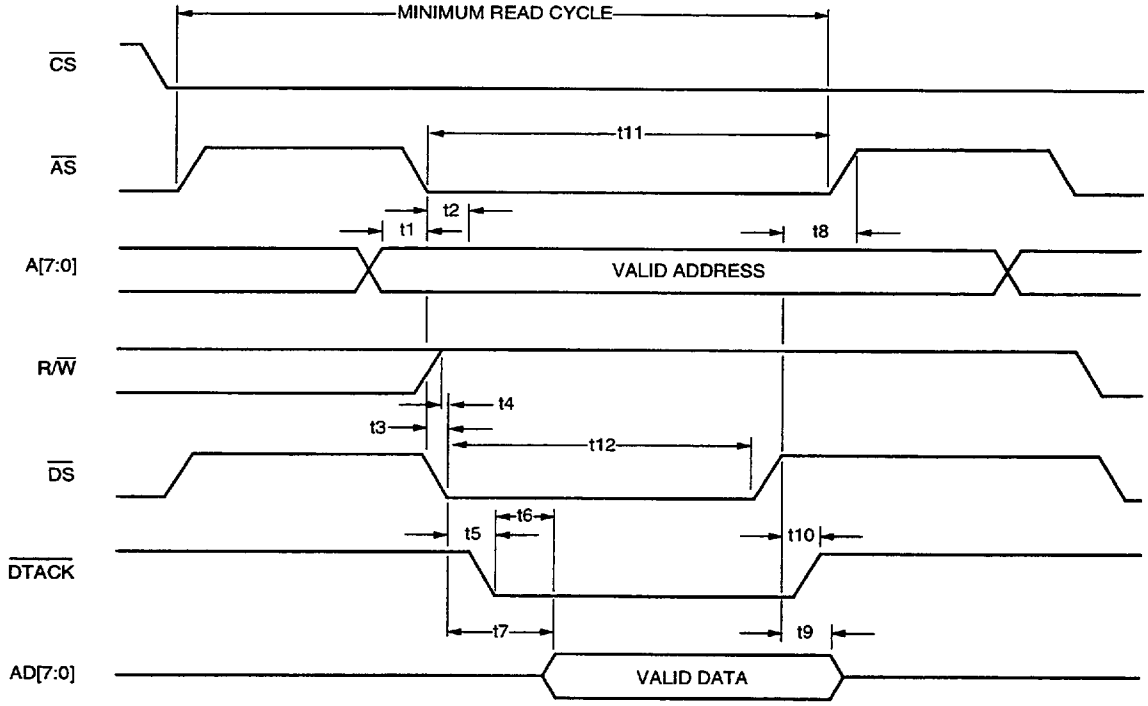

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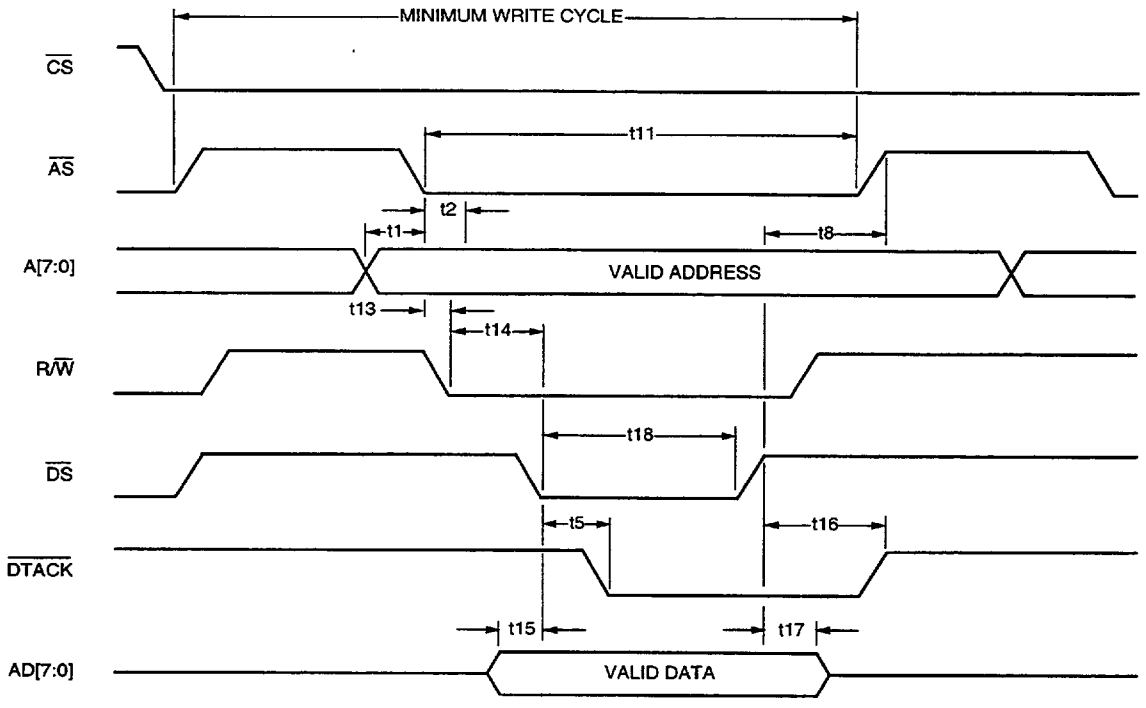
Figure 8. Mode 1—Read Cycle Timing (MPMODE = 0, MPMUX = 0)



5-3686(C).b

Figure 9. Mode 1—Write Cycle Timing (MPMODE = 0, MPMUX = 0)

Microprocessor Interface DS1 Mode (continued)

I/O Timing (continued)

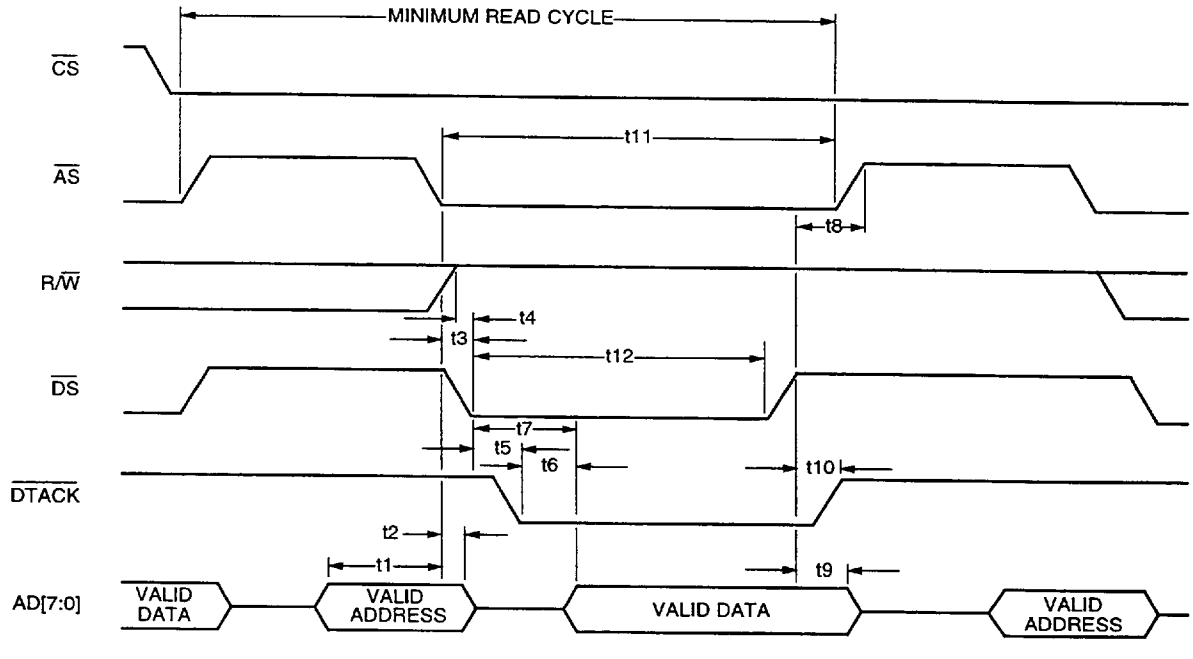


Figure 10. Mode 2—Read Cycle Timing (MPMODE = 0, MPMUX = 1)

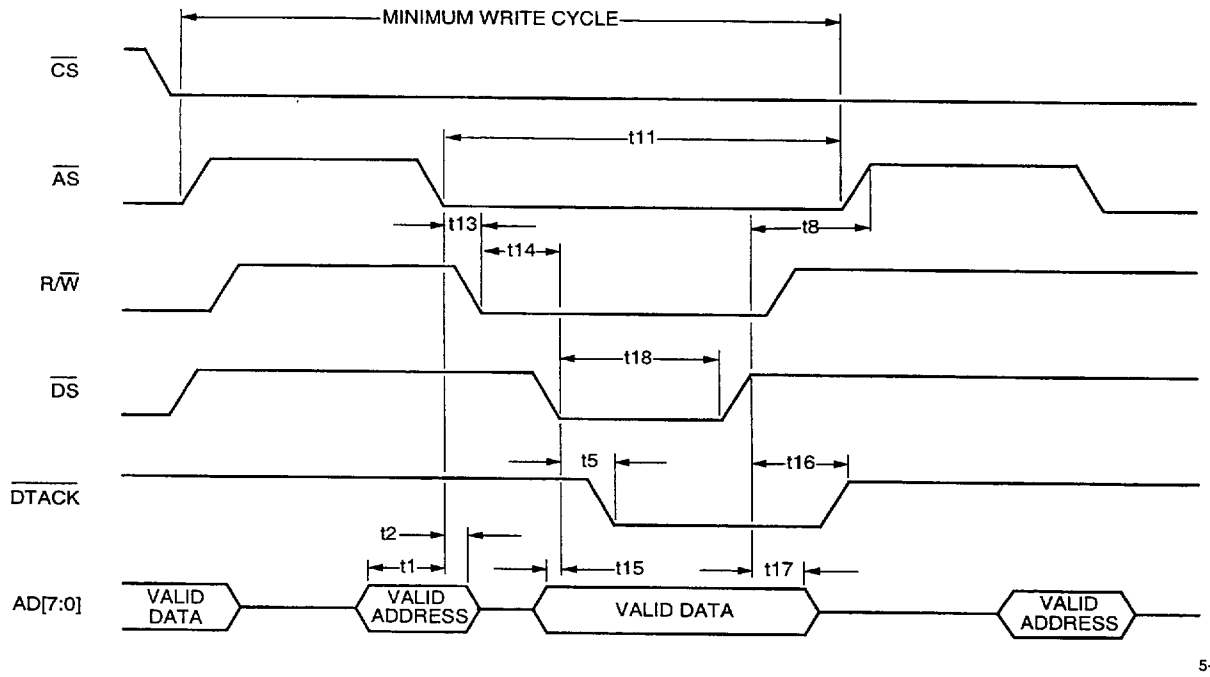


Figure 11. Mode 2—Write Cycle Timing (MPMODE = 0, MPMUX = 1)

Microprocessor Interface DS1 Mode (continued)

I/O Timing (continued)

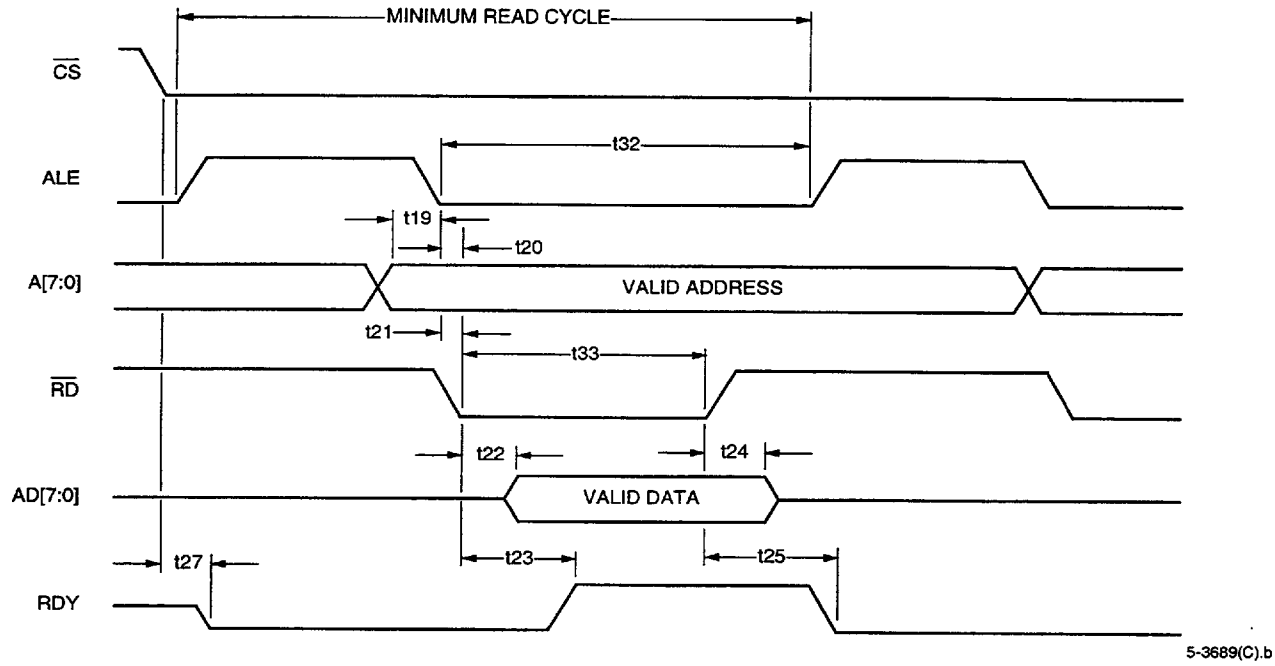


Figure 12. Mode 3—Read Cycle Timing (MPMODE = 1, MPMUX = 0)

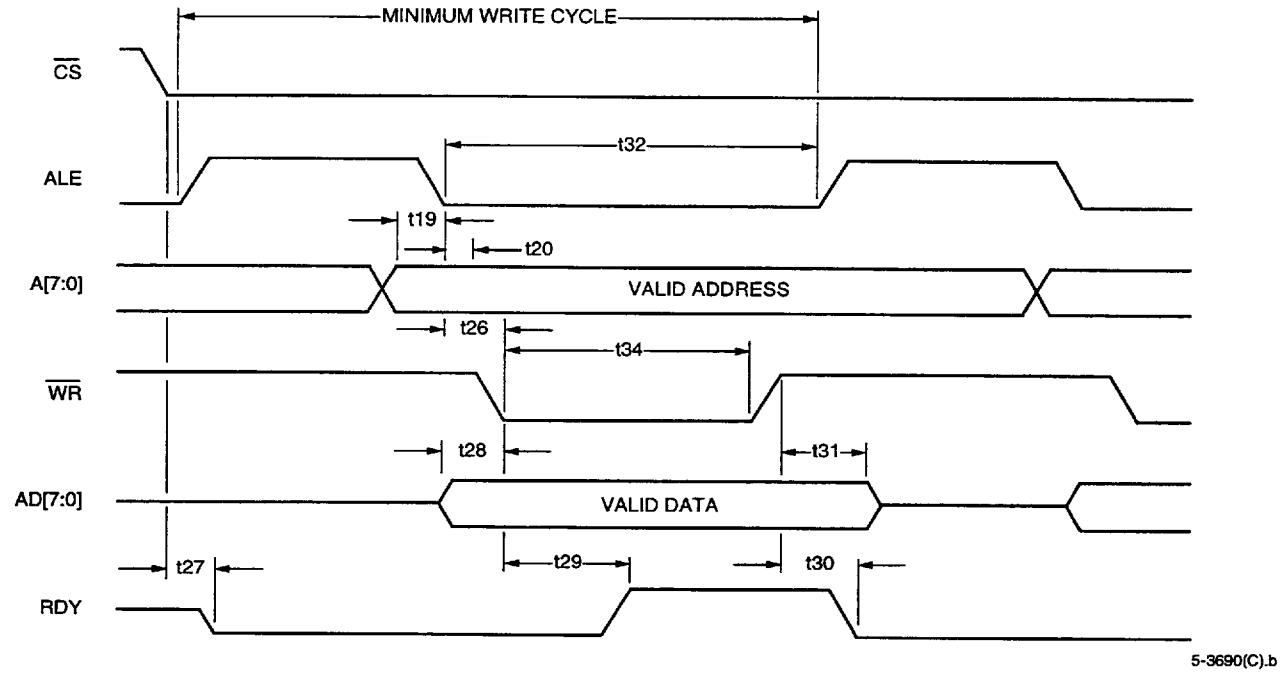


Figure 13. Mode 3—Write Cycle Timing (MPMODE = 1, MPMUX = 0)

Microprocessor Interface DS1 Mode (continued)

I/O Timing (continued)

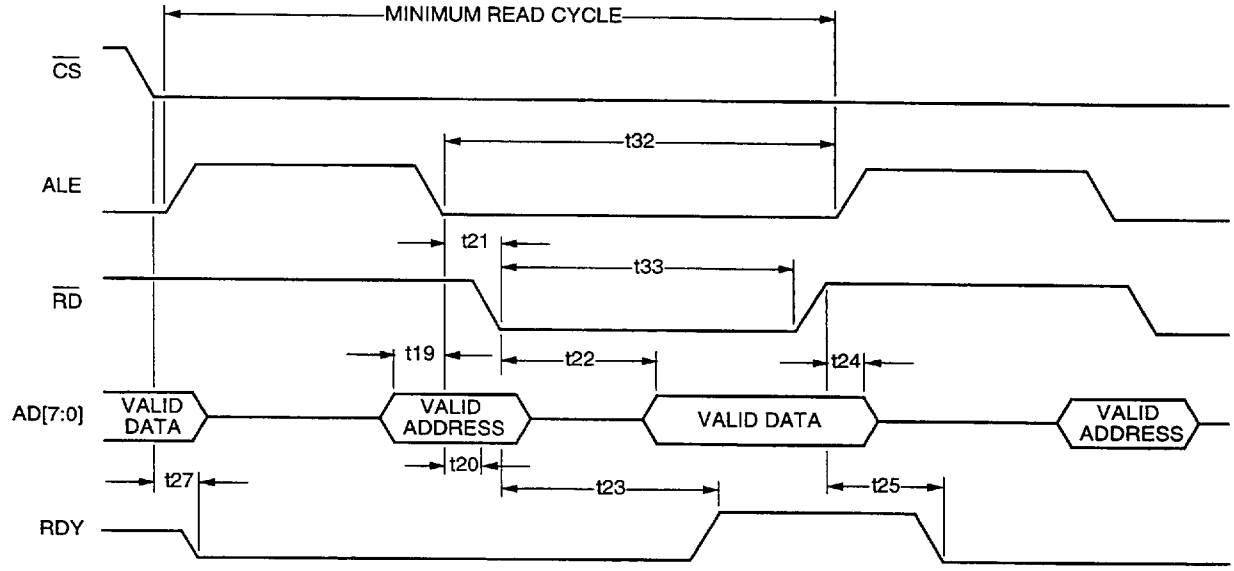


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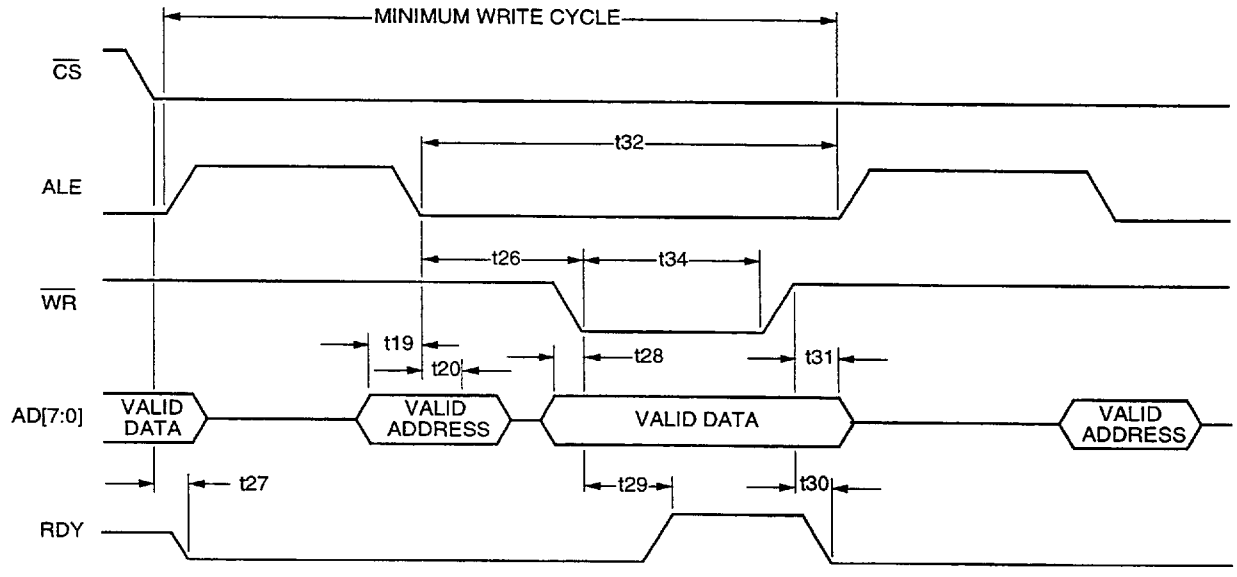
Figure 14. Mode 4—Read Cycle Timing (MPMODE = 1, MPMUX = 1)



5-3692(C)r.3

Figure 15. Mode 4—Write Cycle Timing (MPMODE = 1, MPMUX = 1)

Absolute Maximum Ratings DS1 Mode

Stresses in excess of the absolute maximum ratings can cause permanent or latent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of this device specification. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Table 15. Absolute Maximum Ratings

Parameter	Min	Max	Unit
dc Supply Voltage	–0.5	6.5	V
Storage Temperature	–65	125	°C
Maximum Voltage with Respect to VDD	—	0.5	V
Minimum Voltage with Respect to GND	–0.5	—	V

Handling Precautions DS1 Mode

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. Lucent employs a human-body model (HBM) and charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used in the defined model. No industry-wide standard has been adopted for the CDM. However, a standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely used and, therefore, can be used for comparison purposes. The HBM ESD threshold presented here was obtained by using these circuit parameters.

Table 16. ESD Threshold Voltage

Device	Voltage
TMPR28051	TBD

Operating Conditions DS1 Mode

Table 17. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Ambient Temperature	TA	–40	—	85	°C
Power Supply	VDD	4.75	5.0	5.25	V

Timing Characteristics DS1 Mode

Table 18. Logic Interface Characteristics

An internal 100 kΩ pull-up is provided on the $\overline{ICT}$, $\overline{RESET}$, $\overline{CS}$, TCLK, TDI, TMS, $\overline{TRST}$, RSTS1DATA[7:0], RSTS1PAR, MPCLK, RCLKx, and RDATAx pins. This requires these input pins to sink no more than 20 µA. All buffers use CMOS levels.

Parameter	Symbol	Test Conditions	Min	Max	Unit
Input Voltage: Low High	 V_{IL} V_{IH}	—	 GND V_{DD} – 1.0	 1.0 V_{DD}	 V V
Input Leakage	I_L	—	—	1.0	µA
Output Voltage: Low High	 V_{OL} V_{OH}	 –5.0 mA 5.0 mA	 GND V_{DD} – 1.0	 0.5 V_{DD}	 V V
Input Capacitance	C_I	—	—	3.0	pF
Load Capacitance*	C_L	—	—	25	pF

* 100 pF allowed for AD[7:0] (pins 48 to 50 and 55 to 59).

Timing Characteristics DS1 Mode (continued)

The generic digital system interface timing is shown in Figure 16. Table 19 lists the setup time (t_{SU}) and hold time (t_H) specifications for the transmission path data as well as the propagation delay (t_{PD}) information for the transmission path data.

Table 19. Generic Interface Data Timing

Symbol	Signal	Parameter	Min	Typ	Max	Unit
t_{SU}	RDATA[28:1]	RDATA[28:1]↑↓ to RCLK*[28:1]↑↓	50	—	—	ns
t_H		RDATA[28:1]↑↓ from RCLK*[28:1]↑↓	40	—	—	ns
t_{SU}	RSTS1DATA[7:0]	RSTS1DATA[7:0]↑↓ to RSTS1CLK*↑↓	15	—	—	ns
t_H		RSTS1DATA[7:0]↑↓ from RSTS1CLK*↑↓	2	—	—	ns
t_{SU}	RSTS1PAR	RSTS1PAR↑↓ to RSTS1CLK*↑↓	15	—	—	ns
t_H		RSTS1PAR↑↓ from RSTS1CLK*↑↓	2	—	—	ns
t_{SU}	RSTS1SERIAL	RSTS1SERIAL↑↓ to RSTS1CLK*↑↓	5	—	—	ns
t_H		RSTS1SERIAL↑↓ from RSTS1CLK*↑↓	2	—	—	ns
t_{SU}	TSTS1SYNC	TSTS1SYNC↑↓ to TSTS1CLKIN*↑↓	5	—	—	ns
t_H		TSTS1SYNC↑↓ from TSTS1CLKIN*↑↓	2	—	—	ns
t_{SU}	TDI	TDI↑↓ to TCLK↑	50	—	—	ns
t_H		TDI↑↓ from TCLK↑	50	—	—	ns
t_{PD}	TDATA[28:1]	From TCLK*[28:1]↑↓ to TDATA[28:1]↑↓	40	—	190	ns
t_{PD}	TSTS1DATA[7:0]	From TSTS1CLKIN↑ to TSTS1DATA[7:0]↑↓	2	—	12	ns
t_{PD}	TSTS1PAR	From TSTS1CLKIN↑ to TSTS1PAR↑↓	2	—	12	ns
t_{PD}	TSTS1DATA7	From TSTS1CLKOUT†↑ to TSTS1DATA7↑↓	0	—	3.5	ns
t_{PD}	TDO	From TCLK↓ to TDO↑↓	1.5	—	7	ns

* These clock edges are programable through the microprocessor interface.

† The duty cycle distortion added to the TSTS1CLKOUT signal is ≤2% worst case when measured from 1.5 V in to 1.5 V out with a 2 ns rise time input.

Notes:

↑ represents a low-to-high transition.

↓ represents a high-to-low transition.

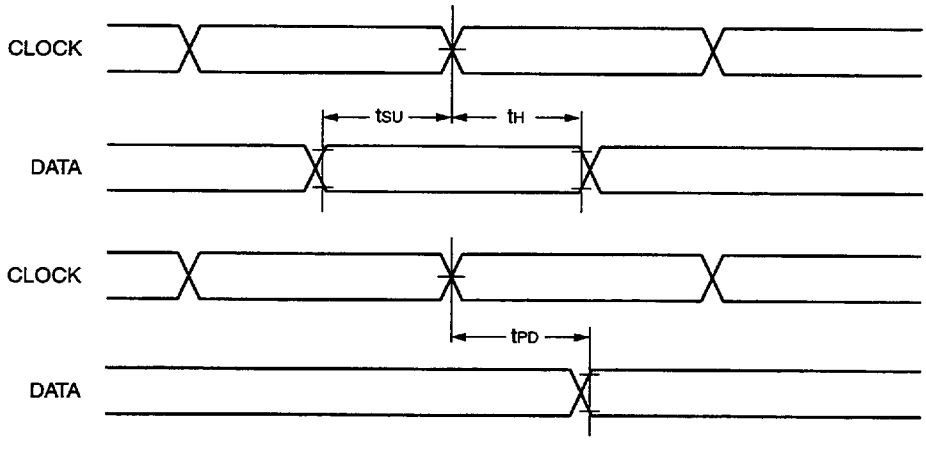


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Figure 16. Generic Interface Data Timing

Description of E1 Mode

The TMPR28051 device provides all of the functions necessary to insert and drop up to 21 asynchronous E1 signals into an SDH AU-3. On the AU-3 side, the device can be configured for either a serial bit stream or an 8-bit parallel input bus. This allows the device to drive a serial signal directly or to allow for modular growth in terminal or add/drop applications. On the E1 side, the device is designed to interface with the Lucent T7690 Quad Line Transceiver, or equivalent, using the internal jitter attenuator buffer for PLL-free operation.

Built-in loopbacks at both the AU-3 and E1 sides provide maximum flexibility for use in a number of SDH/E1 products including terminal multiplexers, add/drop multiplexers, and digital cross connects.

A high-speed microprocessor interface and full user programmability on E1 to TU-12 slot insertion and drop provide maximum flexibility for E1 I/O configuration.

Block Diagram E1 Mode

The E1 mode block diagram is shown in Figure 17. For illustration purposes, only two of the 21 E1 bidirectional blocks are shown.

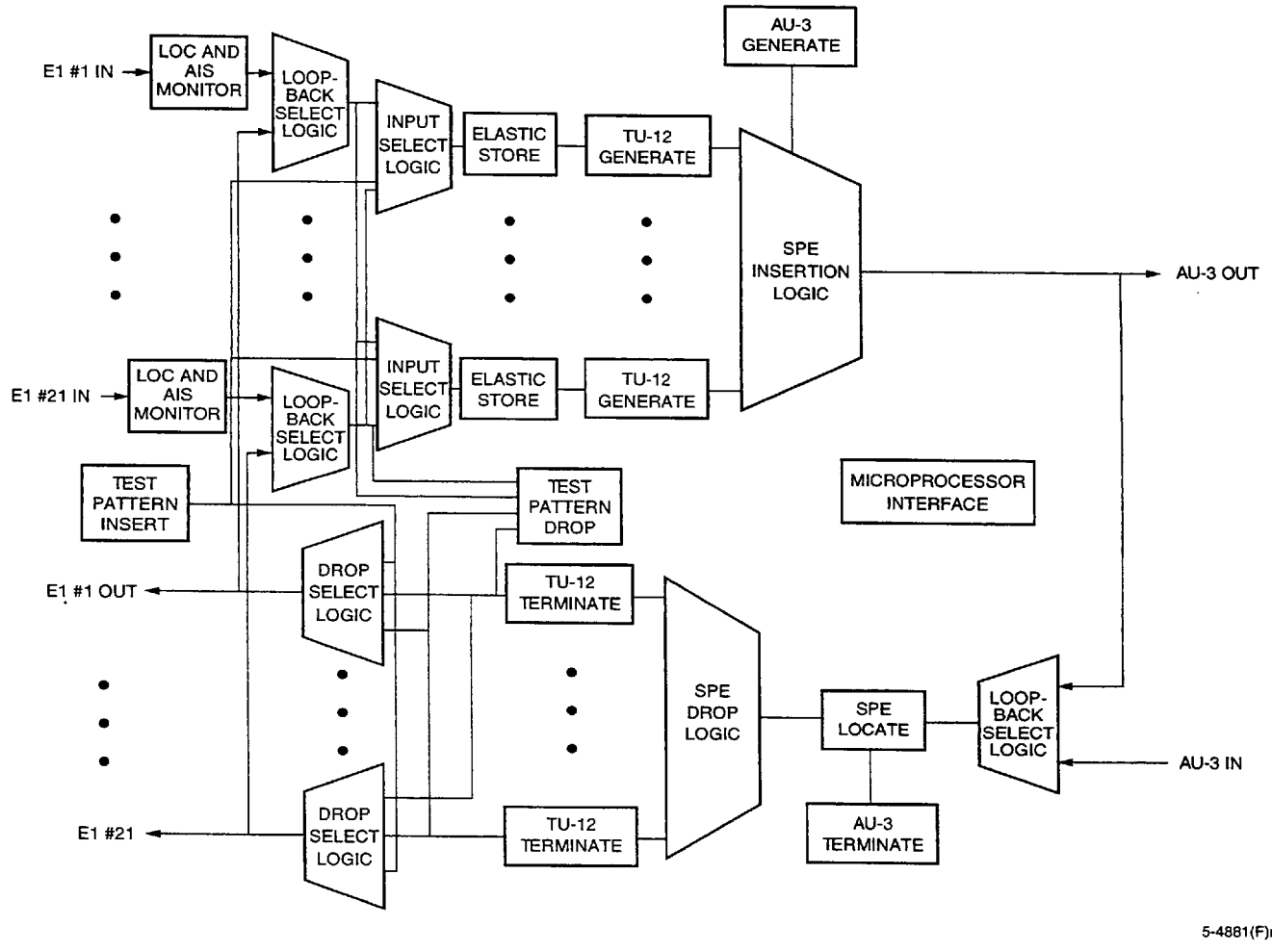

Figure 17. Block Diagram E1 Mode

Pin Information E1 Mode

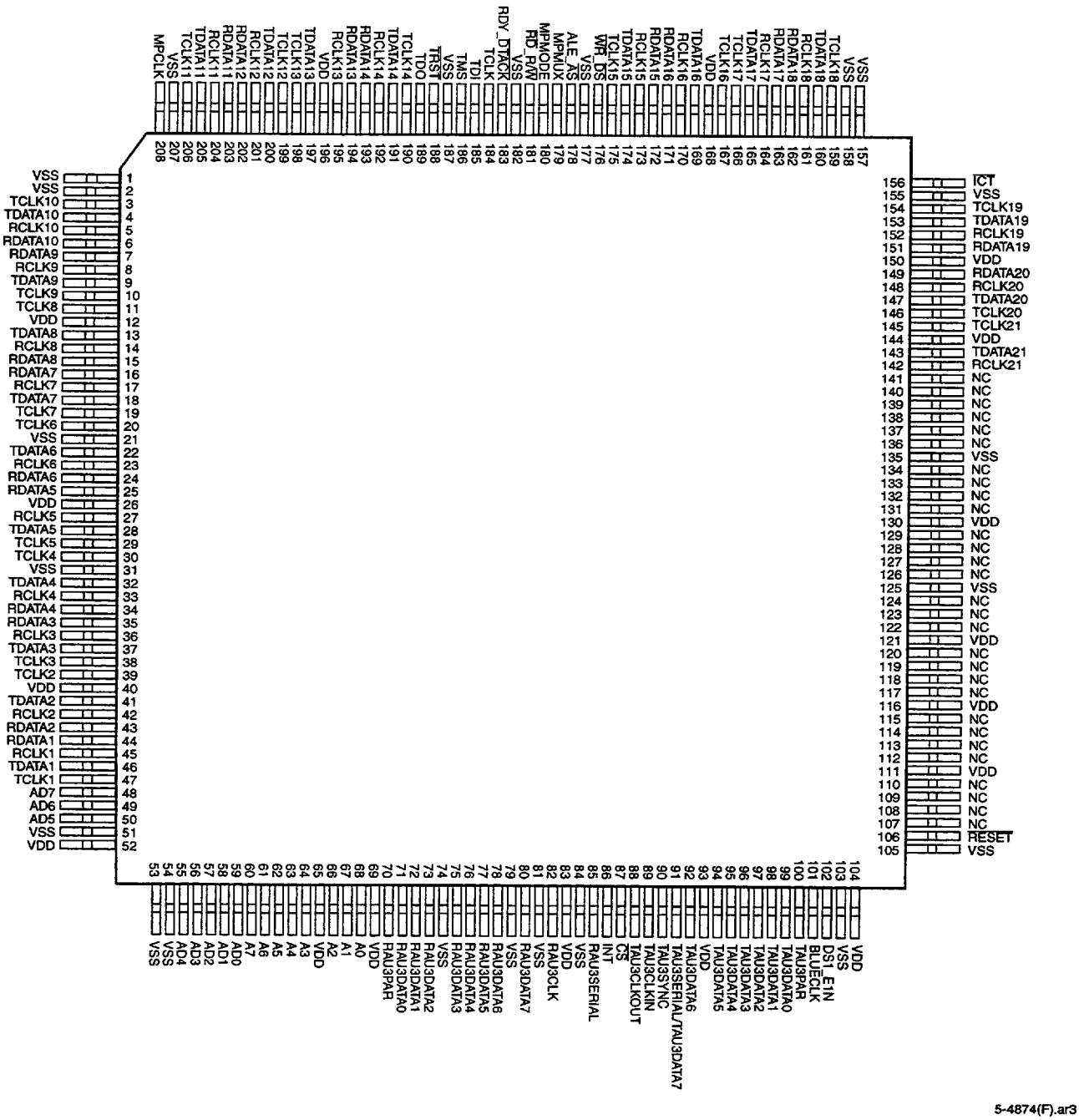

Figure 18. Device Pinout E1 Mode

Pin Information E1 Mode (continued)

Table 20. Pin Descriptions E1 Mode

Pin	Symbol	Type*	Name/Description
47, 39, 38, 30, 29, 20, 19, 11, 10, 3, 206, 199, 198, 190, 175, 167, 166, 159, 154, 146, 145	TCLK[1:21]	O	**Transmit DS1 Clock.** Gapped DS1 clock (not 50% duty cycle).
46, 41, 37, 32, 28, 22, 18, 13, 9, 4, 205, 200, 197, 191, 174, 169, 165, 160, 153, 147, 143	TDATA[1:21]	O	**Transmit DS1 Data.** Transmit data to the LIU.
45, 42, 36, 33, 27, 23, 17, 14, 8, 5, 204, 201, 195, 192, 173, 170, 164, 161, 152, 148, 142	RCLK[1:21]	I^u	**Receive DS1 Clock.** Received clock from the LIU. An internal 100 kΩ pull-up is on these pins.
44, 43, 35, 34, 25, 24, 16, 15, 7, 6, 203, 202, 194, 193, 172, 171, 163, 162, 151, 149, 141	RDATA[1:21]	I^u	**Receive DS1 Data.** Received data from the LIU. An internal 100 kΩ pull-up is on these pins.
102	DS1_E1N	I	**DS1/E1 Input Identifier.** If this pin is pulled high, the device acts as a DS1 to STS-1 mapping device. If pulled low, it acts as an E1 to AU-3 mapper.
101	BLUECLK	I	**Blue Signal Clock.** In the event of a loss of input DS1 clock or an unprovisioned DS1 output, this clock signal is used to generate the DS1 blue signal (all 1s). This clock must be 1.544 MHz ± 32 ppm.
176	$\overline{WR\_DS}$	I	**Write (Active-Low).** If MPMODE = 1 (pin 180), this pin is asserted low by the microprocessor to initiate a write cycle. **Data Strobe (Active-Low).** If MPMODE = 0, this pin becomes the data strobe for the microprocessor. When R/$\overline{W}$ = 0 (write), a low applied to this pin latches the signal on the data bus into internal registers.
179	MPMUX	I	**Microprocessor Multiplex Mode.** Setting MPMUX = 1 allows the microprocessor interface to accept the multiplexed address and data signals. Setting MPMUX = 0 allows the microprocessor interface to accept demultiplexed (separate) address and data signals.
180	MPMODE	I	**Microprocessor Mode.** When MPMODE = 1, the device uses the address latch enable type microprocessor read/write protocol with separate read and write controls. Setting MPMODE = 0 allows the device to use the address strobe type microprocessor read/write protocol with a separate data strobe and a combined read/write control.

* I^u indicates an internal pull-up.

Pin Information E1 Mode (continued)

Table 20. Pin Descriptions E1 Mode (continued)

Pin	Symbol	Type*	Name/Description
181	$\overline{RD}\_R/\overline{W}$	I	**Read (Active-Low).** If MPMODE = 1 (pin 180), this pin is asserted low by the microprocessor to initiate a read cycle. **Read/Write.** If MPMODE = 0, this pin is asserted high by the microprocessor to indicate a read cycle or asserted low to indicate a write cycle.
178	ALE_$\overline{AS}$	I	**Address Latch Enable.** If MPMODE = 1 (pin 180), this pin becomes the address latch enable for the microprocessor. When this pin transitions from high to low, the address bus inputs are latched into the internal registers. **Address Strobe (Active-Low).** If MPMODE = 0, this pin becomes the address strobe for the microprocessor. When this pin transitions from high to low, the address bus inputs are latched into the internal registers.
87	$\overline{CS}$	I^u	**Chip Select (Active-Low).** This pin is asserted low by the microprocessor to enable the microprocessor interface. If MPMUX = 1 (pin 179), $\overline{CS}$ can be externally tied low to use the internal chip selection function (see Microprocessor Configuration Modes section on page 61). An internal 100 kΩ pull-up is on this pin.
86	INT	O	**Interrupt.** This pin is asserted high to indicate an interrupt produced by an alarm condition in register 3 or 5. The activation of this pin can be masked by microprocessor registers 4 and 6.
183	RDY_$\overline{DTACK}$	O	**Ready.** If MPMODE = 1 (pin 180), this pin is asserted high to indicate the device has completed a read or write operation. This pin is in a high-impedance state when $\overline{CS}$ (pin 87) is high. **Data Transfer Acknowledge (Active-Low).** If MPMODE = 0, this pin is asserted low to indicate the device has completed a read or write operation.
106	$\overline{RESET}$	I^u	**Hardware Reset (Active-Low).** If $\overline{RESET}$ is forced low, all internal states in the transceiver paths are reset and data flow through each channel will be interrupted (see Device-Level Control, Alarm, and Mask Bits (0x00—0x16) section on page 75). An internal 100 kΩ pull-up is on this pin.
156	$\overline{ICT}$	I^u	**In-Circuit Test Control (Active-Low).** If $\overline{ICT}$ is forced low, certain output pins are placed in the high-impedance state. An internal 100 kΩ pull-up is on this pin.
48—50, 55—59	AD[7:0]	I/O	**Microprocessor Interface Address/Data Bus.** If MPMUX = 0 (pin 180), these pins become the bidirectional, 3-statable data bus. If MPMUX = 1, these pins become the multiplexed address/data bus. In this mode, only the lower 7 bits (AD[6:0]) are used for the internal register addresses.
60—64, 66—68	A[7:0]	I	**Microprocessor Interface Address.** If MPMUX = 0 (pin 180), these pins become the address bus for the microprocessor interface registers.
208	MPCLK	I^u	**Microprocessor Interface Clock.** Microprocessor interface clock rates from twice the E1 line clock rate (4.096 MHz) to 16.384 MHz are supported. An internal 100 kΩ pull-up is on this pin.
184	TCLK	I^u	**JTAG Clock.** An internal 100 kΩ pull-up is on this pin.
185	TDI	I^u	**JTAG Input Data.** An internal 100 kΩ pull-up is on this pin.
186	TMS	I^u	**JTAG Mode Select.** An internal 100 kΩ pull-up is on this pin.
188	$\overline{TRST}$	I^u	**JTAG Reset (Active-Low).** An internal 100 kΩ pull-up is on this pin.
189	TDO	O	**JTAG Output Data.**

* I^u indicates an internal pull-up.

Pin Information E1 Mode (continued)

Table 20. Pin Descriptions E1 Mode (continued)

Pin	Symbol	Type*	Name/Description
89	TAU3CLKIN	I	**Transmit AU-3 Clock.** The AU-3 clock can be 51.84 MHz for serial input data or 6.48 MHz for byte wide data.
90	TAU3SYNC	I	**Transmit AU-3 Sync.** The AU-3 sync pulse can be provisioned to be active on either the first or last clock of the AU-3 frame.
92, 94—99	TAU3DATA[6:0]	O	**Transmit AU-3 Data.** In the byte wide output mode this is bit 6—bit 0 of the data bus. TAU3DATA7 is the most significant bit of the input byte.
100	TAU3PAR	O	**Transmit AU-3 Parity.** The parity output is only defined for byte wide data. The device can be provisioned to source either an odd or even parity.
91	TAU3SERIAL/ TAU3DATA7	O	**Transmit AU-3 Serial Data/Transmit AU-3 Data Bit 7 (MSB).** In serial mode this pin provides 51.84 Mbits/s serial data. In parallel mode this pin provides TAU3DATA7.
88	TAU3CLKOUT	O	**Transmit AU-3 Output Clock.**
82	RAU3CLK	I	**Receive AU-3 Clock.** The AU-3 clock can be 51.84 MHz for serial input data or 6.48 MHz for byte wide data.
80, 78—75, 73—71	RAU3DATA[7:0]	I^u	**Receive AU-3 Data.** If the device is operating in the serial mode, then RAU3DATA7 is used as the input data pin. In the byte wide input mode, RAU3DATA7 is the most significant bit of the input byte. An internal 100 kΩ pull-up is on this pin.
70	RAU3PAR	I^u	**Receive AU-3 Parity.** The parity input is only defined for byte wide data. The device can be provisioned to accept either an odd or even parity. An internal 100 kΩ pull-up is on this pin.
85	RAU3SERIAL	I	**Receive AU-3 Serial Data.** If the device is operating in the serial mode, then RSERIAL is used as the input data pin.
1, 2, 21, 31, 51, 53, 54, 74, 79, 81, 84, 103, 105, 125, 135, 155, 157, 158, 177, 182, 187, 207	V_{SS}	I	**Ground Reference for Digital Circuitry.**
12, 26, 40, 52, 65, 69, 83, 93, 104, 111, 116, 121, 130, 144, 150, 168, 196	V_{DD}	I	**Power Supply for Digital Circuitry.**
107—110, 112—115, 117—120, 122—124, 126—129, 131—134, 136—141	NC	—	**No Connect.**

* I^u indicates an internal pull-up.

E1 to AU-3

In the descriptions below, some of the control bits exist for each of the E1 or TU-12 signals. These signals are indicated by x to show that there are actually 21 of them in the register map.

LOC & AIS Monitor

The incoming E1 signal is first checked for loss of clock (LOC). LOC is reported to the microprocessor via the E1LOCx bit (LOC = 1, 0 otherwise). The device inserts E1 AIS (all 1s) using the blue signal clock if LOC is present.

The incoming E1 data (TDATA[21:1]) is retimed immediately by the associated E1 clock (TCLK[21:1]). The edge of the clock that is used to retime the data is user provisionable at the device level to either the rising edge (TXE1EDGE = 1) or falling edge (TXE1EDGE = 0).

After being retimed, the incoming data stream is checked for AIS. The device will declare AIS if the input data is logic 1 for 512 consecutive clocks. The device will withstand up to one error in the 512 bits. AIS is reported to the microprocessor via the E1AISx bit (AIS = 1, 0 otherwise).

The blue signal clock that is input to the device can be at the exact E1 rate (2.048 MHz), or at 16 times the E1 rate (32.768 MHz). This allows users of the T7690 devices to reuse the XCLK on the board. The TMPR28051 is provisioned to accept the exact E1 rate by default (BLUECLKSEL = 0), but can be changed to perform the divide by 16 function (BLUECLKSEL = 1).

E1 Loopback Select Logic

The first stage after retiming the signal into the device is selection of the received E1 (E1xLB = 0) or the looped back E1 (E1xLB = 1). This selection is provisionable per E1 input (21 total).

Input Select Logic

Once the E1 data sources have been selected, the E1 for each TU-12 tributary is selected. This selection requires 5 bits per slot to determine which E1 input to use. The numbering scheme for the five provisioned bits ranges from 00001 to 10101 where the binary value of the 5 bits corresponds to the E1 input. For instance, the value 00001 corresponds to selecting E1 #1.

The unused value of 00000 results in TU unequipped being transmitted. This is the default value for all the TU-12 slots at powerup. TU unequipped is a valid pointer and all zero payload.

The unused values of 10110—11110 will cause TUAIS to be inserted for that TU-12 slot. The value of 11111 will cause the internally generated test pattern to be inserted for that TU-12 slot.

There are no restrictions on the number of TU-12 slots that any given E1 input can supply (i.e., up to 21 TU-12 slots can select the same E1 input).

This block can also be used to insert the test pattern (see Test Pattern E1 Mode section on page 57).

Elastic Store

The selected E1 clock and data signals are fed to an elastic store that is used to synchronize the incoming E1 to the local AU-3 clock. This block determines the need for positive/zero/negative (P/Z/N) stuffing for each E1. Data out of this block is synchronized to the local transmit AU-3 clock (TAU3CLK).

This block allows the device to accept E1 signals at 2.048 Mbits/s ± 130 ppm with up to ±5 unit intervals peak jitter.

TU-12 Generate

This block generates the TU-12 superframe. Unless TUAIS is being forced, the superframe is built with a fixed output pointer value of decimal 105 in all the TU-12 slots. The TU size field is set to 10 and the new data flag is set to 0110. This corresponds to 0110100011001001 (0x68C9) for the V1 and V2 bytes.

This block takes the E1 data and places it into the TU-12. It's in this block that the TU-12 overhead is generated. The format of the TU-12 overhead byte, V5, is shown in Table 21.

Table 21. TU-12 Overhead Byte Format

Bit #	1	2	3	4	5	6	7	8
	BIP-2		FEBE	RFI	Signal Label			FERF

Each TU-12 can be provisioned to insert TUAIS (TUAISx = 1). TUAIS consists of overwriting the entire TU-12 payload and overhead with ones.

E1 to AU-3 (continued)

TU-12 Generate (continued)

RFI and FERF (RDIx[1:0]INS) can be automatically inserted by the device or written into the V5 byte under control of the microprocessor. In the automatic mode, the value for bits 4 and 8 are defined in Table 3.

Table 22. TU RDI Description

Bit 4	Bit 8	Description
0	0	No alarm
0	1	AIS-V or LOP-V
1	0	TU payload mismatch
1	1	VC unequipped

The label for each VC1 is also provisionable (VCLAB[2:0]INSx) by the microprocessor.

This block also automatically generates the BIP-2 signal. Each TU-12 can be configured to intentionally insert BIP-2 errors for troubleshooting purposes (BIP2ERRINSx = 1).

The device can be configured such that any detected BIP-2 errors in the TU-12 receive side result in FEBE being written into the corresponding transmit TU-12 slot (TUFEBE_EN = 1).

The resultant TU-12 superframe is shown here:

V1
V5
RRRRRRRR
Byte 1
.
.
Byte 32
RRRRRRRR
V2
RRRRRRRR
C1C2OOOORR
Byte 1
.
.
Byte 32
RRRRRRRR
V3
RRRRRRRR
C1C2OOOORR
Byte 1
.
.
Byte 32
RRRRRRRR
V4
RRRRRRRR
C1C2RRRRRS1
S2 Byte 1[6:0]
.
.
Byte 32
RRRRRRRR

Where:

I = information bit
O = overhead bit
R = fixed stuff
V1, V2, V3 = pointer and pointer action bytes
S1, S2 = stuff opportunity bits
V4 = reserved
C1, C2 = stuff indication bits
V5 = TU-12 overhead byte

AU-3 Generate

The device generates an AU-3 signal based on an incoming clock (TAU3CLK) and frame sync pulse (TAU3SYNC). The relationship of the incoming frame sync pulse to the output frame can be provisioned such that the sync pulse occurs on either the first clock of

E1 to AU-3 (continued)

AU-3 Generate (continued)

the frame (TXFSYNC = 0) or the last clock of the frame (TXFSYNC = 1). In the absence of an incoming frame sync, the device will freewheel the output sync to the last good frame sync pulse, or to the internal counter in the case that no sync pulses were supplied.

The SDH AU-3 frame is 9 rows x 90 columns that repeats at an 8 kHz rate. Each column is one byte wide. The SDH AU-3 frame contains three columns of transport overhead, one column of path overhead, and 86 columns of payload.

The 36 bytes of SDH overhead are allocated as shown in Table 23.

Table 23. AU-3 Overhead Byte Allocation

	Col. 1	Col. 2	Col. 3	Col. 4
Row 1	A1	A2	C1	J1
Row 2	B1	E1	F1	B3
Row 3	D1	D2	D3	C2
Row 4	H1	H2	H3	G1
Row 5	B2	K1	K2	F2
Row 6	D4	D5	D6	H4
Row 7	D7	D8	D9	Z3
Row 8	D10	D11	D12	Z4
Row 9	Z1	Z2	E2	Z5

The overhead bytes that are inserted by the device are described below. All of the remaining overhead bytes are given a fixed value of all ones.

The device inserts the frame pattern of F628 hex into the A1 and A2 bytes.

The device inserts a value of 0x01 into the C1 byte.

The device generates and inserts valid B1, B2, and B3 BIP even parity bytes in the AU-3 overhead. These bytes are forced to odd parity when BxERRINS = 1.

The device will provide an AU-3 pointer with a fixed value of 522 with 0110 in the NDF bits and 10 in the SS bits. This pointer value indicates that the J1 path overhead byte follows immediately after the C1 line overhead byte.

The J1 byte is used for path trace. This byte repetitively transmits a 64-byte fixed length sequence to verify end-to-end connectivity. These 64 bytes are programmable by the microprocessor (TJ1BYTEx). The method for programming these bits is described in detail in the Microprocessor Interface Register Architecture section on page 64.

The F2 byte can be provisioned by the microprocessor (F2INS[7:0]).

The device inserts a value of 0x02 into the C2 byte indicating VT structured AU-3 SPE.

The three least significant bits of the K2 byte can be provisioned by the microprocessor (K2INS[2:0]).

The Z2 byte is used to report B2 FEBE when FEBE_EN = 1. These bits contain the number of errors seen by the current frames receive B2 BIP-8 when FEBE_EN = 1. Valid values for these 4 bits are 0000—1000.

The G1 byte is used to convey path condition and performance back to the far end. The format of the G1 byte is shown in Table 24.

Table 24. G1 Path Condition/Performance Byte Format

Bit #	1	2	3	4	5	6	7	8
	FEBE				RDI	Unused		

FEBE reports the number of far-end block errors. These bits contain the number of errors seen by the current frames receive B3 BIP-8. Valid values for these 4 bits are 0000—1000. The remote defect indicator (RDI) reports back such conditions as receive path AIS, signal failure, and path trace mismatch.

The H4 byte is inserted using the reduced H4 coding sequence format where the 6 MSBs are ones and the 2 LSBs alternate between 00-01-10-11-00, etc. where the value of 00 indicates that the next AU-3 SPE contains the V1 overhead byte.

The AU-3 can be provisioned to send path AIS (TXPAISINS = 1). Writing path AIS consists of writing all ones into the H1—H3 bytes and the entire SPE.

The transmitted AU-3 can be configured to scramble the output data (AU3SCR = 1) or transmit the data without scrambling (AU3SCR = 0). It is useful to turn off SDH scrambling if the data is going to be immediately multiplexed into a higher rate SDH signal. When AU3SCR = 1, the device scrambles the outgoing AU-3 frame according to the SDH frame synchronous scrambling sequence $x^7 + x^6 + 1$. The sequence is reset to 1111111 at the beginning of the byte following the C1 byte and scrambles all of the AU-3 data except the A1, A2, and C1 bytes. When this bit is 0, then the transmit data is not scrambled by the device.

E1 to AU-3 (continued)

SPE Insertion Logic

In addition to the one column of path overhead and 84 columns of TU-12 payload, the AU-3 SPE also contains two columns of fixed stuff. The path overhead is located in column #1, while column #30 and column #59 contain the fixed stuff. The remaining columns contain the interleaved TU-12 data as shown in Table 25.

Table 25. SPE Insertion Format

SPE Column #	1	2	3	4	5	6	7	8	9	10	11	•••	229	230	231	232	233	•••	571	572	573	574	575	576	•••	813	814	815	816	817	818	819	820	821	822	823	824	825	826	827
	PATH OH	TU12#1	TU12#2	TU12#3	TU12#4	TU12#5	TU12#6	TU12#7	TU12#8	TU12#9	TU12#10	TU11	•••	TU12#6	TU12#7	FIXED	TU12#8	TU12#9	•••	TU12#11	TU12#12	FIXED	TU12#13	TU12#14	TU12#15	•••	TU12#15	TU12#16	TU12#17	TU12#18	TU12#19	TU12#20	TU12#21	TU11	TU11	TU11	TU11	TU11	TU11	TU11

The SPE insertion logic block acts in conjunction with the AU-3 frame generate block to place the TU-12 information in the transmitted data stream. The device can transmit the data as either a serial bit stream (TXSERIAL = 1) or as a parallel byte of data (TXSERIAL = 0). In the parallel mode, the device sends a parity bit with the data. This parity bit is configurable to be either odd (TXPARITY = 1) or even (TXPARITY = 0) parity.

AU-3 to E1

Loopback Select Logic

The device can be configured to loopback the transmit AU-3 (AU3LB = 1) or accept the local AU-3 signal (AU3LB = 0). When the local AU-3 signal is selected, the user can configure which edge of the clock to use to retime the data (RXAU3EDGE = 1 uses the rising edge; RXAU3EDGE = 0 uses the falling edge).

AU-3 Locate

The device can receive the data as either a serial bit stream (RXSERIAL = 1) or as a parallel byte of data (RXSERIAL = 0). In the parallel mode, the device receives a parity bit with the data. This bit is configurable to odd (RXPARITY = 1) or even (RXPARITY = 0) parity. Errors in this bit are reported to the microprocessor (RXPARERR).

This block performs the functions necessary to locate the SPE. The device will frame on the incoming AU-3 signal, and indicate when it is in the out of frame (OOF) condition. The OOF is a latched condition that holds its value until read. The indication will then reset if the condition is no longer true.

AU-3 Terminate

The received AU-3 can be configured to descramble the output data (AU3DSCR = 1) or receive the data without descrambling (AU3DSCR = 0). It is useful to turn off SDH descrambling if the data is received locally from a higher rate SDH signal where descrambling has already taken place.

AU-3 to E1 (continued)

AU-3 Terminate (continued)

For performance monitoring purposes, there are a number of BIP and FEBE error counters in the receive section. All of these internal counters are comprised of a running error counter and a hold register that presents stable results to the microprocessor. The counts in all of the running counters are latched to the hold registers when LATCH_CNT is written from a logic zero to a logic 1. This also zeros out all of the running counters. The results are then held to be read by the microprocessor. All of the internal counters have the ability to store more than 1 second worth of counts; as long as the LATCH_CNT occurs every second, or faster, no counts will be lost. In case this doesn't happen, all of the running counters will hold their maximum value rather than roll over to zero.

The device performs pointer interpretation on the incoming signal to locate the start of the SONET SPE. The pointer interpretation block will indicate when the device is in the loss of pointer (LOP-P) or path AIS (AIS-P) condition.

Loss of pointer condition is declared as the result of either of the following conditions:

1. Continuous NDF. If the device receives NDF (1001) for nine consecutive frames, then LOP-P is declared.
2. Incorrect pointer size bits. The valid pointer size for TU-12 is 10. If the device receives a valid pointer with size bits other than 10, then LOP is declared.
3. Invalid pointer values. If the device receives nine consecutive frames of pointers that are not a normal value, NDF, AIS-P, increment, or decrement, then LOP is declared.

AIS-P is declared on three consecutive frames with all ones in the H1 and H2 bytes.

AIS-P and LOP-P are mutually exclusive conditions. If neither AU3PAIS or AU3LOP is logic 1, then the pointer interpreter is declaring normal pointer. As part of the normal operation, the device will respond appropriately to valid NDF, increment and decrement indications. Increment and decrement operations will be counted by the device and presented to the microprocessor (INC[7:0], DEC[7:0]).

The B1, B2, and B3 BIP-8 values are recalculated and compared to the received values. Any differences are counted by the appropriate error counter (BxCNT[15:0]). In addition, B2 and B3 FEBE errors are also counted (BxFEBE[15:0]). The running and latched counts for both B1 and B2 counters are held at zero during OOF. The running and latched counts for B3 counters are held at zero during OOF as well as LOP-P.

The J1 byte is terminated within the device. This consists of writing the receive J1 value in a set of registers modulo 64. At start-up, the receive J1 byte register is all 0. Whenever the received J1 byte value doesn't match the current J1 byte in the register, then the TRACE_MIS is set to logic 1. This allows the user to read the 64-byte register once, and then ignore it unless differences are received. TRACE_MIS is masked during AIS-P and LOP-P.

The F2 byte (F2[7:0]), the C2 byte (C2[7:0]), the three least significant bits of the K2 byte (K2[2:0]), and the four least significant bits of the G1 byte (G1[3:0]) are monitored by the microprocessor. The number of consistent, consecutive frames to update the values of all of these monitored bytes can be set by the user at anywhere between 3 and 15 frames (F2NxDET[3:0], C2NxDET[3:0], K2NxDET[3:0], G1NxDET[3:0]). None of these registers will update during OOF.

SPE Drop Logic

The SPE drop logic uses the H4 multiframe indicator to identify the TU-12 slots and drop the data to the correct TU-12 termination blocks. Loss of multiframe synchronization will be reported to the microprocessor (H4LOMF).

TU-12 Terminate

The TU-12 terminate block performs TU pointer interpretation on the received signal to locate the VC1 overhead. TULOP (TULOPx) and TUAIS (TUAISx) are reported to the microprocessor.

TULOP is declared as a result of either of the following conditions:

1. Continuous NDF. If the device receives NDF (1001) for nine consecutive superframes, then TULOP is declared.
2. Invalid pointer values. If the device receives nine frames consecutively of a pointer that is not a normal value, NDF, TUAIS, increment, or decrement, then TULOP is declared. The SS bits **do** contribute to TULOP.

TUAIS is declared on three consecutive frames with all ones in the V1 and V2 bytes.

AU-3 to E1 (continued)

TU-12 Terminate (continued)

TUAIS and TULOP are mutually exclusive conditions. If neither TUAIS or TULOP is logic 1, then the pointer interpreter is declaring normal pointer. As part of the normal operation, the device will respond appropriately by the device and presented to the microprocessor (TUx+[3:0], TUx–[3:0]).

Mismatches between the expected VT1.5 size bits, 11, and the actual received ss size bits are reported to the microprocessor (TUSIZEERx).

Once the V5 byte is located, the device checks for received BIP-2 errors (RXBIP2ERRx) and received FEBE (RXFEBEx). In addition to reporting the occurrence of BIP-2 errors and FEBE, the device also maintains a count of each of these on a per TU-12 basis (FEBECNTx and BIP2CNTx).

Additionally, the device checks for received TU RDI (VTRDIx[1:0]) and received TU label (VTLAB[2:0]). Whenever the device receives three consecutive consistent values for these fields that are different from the current values, it latches the new value and reports the change to the microprocessor.

Output Select Logic

Once the TU-12 has been terminated, the TU-12 for each E1 output is selected. This selection requires 5 bits per slot to determine which TU-12 to use (TUxDROP). The numbering scheme for the five provisioned bits ranges from 00001—10101 where the binary value of the 5 bits corresponds to the TU-12 source. For instance, the value 00001 corresponds to selecting TU-12 #1, group 1.

The unused values of 00000 and 10110—11110 will cause AIS to be inserted for that E1 output. By default, on powerup all E1 outputs reset to a value of 00000 which causes all of the E1s to transmit AIS (all 1s) using the blue signal clock (BLUECLK).

The device can accept a blue signal clock at either the exact E1 rate (BLUECLKSEL = 0), or at 16 times the E1 rate (BLUECLKSEL = 1). The clock at 16 times the E1 rate is exactly the same as the XCLK used in the Lucent T7690/T7693 quad line transceiver devices.

The unused value of 11111 is reserved for inserting the test pattern into the E1 as described below.

Test Pattern E1 Mode

The device contains a test pattern generator and a test pattern detector for use in maintenance and troubleshooting.

Test Pattern Generation

The test pattern generator is a QRSS sequence generator. The QRSS pattern is a $2^{20} - 1$ pseudorandom bit sequence defined by the equation $x^{20} + x^{17} + 1 = 0$, with a 14 zero limit. As can be seen in Figure 17 on page 47, this test pattern can be inserted in the place of any of the transmitted **or** received E1 signals. Since the test pattern contains an unframed signal, it is only intended for use in maintenance and troubleshooting.

Test Pattern Detector

The test pattern detector contains a self-synchronizing detector using the identical QRSS sequence as found in the test pattern generator. When the detector is out of sync, the device continually monitors the input data signal for matches to the expected data signal. When the device detects 32 matches in a row, it declares itself in sync and the error detector is enabled. If the device detects eight consecutive mismatches, the test pattern detector declares itself out of sync and starts searching again.

While in sync, the device counts the number of times the input data differs from the expected data in a 7-bit counter that holds its count when it reaches the maximum value of 128. This counter is reset when read by the microprocessor, and is not affected by the LATCH_CNT bit that resets all of the other counters within the device.

Typical Uses E1 Mode

Path Termination Multiplex

Using the device without internal loopbacks results in an SDH path terminating multiplex, as shown in Figure 19.

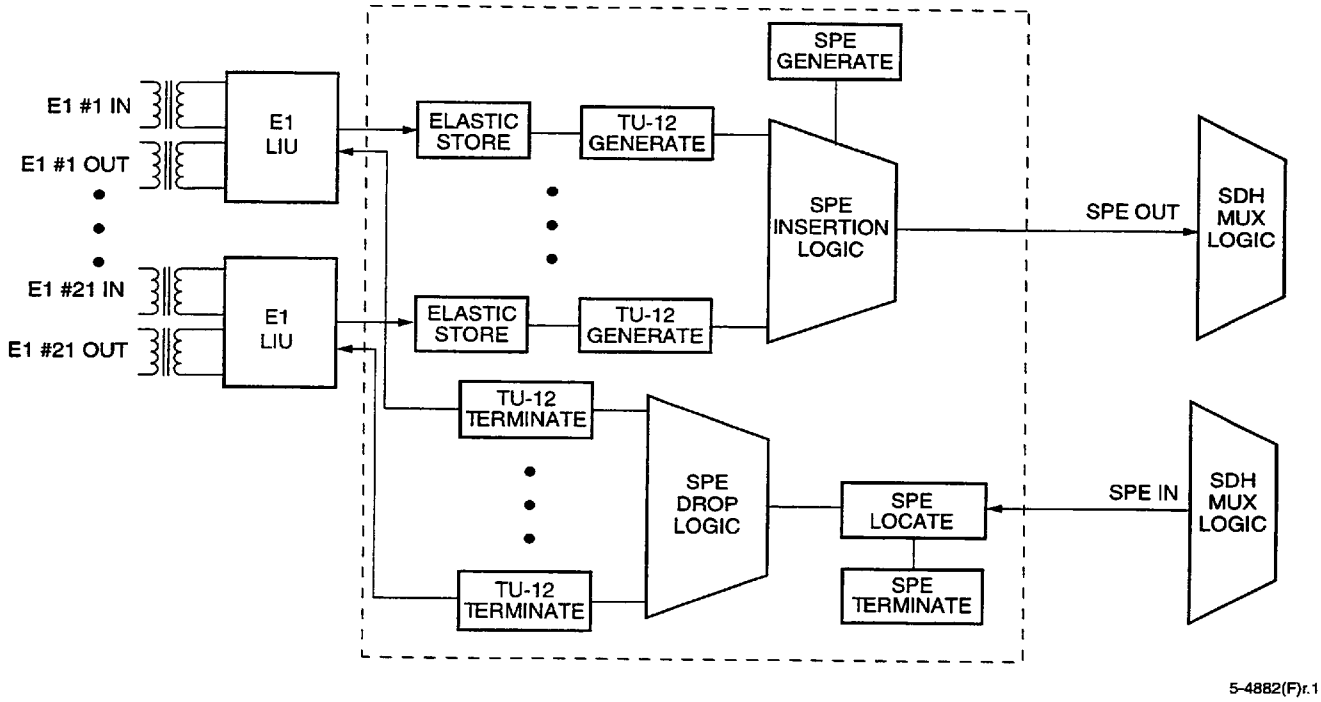

Figure 19. SDH Path Termination Multiplex Application

Typical Uses E1 Mode (continued)

Add/Drop Multiplex

Using the device with E1 internal loopbacks results in an SDH add/drop multiplex, as shown in Figure 20.

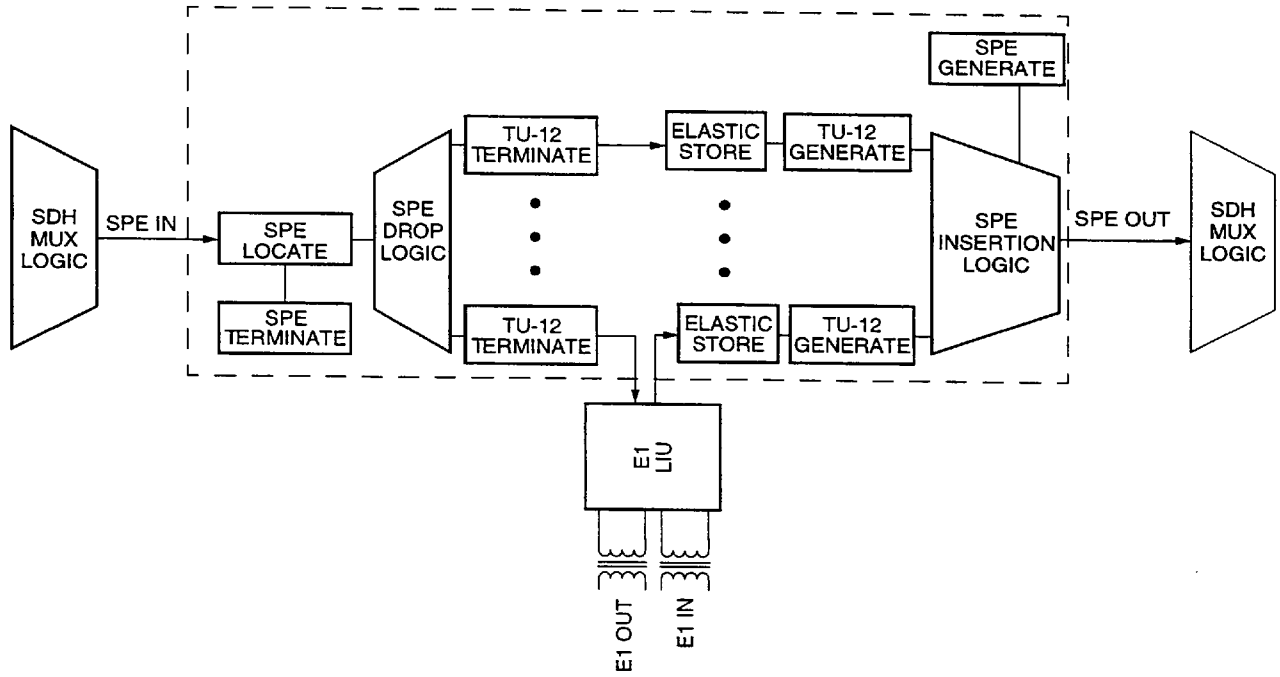

Figure 20. SDH Add/Drop Multiplex Application

Digital Cross Connect

Using the device with AU-3 internal loopbacks results in a digital cross connect, as shown in Figure 21.

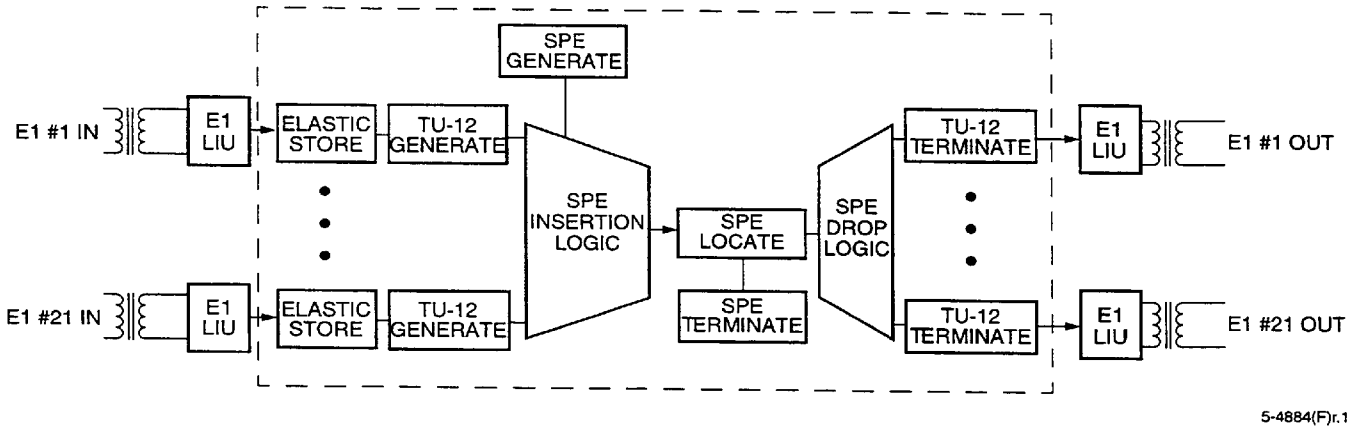

Figure 21. Digital Cross Connect Application

Typical Uses E1 Mode (continued)

Test Pattern Use — Complete System

The internal test pattern generator can be used in conjunction with E1 LIU devices that have built-in loopbacks (such as the Lucent T7690) to do a complete system test, as shown in Figure 22.

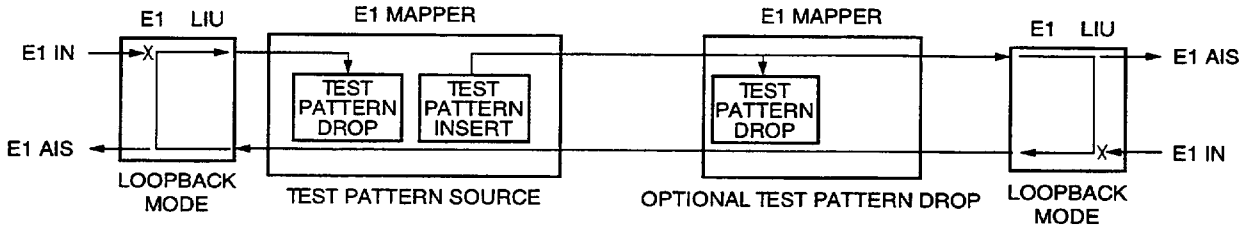

Figure 22. Test Pattern Usage for Complete System

Test Pattern Use — End to End

The internal test pattern generator can be used to test connectivity within a link by setting up a test pattern insert at one end and a drop at the other as shown in Figure 23.

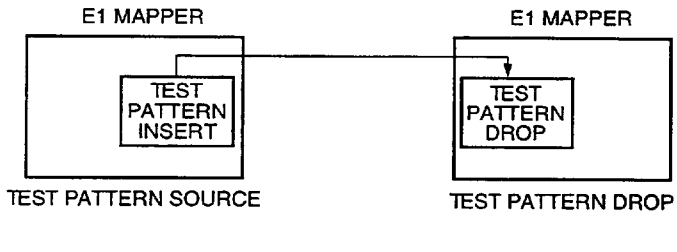

Figure 23. Test Pattern Usage for End-to-End Operation

Microprocessor Interface E1 Mode

Overview

The device is equipped with an asynchronous microprocessor interface that allows operation with most commercially available microprocessors. Inputs MPMUX and MPMODE are used to configure this interface into one of four possible modes. The MPMUX setting selects either a multiplexed 8-bit address/data bus (AD[7:0]) or a demultiplexed 8-bit address bus (A[7:0]) and an 8-bit data bus (AD[7:0]). The MPMODE setting selects the associated set of registers within the device.

The microprocessor interface can operate at speeds up to 16.384 MHz in interrupt-driven or polled mode without requiring any wait-states. To provide device flexibility, there are no default powerup or reset states. All read/write registers must be written by the microprocessor on system start-up to guarantee proper device functionality.

Microprocessor Configuration Modes

Table 26 highlights the four microprocessor modes controlled by the MPMUX and MPMODE inputs.

Table 26. Microprocessor Configuration Modes

Mode	MPMODE	MPMUX	Address/Data Bus	Generic Control, Data, and Output Pin Names
Mode 1	0	0	DEMUXed	$\overline{CS}$, $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$, A[7:0], AD[7:0], INT, $\overline{DTACK}$
Mode 2	0	1	MUXed	$\overline{CS}$, $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$, AD[7:0], INT, $\overline{DTACK}$
Mode 3	1	0	DEMUXed	$\overline{CS}$, ALE, $\overline{RD}$, $\overline{WR}$, A[7:0], AD[7:0], INT, RDY
Mode 4	1	1	MUXed	$\overline{CS}$, ALE, $\overline{RD}$, $\overline{WR}$, AD[7:0], INT, RDY

Microprocessor Interface E1 Mode (continued)

Microprocessor Interface Pinout Descriptions

The mode [1—4] specific pin definitions are given in Table 27. Note that the microprocessor interface uses the same set of pins in all modes.

Table 27. Mode [1—4] Microprocessor Pin Definitions

Configuration	Device Pin Name	Generic Pin Name	Pin Type	Assertion Sense	Function
Mode 1	$\overline{WR}\_\overline{DS}$	$\overline{DS}$	Input	Active-Low	Data Strobe
	$\overline{RD}\_R/\overline{W}$	$R/\overline{W}$	Input	—	Read/Write R/W = 1 for Read R/W = 0 for Write
	ALE_$\overline{AS}$	$\overline{AS}$	Input	—	Address Strobe
	$\overline{CS}$	$\overline{CS}$	Input	Active-Low	Chip Select
	INT	INT	Output	Active-High	Interrupt
	RDY_$\overline{DTACK}$	$\overline{DTACK}$	Output	Active-Low	Data Acknowledge
	AD[7:0)]	AD[7:0]	I/O	—	Data Bus
	A[7:0]	A[7:0]	Input	—	Address Bus
	MPCLK	MPCLK	Input	—	Microprocessor Clock
Mode 2	$\overline{WR}\_\overline{DS}$	$\overline{DS}$	Input	Active-Low	Data Strobe
	$\overline{RD}\_R/\overline{W}$	$R/\overline{W}$	Input	—	Read/Write R/W = 1 for Read R/W = 0 for Write
	ALE_$\overline{AS}$	$\overline{AS}$	Input	—	Address Strobe
	$\overline{CS}$	$\overline{CS}$	Input	Active-Low	Chip Select
	INT	INT	Output	Active-High	Interrupt
	RDY_$\overline{DTACK}$	$\overline{DTACK}$	Output	Active-Low	Data Acknowledge
	AD[7:0)]	AD[7:0]	I/O	—	Address/Data Bus
	MPCLK	MPCLK	Input	—	Microprocessor Clock

Microprocessor Interface E1 Mode (continued)

Microprocessor Interface Pinout Descriptions (continued)

Table 27. Mode [1—4] Microprocessor Pin Definitions (continued)

Configuration	Device Pin Name	Generic Pin Name	Pin Type	Assertion Sense	Function
Mode 3	$\overline{WR}$_$\overline{DS}$	$\overline{WR}$	Input	Active-Low	Write
	$\overline{RD}$_R/$\overline{W}$	$\overline{RD}$	Input	—	Read
	ALE_$\overline{AS}$	ALE	Input	—	Address Latch Enable
	$\overline{CS}$	$\overline{CS}$	Input	Active-Low	Chip Select
	INT	INT	Output	Active-High	Interrupt
	RDY_$\overline{DTACK}$	RDY	Output	Active-Low	Ready
	AD[7:0)]	AD[7:0]	I/O	—	Data Bus
	A[7:0]	A[7:0]	Input	—	Address Bus
	MPCLK	MPCLK	Input	—	Microprocessor Clock
Mode 4	$\overline{WR}$_$\overline{DS}$	$\overline{WR}$	Input	Active-Low	Write
	$\overline{RD}$_R/$\overline{W}$	$\overline{RD}$	Input	—	Read
	ALE_$\overline{AS}$	ALE	Input	—	Address Latch Enable
	$\overline{CS}$	$\overline{CS}$	Input	Active-Low	Chip Select
	INT	INT	Output	Active-High	Interrupt
	RDY_$\overline{DTACK}$	RDY	Output	Active-Low	Ready
	AD[7:0)]	AD[7:0]	I/O	—	Address/Data Bus
	MPCLK	MPCLK	Input	—	Microprocessor Clock

Microprocessor Interface E1 Mode (continued)

Microprocessor Interface Register Architecture

The register bank architecture of the microprocessor interface is shown in Table 28. All addresses referred to in this section are given in hexadecimal notation. Hexadecimal is the first column under Address.

Table 28. Device-Level Control, Alarm, and Mask Bits Register Set

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	00000000	TEST_CNT	B1ERRINS	B2ERRINS	B3ERRINS	LATCH_CNT	BLUECLKSEL	BIP2BLKCNT	RESET
01	00000001	FEBE_EN	0	TXPAISINS	0	TXFSYNC	AU3SCR	AU3DSCR	AU3LB
02	00000010	RXSERIAL	TXSERIAL	RXPARITY	TXPARITY	RXAU3EDGE	TXAU3EDGE	RXE1EDGE	TXE1EDGE
03	00000011	TRACEER	RXPARER	0	H4LOMF	AU3PAIS	AU3LOP	AU3LOF	AU3OOF
04	00000100	TRACEERMSK	RXPARERMSK	0	H4LOMFMSK	AU3PAISMSK	AU3LOPMSK	AU3LOFMSK	AU3OOFMSK
05	00000101	ESOFCOM	TUSIZECOM	TULOPCOM	TURDICOM	TUAISCOM	TULABCOM	E1LOCCOM	E1AISCOM
06	00000110	ESOFMSK	TUSIZEMSK	TULOPMSK	TURDIMSK	TUAISMSK	TULABMSK	E1LOCMSK	E1AISMSK
07	00000111	0	0	0	0	0	0	0	DS1_E1N
08	00001000	0	0	0	0	0	0	0	0
09	00001001	0	0	TPDROPSIDE	TPDROP4	TPDROP3	TPDROP2	TPDROP1	TPDROP0
0A	00001010	TPOOS	TPERR6	TPERR5	TPERR4	TPERR3	TPERR2	TPERR1	TPERR0
0B	00001011	F2-7	F2-6	F2-5	F2-4	F2-3	F2-2	F2-1	F2-0
0C	00001100	C2-7	C2-6	C2-5	C2-4	C2-3	C2-2	C2-1	C2-0
0D	00001101	G1-3	G1-2	G1-1	G1-0	0	K2-2	K2-1	K2-0
0E	00001110	C2NxDET3	C2NxDET2	C2NxDET1	C2NxDET0	F2NxDET3	F2NxDET2	F2NxDET1	F2NxDET0
0F	00001111	G1NxDET3	G1NxDET2	G1NxDET1	G1NxDET0	K2NxDET3	K2NxDET2	K2NxDET1	K2NxDET0
10	00010000	F2INS-7	F2INS-6	F2INS-5	F2INS-4	F2INS-3	F2INS-2	F2INS-1	F2INS-0
11	00010001	G1INS-3	G1INS-2	G1INS-1	G1INS-0	0	K2INS-2	K2INS-1	K2INS-0
12	00010010	0	0	0	0	0	0	0	0
13	00010011	0	0	0	0	0	0	0	0
14	00010100	0	0	0	0	0	0	0	0
15	00010101	0	0	0	0	0	0	0	0

Microprocessor Interface E1 Mode (continued)

Microprocessor Interface Register Architecture (continued)

Table 28. Device-Level Control, Alarm, and Mask Bits Register Set (continued)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
16	00010110	0	0	0	0	0	0	0	0
17	00010111	E1AIS1	E1LOC1	E11LB	E1_1INS4	E1_1INS3	E1_1INS2	E1_1INS1	E1_1INS0
18	00011000	E1AIS2	E1LOC2	E12LB	E1_2INS4	E1_2INS3	E1_2INS2	E1_2INS1	E1_2INS0
19	00011001	E1AIS3	E1LOC3	E13LB	E1_3INS4	E1_3INS3	E1_3INS2	E1_3INS1	E1_3INS0
1A	00011010	E1AIS4	E1LOC4	E14LB	E1_4INS4	E1_4INS3	E1_4INS2	E1_4INS1	E1_4INS0
1B	00011011	E1AIS5	E1LOC5	E15LB	E1_5INS4	E1_5INS3	E1_5INS2	E1_5INS1	E1_5INS0
1C	00011100	E1AIS6	E1LOC6	E16LB	E1_6INS4	E1_6INS3	E1_6INS2	E1_6INS1	E1_6INS0
1D	00011101	E1AIS7	E1LOC7	E17LB	E1_7INS4	E1_7INS3	E1_7INS2	E1_7INS1	E1_7INS0
1E	00011110	E1AIS8	E1LOC8	E18LB	E1_8INS4	E1_8INS3	E1_8INS2	E1_8INS1	E1_8INS0
1F	00011111	E1AIS9	E1LOC9	E19LB	E1_9INS4	E1_9INS3	E1_9INS2	E1_9INS1	E1_9INS0
20	00100000	E1AIS10	E1LOC10	E110LB	E1_10INS4	E1_10INS3	E1_10INS2	E1_10INS1	E1_10INS0
21	00100001	E1AIS11	E1LOC11	E111LB	E1_11INS4	E1_11INS3	E1_11INS2	E1_11INS1	E1_11INS0
22	00100010	E1AIS12	E1LOC12	E112LB	E1_12INS4	E1_12INS3	E1_12INS2	E1_12INS1	E1_12INS0
23	00100011	E1AIS13	E1LOC13	E113LB	E1_13INS4	E1_13INS3	E1_13INS2	E1_13INS1	E1_13INS0
24	00100100	E1AIS14	E1LOC14	E114LB	E1_14INS4	E1_14INS3	E1_14INS2	E1_14INS1	E1_14INS0
25	00100101	E1AIS15	E1LOC15	E115LB	E1_15INS4	E1_15INS3	E1_15INS2	E1_15INS1	E1_15INS0
26	00100110	E1AIS16	E1LOC16	E116LB	E1_16INS4	E1_16INS3	E1_16INS2	E1_16INS1	E1_16INS0
27	00100111	E1AIS17	E1LOC17	E117LB	E1_17INS4	E1_17INS3	E1_17INS2	E1_17INS1	E1_17INS0
28	00101000	E1AIS18	E1LOC18	E118LB	E1_18INS4	E1_18INS3	E1_18INS2	E1_18INS1	E1_18INS0
29	00101001	E1AIS19	E1LOC19	E119LB	E1_19INS4	E1_19INS3	E1_19INS2	E1_19INS1	E1_19INS0
2A	00101010	E1AIS20	E1LOC20	E120LB	E1_20INS4	E1_20INS3	E1_20INS2	E1_20INS1	E1_20INS0
2B	00101011	E1AIS21	E1LOC21	E121LB	E1_21INS4	E1_21INS3	E1_21INS2	E1_21INS1	E1_21INS0
2C	00101100	X	X	X	X	X	X	X	X
2D	00101101	X	X	X	X	X	X	X	X
2E	00101110	X	X	X	X	X	X	X	X
2F	00101111	X	X	X	X	X	X	X	X
30	00110000	X	X	X	X	X	X	X	X
31	00110001	X	X	X	X	X	X	X	X
32	00110010	X	X	X	X	X	X	X	X
33	00110011	0	RXESOF1	TXESOF1	TU_1DROP4	TU_1DROP3	TU_1DROP2	TU_1DROP1	TU_1DROP0
34	00110100	0	RXESOF2	TXESOF2	TU_2DROP4	TU_2DROP3	TU_2DROP2	TU_2DROP1	TU_2DROP0
35	00110101	0	RXESOF3	TXESOF3	TU_3DROP4	TU_3DROP3	TU_3DROP2	TU_3DROP1	TU_3DROP0
36	00110110	0	RXESOF4	TXESOF4	TU_4DROP4	TU_4DROP3	TU_4DROP2	TU_4DROP1	TU_4DROP0
37	00110111	0	RXESOF5	TXESOF5	TU_5DROP4	TU_5DROP3	TU_5DROP2	TU_5DROP1	TU_5DROP0
38	00111000	0	RXESOF6	TXESOF6	TU_6DROP4	TU_6DROP3	TU_6DROP2	TU_6DROP1	TU_6DROP0
39	00111001	0	RXESOF7	TXESOF7	TU_7DROP4	TU_7DROP3	TU_7DROP2	TU_7DROP1	TU_7DROP0
3A	00111010	0	RXESOF8	TXESOF8	TU_8DROP4	TU_8DROP3	TU_8DROP2	TU_8DROP1	TU_8DROP0
3B	00111011	0	RXESOF9	TXESOF9	TU_9DROP4	TU_9DROP3	TU_9DROP2	TU_9DROP1	TU_9DROP0
3C	00111100	0	RXESOF10	TXESOF10	TU_10DROP4	TU_10DROP3	TU_10DROP2	TU_10DROP1	TU_10DROP0
3D	00111101	0	RXESOF11	TXESOF11	TU_11DROP4	TU_11DROP3	TU_11DROP2	TU_11DROP1	TU_11DROP0
3E	00111110	0	RXESOF12	TXESOF12	TU_12DROP4	TU_12DROP3	TU_12DROP2	TU_12DROP1	TU_12DROP0
3F	00111111	0	RXESOF14	TXESOF13	TU_13DROP4	TU_13DROP3	TU_13DROP2	TU_13DROP1	TU_13DROP0

Microprocessor Interface E1 Mode (continued)

Microprocessor Interface Register Architecture (continued)

Table 28. Device-Level Control, Alarm, and Mask Bits Register Set (continued)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
40	01000000	0	RXESOF14	TXESOF14	TU_14DROP4	TU_14DROP3	TU_14DROP2	TU_14DROP1	TU_14DROP0
41	01000001	0	RXESOF15	TXESOF15	TU_15DROP4	TU_15DROP3	TU_15DROP2	TU_15DROP1	TU_15DROP0
42	01000010	0	RXESOF16	TXESOF16	TU_16DROP4	TU_16DROP3	TU_16DROP2	TU_16DROP1	TU_16DROP0
43	01000011	0	RXESOF17	TXESOF17	TU_17DROP4	TU_17DROP3	TU_17DROP2	TU_17DROP1	TU_17DROP0
44	01000100	0	RXESOF18	TXESOF18	TU_18DROP4	TU_18DROP3	TU_18DROP2	TU_18DROP1	TU_18DROP0
45	01000101	0	RXESOF19	TXESOF19	TU_19DROP4	TU_19DROP3	TU_19DROP2	TU_19DROP1	TU_19DROP0
46	01000110	0	RXESOF20	TXESOF20	TU_20DROP4	TU_20DROP3	TU_20DROP2	TU_20DROP1	TU_20DROP0
47	01000111	0	RXESOF21	TXESOF21	TU_21DROP4	TU_21DROP3	TU_21DROP2	TU_21DROP1	TU_21DROP0
48	01001000	0	X	X	X	X	X	X	X
49	01001001	0	X	X	X	X	X	X	X
4A	01001010	0	X	X	X	X	X	X	X
4B	01001011	0	X	X	X	X	X	X	X
4C	01001100	0	X	X	X	X	X	X	X
4D	01001101	0	X	X	X	X	X	X	X
4E	01001110	0	X	X	X	X	X	X	X
4F	01001111	BIP2ERINS1	TURD11_EN	VTRDI1_INS1	VTRDI1_INS0	TUAISINS1	TULAB2INS1	TULAB1INS1	TULAB0INS1
50	01010000	BIP2ERINS2	TURD12_EN	VTRDI2_INS1	VTRDI2_INS0	TUAISINS2	TULAB2INS2	TULAB1INS2	TULAB0INS2
51	01010001	BIP2ERINS3	TURD13_EN	VTRDI3_INS1	VTRDI3_INS0	TUAISINS3	TULAB2INS3	TULAB1INS3	TULAB0INS3
52	01010010	BIP2ERINS4	TURD14_EN	VTRDI4_INS1	VTRDI4_INS0	TUAISINS4	TULAB2INS4	TULAB1INS4	TULAB0INS4
53	01010011	BIP2ERINS5	TURD15_EN	VTRDI5_INS1	VTRDI5_INS0	TUAISINS5	TULAB2INS5	TULAB1INS5	TULAB0INS5
54	01010100	BIP2ERINS6	TURD16_EN	VTRDI6_INS1	VTRDI6_INS0	TUAISINS6	TULAB2INS6	TULAB1INS6	TULAB0INS6
55	01010101	BIP2ERINS7	TURD17_EN	VTRDI7_INS1	VTRDI7_INS0	TUAISINS7	TULAB2INS7	TULAB1INS7	TULAB0INS7
56	01010110	BIP2ERINS8	TURD18_EN	VTRDI8_INS1	VTRDI8_INS0	TUAISINS8	TULAB2INS8	TULAB1INS8	TULAB0INS8
57	01010111	BIP2ERINS9	TURD19_EN	VTRDI9_INS1	VTRDI9_INS0	TUAISINS9	TULAB2INS9	TULAB1INS9	TULAB0INS9
58	01011000	BIP2ERINS10	TURD110_EN	VTRDI10_INS1	VTRDI10_INS0	TUAISINS10	TULAB2INS10	TULAB1INS10	TULAB0INS10
59	01011001	BIP2ERINS11	TURD111_EN	VTRDI11_INS1	VTRDI11_INS0	TUAISINS11	TULAB2INS11	TULAB1INS11	TULAB0INS11
5A	01011010	BIP2ERINS12	TURD112_EN	VTRDI12_INS1	VTRDI12_INS0	TUAISINS12	TULAB2INS12	TULAB1INS12	TULAB0INS12
5B	01011011	BIP2ERINS13	TURD113_EN	VTRDI13_INS1	VTRDI13_INS0	TUAISINS13	TULAB2INS13	TULAB1INS13	TULAB0INS13
5C	01011100	BIP2ERINS14	TURD114_EN	VTRDI14_INS1	VTRDI14_INS0	TUAISINS14	TULAB2INS14	TULAB1INS14	TULAB0INS14
5D	01011101	BIP2ERINS15	TURD115_EN	VTRDI15_INS1	VTRDI15_INS0	TUAISINS15	TULAB2INS15	TULAB1INS15	TULAB0INS15
5E	01011110	BIP2ERINS16	TURD116_EN	VTRDI16_INS1	VTRDI16_INS0	TUAISINS16	TULAB2INS16	TULAB1INS16	TULAB0INS16
5F	01011111	BIP2ERINS17	TURD117_EN	VTRDI17_INS1	VTRDI17_INS0	TUAISINS17	TULAB2INS17	TULAB1INS17	TULAB0INS17
60	01100000	BIP2ERINS18	TURD118_EN	VTRDI18_INS1	VTRDI18_INS0	TUAISINS18	TULAB2INS18	TULAB1INS18	TULAB0INS18
61	01100001	BIP2ERINS19	TURD119_EN	VTRDI19_INS1	VTRDI19_INS0	TUAISINS19	TULAB2INS19	TULAB1INS19	TULAB0INS19
62	01100010	BIP2ERINS20	TURD120_EN	VTRDI20_INS1	VTRDI20_INS0	TUAISINS20	TULAB2INS20	TULAB1INS20	TULAB0INS20
63	01100011	BIP2ERINS21	TURD121_EN	VTRDI21_INS1	VTRDI21_INS0	TUAISINS21	TULAB2INS21	TULAB1INS21	TULAB0INS21
64	01100100	X	X	X	X	X	X	X	X
65	01100101	X	X	X	X	X	X	X	X
66	01100110	X	X	X	X	X	X	X	X
67	01100111	X	X	X	X	X	X	X	X
68	01101000	X	X	X	X	X	X	X	X
69	01101001	X	X	X	X	X	X	X	X

Microprocessor Interface E1 Mode (continued)

Microprocessor Interface Register Architecture (continued)

Table 28. Device-Level Control, Alarm, and Mask Bits Register Set (continued)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
6A	01101010	X	X	X	X	X	X	X	X
6B	01101011	TUSIZEER1	TULOP1	VTRDI11	VTRDI10	TUAIS1	TULAB21	TULAB11	TULAB01
6C	01101100	TUSIZEER2	TULOP2	VTRDI21	VTRDI20	TUAIS2	TULAB22	TULAB12	TULAB02
6D	01101101	TUSIZEER3	TULOP3	VTRDI31	VTRDI30	TUAIS3	TULAB23	TULAB13	TULAB03
6E	01101110	TUSIZEER4	TULOP4	VTRDI41	VTRDI40	TUAIS4	TULAB24	TULAB14	TULAB04
6F	01101111	TUSIZEER5	TULOP5	VTRDI51	VTRDI50	TUAIS5	TULAB25	TULAB15	TULAB05
70	01110000	TUSIZEER6	TULOP6	VTRDI61	VTRDI60	TUAIS6	TULAB26	TULAB16	TULAB06
71	01110001	TUSIZEER7	TULOP7	VTRDI71	VTRDI70	TUAIS7	TULAB27	TULAB17	TULAB07
72	01110010	TUSIZEER8	TULOP8	VTRDI81	VTRDI80	TUAIS8	TULAB28	TULAB18	TULAB08
73	01110011	TUSIZEER9	TULOP9	VTRDI91	VTRDI90	TUAIS9	TULAB29	TULAB19	TULAB09
74	01110100	TUSIZEER10	TULOP10	VTRDI101	VTRDI100	TUAIS10	TULAB210	TULAB110	TULAB010
75	01110101	TUSIZEER11	TULOP11	VTRDI111	VTRDI110	TUAIS11	TULAB211	TULAB111	TULAB011
76	01110110	TUSIZEER12	TULOP12	VTRDI121	VTRDI120	TUAIS12	TULAB212	TULAB112	TULAB012
77	01110111	TUSIZEER13	TULOP13	VTRDI131	VTRDI130	TUAIS13	TULAB213	TULAB113	TULAB013
78	01111000	TUSIZEER14	TULOP14	VTRDI141	VTRDI140	TUAIS14	TULAB214	TULAB114	TULAB014
79	01111001	TUSIZEER15	TULOP15	VTRDI151	VTRDI150	TUAIS15	TULAB215	TULAB115	TULAB015
7A	01111010	TUSIZEER16	TULOP16	VTRDI161	VTRDI160	TUAIS16	TULAB216	TULAB116	TULAB016
7B	01111011	TUSIZEER17	TULOP17	VTRDI171	VTRDI170	TUAIS17	TULAB217	TULAB117	TULAB017
7C	01111100	TUSIZEER18	TULOP18	VTRDI181	VTRDI180	TUAIS18	TULAB218	TULAB118	TULAB018
7D	01111101	TUSIZEER19	TULOP19	VTRDI191	VTRDI190	TUAIS19	TULAB219	TULAB119	TULAB019
7E	01111110	TUSIZEER20	TULOP20	VTRDI201	VTRDI200	TUAIS20	TULAB220	TULAB120	TULAB020
7F	01111111	TUSIZEER21	TULOP21	VTRDI211	VTRDI210	TUAIS21	TULAB221	TULAB121	TULAB021
80	10000000	X	X	X	X	X	X	X	X
81	10000001	X	X	X	X	X	X	X	X
82	10000010	X	X	X	X	X	X	X	X
83	10001000	X	X	X	X	X	X	X	X
84	10000100	X	X	X	X	X	X	X	X
85	10000101	X	X	X	X	X	X	X	X
86	10000110	X	X	X	X	X	X	X	X
87	10000111	0	0	0	0	0	0	0	0
88	10001000	0	0	0	0	0	0	0	0
89	10001001	0	0	0	0	0	0	0	0
8A	10001010	0	0	0	0	0	0	0	0
8B	10001011	0	0	0	0	0	0	0	0
8C	10001100	0	0	0	0	0	0	0	0
8D	10001101	0	0	0	0	0	0	0	0
8E	10001110	0	0	0	0	0	0	0	0
8F	10001111	0	0	0	0	0	0	0	0
90	10010000	0	0	0	0	0	0	0	0
91	10010001	0	0	0	0	0	0	0	0
92	10010010	0	0	0	0	0	0	0	0
93	10010011	0	0	0	0	0	0	0	0
94	10010100	0	0	0	0	0	0	0	0
95	10010101	0	0	0	0	0	0	0	0

Microprocessor Interface E1 Mode (continued)

Microprocessor Interface Register Architecture (continued)

Table 28. Device-Level Control, Alarm, and Mask Bits Register Set (continued)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
96	10010110	0	0	0	0	0	0	0	0
97	10010111	0	0	0	0	0	0	0	0
98	10011000	0	0	0	0	0	0	0	0
99	10011001	0	0	0	0	0	0	0	0
9A	10011010	0	0	0	0	0	0	0	0
9B	10011011	0	0	0	0	0	0	0	0
9C	10011100	0	0	0	0	0	0	0	0
9D	10011101	0	0	0	0	0	0	0	0
9E	10011110	0	0	0	0	0	0	0	0
9F	10011111	0	0	0	0	0	0	0	0
A0	10100000	0	0	0	0	0	0	0	0
A1	10100001	0	0	0	0	0	0	0	0
A2	10100010	0	0	0	0	0	0	0	0
A3	10100011	0	0	0	0	0	0	0	0
A4	10100100	0	0	0	0	0	0	0	0
A5	10100101	0	0	0	0	0	0	0	0
A6	10100110	0	0	0	0	0	0	0	0
A7	10100111	0	0	0	0	0	0	0	0
A8	10101000	0	0	0	0	0	0	0	0
A9	10101001	0	0	0	0	0	0	0	0
AA	10101010	0	0	0	0	0	0	0	0
AB	10101011	0	0	0	0	0	0	0	0
AC	10101100	0	0	0	0	0	0	0	0
AD	10101101	0	0	0	0	0	0	0	0
AE	10101110	0	0	0	0	0	0	0	0
AF	10101111	0	0	0	0	0	0	0	0
B0	10110000	0	0	0	0	0	0	0	0
B1	10110001	0	0	0	0	0	0	0	0
B2	10110010	0	0	0	0	0	0	0	0
B3	10110011	0	0	0	0	0	0	0	0
B4	10110100	0	0	0	0	0	0	0	0
B5	10110101	0	0	0	0	0	0	0	0
B6	10110110	0	0	0	0	0	0	0	0
B7	10110111	0	0	0	0	0	0	0	0
B8	10111000	0	0	0	0	0	0	0	0
B9	10111001	0	0	0	0	0	0	0	0
BA	10111010	0	0	0	0	0	0	0	0
BB	10111011	0	0	0	0	0	0	0	0
BC	10111100	0	0	0	0	0	0	0	0
BD	10111101	0	0	0	0	0	0	0	0
BE	10111110	0	0	0	0	0	0	0	0

Microprocessor Interface E1 Mode (continued)

Microprocessor Interface Register Architecture (continued)

Table 28. Device-Level Control, Alarm, and Mask Bits Register Set (continued)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BF	10111111	0	0	0		TJ1BYTE	RJ1BYTE	FEBE_CNTS	BIP_CNTS
When BIP_CNTS = 1									
C0	11000000	B1BIPCNT15	B1BIPCNT14	B1BIPCNT13	B1BIPCNT12	B1BIPCNT11	B1BIPCNT10	B1BIPCNT9	B1BIPCNT8
C1	11000001	B1BIPCNT7	B1BIPCNT6	B1BIPCNT5	B1BIPCNT4	B1BIPCNT3	B1BIPCNT2	B1BIPCNT1	B1BIPCNT0
C2	11000010	B2BIPCNT15	B2BIPCNT14	B2BIPCNT13	B2BIPCNT12	B2BIPCNT11	B2BIPCNT10	B2BIPCNT9	B2BIPCNT8
C3	11000011	B2BIPCNT7	B2BIPCNT6	B2BIPCNT5	B2BIPCNT4	B2BIPCNT3	B2BIPCNT2	B2BIPCNT1	B2BIPCNT0
C4	11000100	B3BIPCNT15	B3BIPCNT14	B3BIPCNT13	B3BIPCNT12	B3BIPCNT11	B3BIPCNT10	B3BIPCNT9	B3BIPCNT8
C5	11000101	B3BIPCNT7	B3BIPCNT6	B3BIPCNT5	B3BIPCNT4	B3BIPCNT3	B3BIPCNT2	B3BIPCNT1	B3BIPCNT0
C6	11000110	TU1PTR+3	TU1PTR+2	TU1PTR+1	TU1PTR+0	BIP2CNT111	BIP2CNT101	BIP2CNT91	BIP2CNT81
C7	11000111	BIP2CNT71	BIP2CNT61	BIP2CNT51	BIP2CNT41	BIP2CNT31	BIP2CNT21	BIP2CNT11	BIP2CNT01
C8	11001000	TU2PTR+3	TU2PTR+2	TU2PTR+1	TU2PTR+0	BIP2CNT112	BIP2CNT102	BIP2CNT92	BIP2CNT82
C9	11001001	BIP2CNT72	BIP2CNT62	BIP2CNT52	BIP2CNT42	BIP2CNT32	BIP2CNT22	BIP2CNT12	BIP2CNT02
CA	11001010	TU3PTR+3	TU3PTR+2	TU3PTR+1	TU3PTR+0	BIP2CNT113	BIP2CNT103	BIP2CNT93	BIP2CNT83
CB	11001011	BIP2CNT73	BIP2CNT63	BIP2CNT53	BIP2CNT43	BIP2CNT33	BIP2CNT23	BIP2CNT13	BIP2CNT03
CC	11001100	TU4PTR+3	TU4PTR+2	TU4PTR+1	TU4PTR+0	BIP2CNT114	BIP2CNT104	BIP2CNT94	BIP2CNT84
CD	11001101	BIP2CNT74	BIP2CNT64	BIP2CNT54	BIP2CNT44	BIP2CNT34	BIP2CNT24	BIP2CNT14	BIP2CNT04
CE	11001110	TU5PTR+3	TU5PTR+2	TU5PTR+1	TU5PTR+0	BIP2CNT115	BIP2CNT105	BIP2CNT95	BIP2CNT85
CF	11001111	BIP2CNT75	BIP2CNT65	BIP2CNT55	BIP2CNT45	BIP2CNT35	BIP2CNT25	BIP2CNT15	BIP2CNT05
D0	11010000	TU6PTR+3	TU6PTR+2	TU6PTR+1	TU6PTR+0	BIP2CNT116	BIP2CNT106	BIP2CNT96	BIP2CNT86
D1	11010001	BIP2CNT76	BIP2CNT66	BIP2CNT56	BIP2CNT46	BIP2CNT36	BIP2CNT26	BIP2CNT16	BIP2CNT06
D2	11010010	TU7PTR+3	TU7PTR+2	TU7PTR+1	TU7PTR+0	BIP2CNT117	BIP2CNT107	BIP2CNT97	BIP2CNT87
D3	11010011	BIP2CNT77	BIP2CNT67	BIP2CNT57	BIP2CNT47	BIP2CNT37	BIP2CNT27	BIP2CNT17	BIP2CNT07
D4	11010100	TU8PTR+3	TU8PTR+2	TU8PTR+1	TU8PTR+0	BIP2CNT118	BIP2CNT108	BIP2CNT98	BIP2CNT88
D5	11010101	BIP2CNT78	BIP2CNT68	BIP2CNT58	BIP2CNT48	BIP2CNT38	BIP2CNT28	BIP2CNT18	BIP2CNT08
D6	11010110	TU9PTR+3	TU9PTR+2	TU9PTR+1	TU9PTR+0	BIP2CNT119	BIP2CNT109	BIP2CNT99	BIP2CNT89
D7	11010111	BIP2CNT79	BIP2CNT69	BIP2CNT59	BIP2CNT49	BIP2CNT39	BIP2CNT29	BIP2CNT19	BIP2CNT09
D8	11011000	TU10PTR+3	TU10PTR+2	TU10PTR+1	TU10PTR+0	BIP2CNT1110	BIP2CNT1010	BIP2CNT910	BIP2CNT810
D9	11011001	BIP2CNT710	BIP2CNT610	BIP2CNT510	BIP2CNT410	BIP2CNT310	BIP2CNT210	BIP2CNT101	BIP2CNT010
DA	11011010	TU11PTR+3	TU11PTR+2	TU11PTR+1	TU11PTR+0	BIP2CNT1111	BIP2CNT1011	BIP2CNT911	BIP2CNT811
DB	11011011	BIP2CNT711	BIP2CNT611	BIP2CNT511	BIP2CNT411	BIP2CNT311	BIP2CNT211	BIP2CNT111	BIP2CNT011
DC	11011100	TU12PTR+3	TU12PTR+2	TU12PTR+1	TU12PTR+0	BIP2CNT1112	BIP2CNT1012	BIP2CNT912	BIP2CNT812
DD	11011101	BIP2CNT712	BIP2CNT612	BIP2CNT512	BIP2CNT412	BIP2CNT312	BIP2CNT212	BIP2CNT112	BIP2CNT012
DE	11011110	TU13PTR+3	TU13PTR+2	TU13PTR+1	TU13PTR+0	BIP2CNT1113	BIP2CNT1013	BIP2CNT913	BIP2CNT813
DF	11011111	BIP2CNT713	BIP2CNT613	BIP2CNT513	BIP2CNT413	BIP2CNT313	BIP2CNT213	BIP2CNT113	BIP2CNT013
E0	11100000	TU14PTR+3	TU14PTR+2	TU14PTR+1	TU14PTR+0	BIP2CNT1114	BIP2CNT1014	BIP2CNT914	BIP2CNT814
E1	11100001	BIP2CNT714	BIP2CNT614	BIP2CNT514	BIP2CNT414	BIP2CNT314	BIP2CNT214	BIP2CNT114	BIP2CNT014
E2	11100010	TU15PTR+3	TU15PTR+2	TU15PTR+1	TU15PTR+0	BIP2CNT1115	BIP2CNT1015	BIP2CNT915	BIP2CNT815
E3	11100011	BIP2CNT715	BIP2CNT615	BIP2CNT515	BIP2CNT415	BIP2CNT315	BIP2CNT215	BIP2CNT115	BIP2CNT015
E4	11100100	TU16PTR+3	TU16PTR+2	TU16PTR+1	TU16PTR+0	BIP2CNT1116	BIP2CNT1016	BIP2CNT916	BIP2CNT816

Microprocessor Interface E1 Mode (continued)

Microprocessor Interface Register Architecture (continued)

Table 28. Device-Level Control, Alarm, and Mask Bits Register Set (continued)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
E5	11100101	BIP2CNT716	BIP2CNT616	BIP2CNT516	BIP2CNT416	BIP2CNT316	BIP2CNT216	BIP2CNT116	BIP2CNT016
E6	11100110	TU17PTR+3	TU17PTR+2	TU17PTR+1	TU17PTR+0	BIP2CNT1117	BIP2CNT1017	BIP2CNT917	BIP2CNT817
E7	11100111	BIP2CNT717	BIP2CNT617	BIP2CNT517	BIP2CNT417	BIP2CNT317	BIP2CNT217	BIP2CNT117	BIP2CNT017
E8	11101000	TU18PTR+3	TU18PTR+2	TU18PTR+1	TU188PTR+0	BIP2CNT1118	BIP2CNT1018	BIP2CNT918	BIP2CNT818
E9	11101001	BIP2CNT718	BIP2CNT618	BIP2CNT518	BIP2CNT418	BIP2CNT318	BIP2CNT218	BIP2CNT118	BIP2CNT018
EA	11101010	TU19PTR+3	TU19PTR+2	TU19PTR+1	TU19PTR+0	BIP2CNT1119	BIP2CNT1019	BIP2CNT919	BIP2CNT819
EB	11101011	BIP2CNT719	BIP2CNT619	BIP2CNT519	BIP2CNT419	BIP2CNT319	BIP2CNT219	BIP2CNT119	BIP2CNT019
EC	11101100	TU20PTR+3	TU20PTR+2	TU20PTR+1	TU20PTR+0	BIP2CNT1120	BIP2CNT1020	BIP2CNT920	BIP2CNT820
ED	11101101	BIP2CNT720	BIP2CNT620	BIP2CNT520	BIP2CNT420	BIP2CNT320	BIP2CNT220	BIP2CNT120	BIP2CNT020
EE	11101110	TU21PTR+3	TU21PTR+2	TU21PTR+1	TU21PTR+0	BIP2CNT1121	BIP2CNT1021	BIP2CNT921	BIP2CNT821
EF	11101111	BIP2CNT721	BIP2CNT621	BIP2CNT521	BIP2CNT421	BIP2CNT321	BIP2CNT221	BIP2CNT121	BIP2CNT021
F0	11110000	X	X	X	X	X	X	X	X
F1	11110001	X	X	X	X	X	X	X	X
F2	11110010	X	X	X	X	X	X	X	X
F3	11110011	X	X	X	X	X	X	X	X
F4	11110100	X	X	X	X	X	X	X	X
F5	11110101	X	X	X	X	X	X	X	X
F6	11110110	X	X	X	X	X	X	X	X
F7	11110111	X	X	X	X	X	X	X	X
F8	11111000	X	X	X	X	X	X	X	X
F9	11111001	X	X	X	X	X	X	X	X
FA	11111010	X	X	X	X	X	X	X	X
FB	11111011	X	X	X	X	X	X	X	X
FC	11111100	X	X	X	X	X	X	X	X
FD	11111101	X	X	X	X	X	X	X	X
FE	11111110	SPTR+7	SPTR+6	SPTR+5	SPTR+4	SPTR+3	SPTR+2	SPTR+1	SPTR+0
FF	11111111	SPTR–7	SPTR–6	SPTR–5	SPTR–4	SPTR–3	SPTR–2	SPTR–1	SPTR–0
When FEBE_CNTS = 1									
C0	11000000	0	0	0	0	0	0	0	0
C1	11000001	0	0	0	0	0	0	0	0
C2	11000010	B2FEBE15	B2FEBE14	B2FEBE13	B2FEBE12	B2FEBE11	B2FEBE10	B2FEBE9	B2FEBE8
C3	11000011	B2FEBE7	B2FEBE6	B2FEBE5	B2FEBE4	B2FEBE3	B2FEBE2	B2FEBE1	B2FEBE0
C4	11000100	B3FEBE15	B3FEBE14	B3FEBE13	B3FEBE12	B3FEBE11	B3FEBE10	B3FEBE9	B3FEBE8
C5	11000101	B3FEBE7	B3FEBE6	B3FEBE5	B3FEBE4	B3FEBE3	B3FEBE2	B3FEBE1	B3FEBE0
C6	11000110	TU1PTR-3	TU1PTR-2	TU1PTR-1	TU1PTR-0	0	TUFEBE101	TUFEBE91	TUFEBE81
C7	11000111	TUFEBE71	TUFEBE61	TUFEBE51	TUFEBE41	TUFEBE31	TUFEBE21	TUFEBE11	TUFEBE01
C8	11001000	TU2PTR-3	TU2PTR-2	TU2PTR-1	TU2PTR-0	0	TUFEBE102	TUFEBE92	TUFEBE82
C9	11001001	TUFEBE72	TUFEBE62	TUFEBE52	TUFEBE42	TUFEBE32	TUFEBE22	TUFEBE12	TUFEBE02
CA	11001010	TU3PTR-3	TU3PTR-2	TU3PTR-1	TU3PTR-0	0	TUFEBE103	TUFEBE93	TUFEBE83
CB	11001011	TUFEBE73	TUFEBE63	TUFEBE53	TUFEBE43	TUFEBE33	TUFEBE23	TUFEBE13	TUFEBE03
CC	11001100	TU4PTR-3	TU4PTR-2	TU4PTR-1	TU4PTR-0	0	TUFEBE104	TUFEBE94	TUFEBE84
CD	11001101	TUFEBE74	TUFEBE64	TUFEBE54	TUFEBE44	TUFEBE34	TUFEBE24	TUFEBE14	TUFEBE04
CE	11001110	TU5PTR-3	TU5PTR-2	TU5PTR-1	TU5PTR-0	0	TUFEBE105	TUFEBE95	TUFEBE85
CF	11001111	TUFEBE75	TUFEBE65	TUFEBE55	TUFEBE45	TUFEBE35	TUFEBE25	TUFEBE15	TUFEBE05
D0	11010000	TU6PTR-3	TU6PTR-2	TU6PTR-1	TU6PTR-0	0	TUFEBE106	TUFEBE96	TUFEBE86

Microprocessor Interface E1 Mode (continued)

Microprocessor Interface Register Architecture (continued)

Table 28. Device-Level Control, Alarm, and Mask Bits Register Set (continued)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D1	11010001	TUFEBE76	TUFEBE66	TUFEBE56	TUFEBE46	TUFEBE36	TUFEBE26	TUFEBE16	TUFEBE06
D2	11010010	TU7PTR-3	TU7PTR-2	TU7PTR-1	TU7PTR-0	0	TUFEBE107	TUFEBE97	TUFEBE87
D3	11010011	TUFEBE77	TUFEBE67	TUFEBE57	TUFEBE47	TUFEBE37	TUFEBE27	TUFEBE17	TUFEBE07
D4	11010100	TU8PTR-3	TU8PTR-2	TU8PTR-1	TU8PTR-0	0	TUFEBE108	TUFEBE98	TUFEBE88
D5	11010101	TUFEBE78	TUFEBE68	TUFEBE58	TUFEBE48	TUFEBE38	TUFEBE28	TUFEBE18	TUFEBE08
D6	11010110	TU9PTR-3	TU9PTR-2	TU9PTR-1	TU9PTR-0	0	TUFEBE109	TUFEBE99	TUFEBE89
D7	11010111	TUFEBE79	TUFEBE69	TUFEBE59	TUFEBE49	TUFEBE39	TUFEBE29	TUFEBE19	TUFEBE09
D8	11011000	TU10PTR-3	TU10PTR-2	TU10PTR-1	TU10PTR-0	0	TUFEBE1010	TUFEBE910	TUFEBE810
D9	11011001	TUFEBE710	TUFEBE610	TUFEBE510	TUFEBE410	TUFEBE310	TUFEBE210	TUFEBE101	TUFEBE010
DA	11011010	TU11PTR-3	TU11PTR-2	TU11PTR-1	TU11PTR-0	0	TUFEBE1011	TUFEBE911	TUFEBE811
DB	11011011	TUFEBE711	TUFEBE611	TUFEBE511	TUFEBE411	TUFEBE311	TUFEBE211	TUFEBE111	TUFEBE011
DC	11011100	TU12PTR-3	TU12PTR-2	TU12PTR-1	TU12PTR-0	0	TUFEBE1012	TUFEBE912	TUFEBE812
DD	11011101	TUFEBE712	TUFEBE612	TUFEBE512	TUFEBE412	TUFEBE312	TUFEBE212	TUFEBE112	TUFEBE012
DE	11011110	TU13PTR-3	TU13PTR-2	TU13PTR-1	TU13PTR-0	0	TUFEBE1013	TUFEBE913	TUFEBE813
DF	11011111	TUFEBE713	TUFEBE613	TUFEBE513	TUFEBE413	TUFEBE313	TUFEBE213	TUFEBE113	TUFEBE013
E0	11100000	TU14PTR-3	TU14PTR-2	TU14PTR-1	TU14PTR-0	0	TUFEBE1014	TUFEBE914	TUFEBE814
E1	11100001	TUFEBE714	TUFEBE614	TUFEBE514	TUFEBE414	TUFEBE314	TUFEBE214	TUFEBE114	TUFEBE014
E2	11100010	TU15PTR-3	TU15PTR-2	TU15PTR-1	TU15PTR-0	0	TUFEBE1015	TUFEBE915	TUFEBE815
E3	11100011	TUFEBE715	TUFEBE615	TUFEBE515	TUFEBE415	TUFEBE315	TUFEBE215	TUFEBE115	TUFEBE015
E4	11100100	TU16PTR-3	TU16PTR-2	TU16PTR-1	TU16PTR-0	0	TUFEBE1016	TUFEBE916	TUFEBE816
E5	11100101	TUFEBE716	TUFEBE616	TUFEBE516	TUFEBE416	TUFEBE316	TUFEBE216	TUFEBE116	TUFEBE016
E6	11100110	TU17PTR-3	TU17PTR-2	TU17PTR-1	TU17PTR-0	0	TUFEBE1017	TUFEBE917	TUFEBE817
E7	11100111	TUFEBE717	TUFEBE617	TUFEBE517	TUFEBE417	TUFEBE317	TUFEBE217	TUFEBE117	TUFEBE017
E8	11101000	TU18PTR-3	TU18PTR-2	TU18PTR-1	TU188PTR-0	0	TUFEBE1018	TUFEBE918	TUFEBE818
E9	11101001	TUFEBE718	TUFEBE618	TUFEBE518	TUFEBE418	TUFEBE318	TUFEBE218	TUFEBE118	TUFEBE018
EA	11101010	TU19PTR-3	TU19PTR-2	TU19PTR-1	TU19PTR-0	0	TUFEBE1019	TUFEBE919	TUFEBE819
EB	11101011	TUFEBE719	TUFEBE619	TUFEBE519	TUFEBE419	TUFEBE319	TUFEBE219	TUFEBE119	TUFEBE019
EC	11101100	TU20PTR-3	TU20PTR-2	TU20PTR-1	TU20PTR-0	0	TUFEBE1020	TUFEBE920	TUFEBE820
ED	11101101	TUFEBE720	TUFEBE620	TUFEBE520	TUFEBE420	TUFEBE320	TUFEBE220	TUFEBE120	TUFEBE020
EE	11101110	TU21PTR-3	TU21PTR-2	TU21PTR-1	TU21PTR-0	0	TUFEBE1021	TUFEBE921	TUFEBE821
EF	11101111	TUFEBE721	TUFEBE621	TUFEBE521	TUFEBE421	TUFEBE321	TUFEBE221	TUFEBE121	TUFEBE021
F0	11110000	X	X	X	X	X	X	X	X
F1	11110001	X	X	X	X	X	X	X	X
F2	11110010	X	X	X	X	X	X	X	X
F3	11110011	X	X	X	X	X	X	X	X
F4	11110100	X	X	X	X	X	X	X	X
F5	11110101	X	X	X	X	X	X	X	X
F6	11110110	X	X	X	X	X	X	X	X
F7	11110111	X	X	X	X	X	X	X	X
F8	11111000	X	X	X	X	X	X	X	X
F9	11111001	X	X	X	X	X	X	X	X
FA	11111010	X	X	X	X	X	X	X	X
FB	11111011	X	X	X	X	X	X	X	X
FC	11111100	X	X	X	X	X	X	X	X

Microprocessor Interface E1 Mode (continued)

Microprocessor Interface Register Architecture (continued)

Table 28. Device-Level Control, Alarm, and Mask Bits Register Set (continued)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FD	11111101	X	X	X	X	X	X	X	X
FE	11111110	0	0	0	0	0	0	0	0
FF	11111111	0	0	0	0	0	0	0	0
When RJ1BYTE = 1									
C0	11000000	RJ1BYTE647	RJ1BYTE646	RJ1BYTE645	RJ1BYTE644	RJ1BYTE643	RJ1BYTE642	RJ1BYTE641	RJ1BYTE640
C1	11000001	RJ1BYTE637	RJ1BYTE636	RJ1BYTE635	RJ1BYTE634	RJ1BYTE633	RJ1BYTE632	RJ1BYTE631	RJ1BYTE630
C2	11000010	RJ1BYTE627	RJ1BYTE626	RJ1BYTE625	RJ1BYTE624	RJ1BYTE623	RJ1BYTE622	RJ1BYTE621	RJ1BYTE620
C3	11000011	RJ1BYTE617	RJ1BYTE616	RJ1BYTE615	RJ1BYTE614	RJ1BYTE613	RJ1BYTE612	RJ1BYTE611	RJ1BYTE610
C4	11000100	RJ1BYTE607	RJ1BYTE606	RJ1BYTE605	RJ1BYTE604	RJ1BYTE603	RJ1BYTE602	RJ1BYTE601	RJ1BYTE600
C5	11000101	RJ1BYTE597	RJ1BYTE596	RJ1BYTE595	RJ1BYTE594	RJ1BYTE593	RJ1BYTE592	RJ1BYTE591	RJ1BYTE590
C6	11000110	RJ1BYTE587	RJ1BYTE586	RJ1BYTE585	RJ1BYTE584	RJ1BYTE583	RJ1BYTE582	RJ1BYTE581	RJ1BYTE580
C7	11000111	RJ1BYTE577	RJ1BYTE576	RJ1BYTE575	RJ1BYTE574	RJ1BYTE573	RJ1BYTE572	RJ1BYTE571	RJ1BYTE570
C8	11001000	RJ1BYTE567	RJ1BYTE566	RJ1BYTE565	RJ1BYTE564	RJ1BYTE563	RJ1BYTE562	RJ1BYTE561	RJ1BYTE560
C9	11001001	RJ1BYTE557	RJ1BYTE556	RJ1BYTE555	RJ1BYTE554	RJ1BYTE553	RJ1BYTE552	RJ1BYTE551	RJ1BYTE550
CA	11001010	RJ1BYTE547	RJ1BYTE546	RJ1BYTE545	RJ1BYTE544	RJ1BYTE543	RJ1BYTE542	RJ1BYTE541	RJ1BYTE540
CB	11001011	RJ1BYTE537	RJ1BYTE536	RJ1BYTE535	RJ1BYTE534	RJ1BYTE533	RJ1BYTE532	RJ1BYTE531	RJ1BYTE530
CC	11001100	RJ1BYTE527	RJ1BYTE526	RJ1BYTE525	RJ1BYTE524	RJ1BYTE523	RJ1BYTE522	RJ1BYTE521	RJ1BYTE520
CD	11001101	RJ1BYTE517	RJ1BYTE516	RJ1BYTE515	RJ1BYTE514	RJ1BYTE513	RJ1BYTE512	RJ1BYTE511	RJ1BYTE510
CE	11001110	RJ1BYTE507	RJ1BYTE506	RJ1BYTE505	RJ1BYTE504	RJ1BYTE503	RJ1BYTE502	RJ1BYTE501	RJ1BYTE500
CF	11001111	RJ1BYTE497	RJ1BYTE496	RJ1BYTE495	RJ1BYTE494	RJ1BYTE493	RJ1BYTE492	RJ1BYTE491	RJ1BYTE490
D0	11010000	RJ1BYTE487	RJ1BYTE486	RJ1BYTE485	RJ1BYTE484	RJ1BYTE483	RJ1BYTE482	RJ1BYTE481	RJ1BYTE480
D1	11010001	RJ1BYTE477	RJ1BYTE476	RJ1BYTE475	RJ1BYTE474	RJ1BYTE473	RJ1BYTE472	RJ1BYTE471	RJ1BYTE470
D2	11010010	RJ1BYTE467	RJ1BYTE466	RJ1BYTE465	RJ1BYTE464	RJ1BYTE463	RJ1BYTE462	RJ1BYTE461	RJ1BYTE460
D3	11010011	RJ1BYTE457	RJ1BYTE456	RJ1BYTE455	RJ1BYTE454	RJ1BYTE453	RJ1BYTE452	RJ1BYTE451	RJ1BYTE450
D4	11010100	RJ1BYTE447	RJ1BYTE446	RJ1BYTE445	RJ1BYTE444	RJ1BYTE443	RJ1BYTE442	RJ1BYTE441	RJ1BYTE440
D5	11010101	RJ1BYTE437	RJ1BYTE436	RJ1BYTE435	RJ1BYTE434	RJ1BYTE433	RJ1BYTE432	RJ1BYTE431	RJ1BYTE430
D6	11010110	RJ1BYTE427	RJ1BYTE426	RJ1BYTE425	RJ1BYTE424	RJ1BYTE423	RJ1BYTE422	RJ1BYTE421	RJ1BYTE420
D7	11010111	RJ1BYTE417	RJ1BYTE416	RJ1BYTE415	RJ1BYTE414	RJ1BYTE413	RJ1BYTE412	RJ1BYTE411	RJ1BYTE410
D8	11011000	RJ1BYTE407	RJ1BYTE406	RJ1BYTE405	RJ1BYTE404	RJ1BYTE403	RJ1BYTE402	RJ1BYTE401	RJ1BYTE400
D9	11011001	RJ1BYTE397	RJ1BYTE396	RJ1BYTE395	RJ1BYTE394	RJ1BYTE393	RJ1BYTE392	RJ1BYTE391	RJ1BYTE390
DA	11011010	RJ1BYTE387	RJ1BYTE386	RJ1BYTE385	RJ1BYTE384	RJ1BYTE383	RJ1BYTE382	RJ1BYTE381	RJ1BYTE380
DB	11011011	RJ1BYTE377	RJ1BYTE376	RJ1BYTE375	RJ1BYTE374	RJ1BYTE373	RJ1BYTE372	RJ1BYTE371	RJ1BYTE370
DC	11011100	RJ1BYTE367	RJ1BYTE366	RJ1BYTE365	RJ1BYTE364	RJ1BYTE363	RJ1BYTE362	RJ1BYTE361	RJ1BYTE360
DD	11011101	RJ1BYTE357	RJ1BYTE356	RJ1BYTE355	RJ1BYTE354	RJ1BYTE353	RJ1BYTE352	RJ1BYTE351	RJ1BYTE350
DE	11011110	RJ1BYTE347	RJ1BYTE346	RJ1BYTE345	RJ1BYTE344	RJ1BYTE343	RJ1BYTE342	RJ1BYTE341	RJ1BYTE340
DF	11011111	RJ1BYTE337	RJ1BYTE336	RJ1BYTE335	RJ1BYTE334	RJ1BYTE333	RJ1BYTE332	RJ1BYTE331	RJ1BYTE330
E0	11100000	RJ1BYTE327	RJ1BYTE326	RJ1BYTE325	RJ1BYTE324	RJ1BYTE323	RJ1BYTE322	RJ1BYTE321	RJ1BYTE320
E1	11100001	RJ1BYTE317	RJ1BYTE316	RJ1BYTE315	RJ1BYTE314	RJ1BYTE313	RJ1BYTE312	RJ1BYTE311	RJ1BYTE310
E2	11100010	RJ1BYTE307	RJ1BYTE306	RJ1BYTE305	RJ1BYTE304	RJ1BYTE303	RJ1BYTE302	RJ1BYTE301	RJ1BYTE300
E3	11100011	RJ1BYTE297	RJ1BYTE296	RJ1BYTE295	RJ1BYTE294	RJ1BYTE293	RJ1BYTE292	RJ1BYTE291	RJ1BYTE290
E4	11100100	RJ1BYTE287	RJ1BYTE286	RJ1BYTE285	RJ1BYTE284	RJ1BYTE283	RJ1BYTE282	RJ1BYTE281	RJ1BYTE280
E5	11100101	RJ1BYTE277	RJ1BYTE276	RJ1BYTE275	RJ1BYTE274	RJ1BYTE273	RJ1BYTE272	RJ1BYTE271	RJ1BYTE270
E6	11100110	RJ1BYTE267	RJ1BYTE266	RJ1BYTE265	RJ1BYTE264	RJ1BYTE263	RJ1BYTE262	RJ1BYTE261	RJ1BYTE260
E7	11100111	RJ1BYTE257	RJ1BYTE256	RJ1BYTE255	RJ1BYTE254	RJ1BYTE253	RJ1BYTE252	RJ1BYTE251	RJ1BYTE250

Microprocessor Interface E1 Mode (continued)

Microprocessor Interface Register Architecture (continued)

Table 28. Device-Level Control, Alarm, and Mask Bits Register Set (continued)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
E8	11101000	RJ1BYTE247	RJ1BYTE246	RJ1BYTE245	RJ1BYTE244	RJ1BYTE243	RJ1BYTE242	RJ1BYTE241	RJ1BYTE240
E9	11101001	RJ1BYTE237	RJ1BYTE236	RJ1BYTE235	RJ1BYTE234	RJ1BYTE233	RJ1BYTE232	RJ1BYTE231	RJ1BYTE230
EA	11101010	RJ1BYTE227	RJ1BYTE226	RJ1BYTE225	RJ1BYTE224	RJ1BYTE223	RJ1BYTE222	RJ1BYTE221	RJ1BYTE220
EB	11101011	RJ1BYTE217	RJ1BYTE216	RJ1BYTE215	RJ1BYTE214	RJ1BYTE213	RJ1BYTE212	RJ1BYTE211	RJ1BYTE210
EC	11101100	RJ1BYTE207	RJ1BYTE206	RJ1BYTE205	RJ1BYTE204	RJ1BYTE203	RJ1BYTE202	RJ1BYTE201	RJ1BYTE200
ED	11101101	RJ1BYTE197	RJ1BYTE196	RJ1BYTE195	RJ1BYTE194	RJ1BYTE193	RJ1BYTE192	RJ1BYTE191	RJ1BYTE190
EE	11101110	RJ1BYTE187	RJ1BYTE186	RJ1BYTE185	RJ1BYTE184	RJ1BYTE183	RJ1BYTE182	RJ1BYTE181	RJ1BYTE180
EF	11101111	RJ1BYTE177	RJ1BYTE176	RJ1BYTE175	RJ1BYTE174	RJ1BYTE173	RJ1BYTE172	RJ1BYTE171	RJ1BYTE170
F0	11110000	RJ1BYTE167	RJ1BYTE166	RJ1BYTE165	RJ1BYTE164	RJ1BYTE163	RJ1BYTE162	RJ1BYTE161	RJ1BYTE160
F1	11110001	RJ1BYTE157	RJ1BYTE156	RJ1BYTE155	RJ1BYTE154	RJ1BYTE153	RJ1BYTE152	RJ1BYTE151	RJ1BYTE150
F2	11110010	RJ1BYTE147	RJ1BYTE146	RJ1BYTE145	RJ1BYTE144	RJ1BYTE143	RJ1BYTE142	RJ1BYTE141	RJ1BYTE140
F3	11110011	RJ1BYTE137	RJ1BYTE136	RJ1BYTE135	RJ1BYTE134	RJ1BYTE133	RJ1BYTE132	RJ1BYTE131	RJ1BYTE130
F4	11110100	RJ1BYTE127	RJ1BYTE126	RJ1BYTE125	RJ1BYTE124	RJ1BYTE123	RJ1BYTE122	RJ1BYTE121	RJ1BYTE120
F5	11110101	RJ1BYTE117	RJ1BYTE116	RJ1BYTE115	RJ1BYTE114	RJ1BYTE113	RJ1BYTE112	RJ1BYTE111	RJ1BYTE110
F6	11110110	RJ1BYTE107	RJ1BYTE106	RJ1BYTE105	RJ1BYTE104	RJ1BYTE103	RJ1BYTE102	RJ1BYTE101	RJ1BYTE100
F7	11110111	RJ1BYTE97	RJ1BYTE96	RJ1BYTE95	RJ1BYTE94	RJ1BYTE93	RJ1BYTE92	RJ1BYTE91	RJ1BYTE90
F8	11111000	RJ1BYTE87	RJ1BYTE86	RJ1BYTE85	RJ1BYTE84	RJ1BYTE83	RJ1BYTE82	RJ1BYTE81	RJ1BYTE80
F9	11111001	RJ1BYTE77	RJ1BYTE76	RJ1BYTE75	RJ1BYTE74	RJ1BYTE73	RJ1BYTE72	RJ1BYTE71	RJ1BYTE70
FA	11111010	RJ1BYTE67	RJ1BYTE66	RJ1BYTE65	RJ1BYTE64	RJ1BYTE63	RJ1BYTE62	RJ1BYTE61	RJ1BYTE60
FB	11111011	RJ1BYTE57	RJ1BYTE56	RJ1BYTE55	RJ1BYTE54	RJ1BYTE53	RJ1BYTE52	RJ1BYTE51	RJ1BYTE50
FC	11111100	RJ1BYTE47	RJ1BYTE46	RJ1BYTE45	RJ1BYTE44	RJ1BYTE43	RJ1BYTE42	RJ1BYTE41	RJ1BYTE40
FD	11111101	RJ1BYTE37	RJ1BYTE36	RJ1BYTE35	RJ1BYTE34	RJ1BYTE33	RJ1BYTE32	RJ1BYTE31	RJ1BYTE30
FE	11111110	RJ1BYTE27	RJ1BYTE26	RJ1BYTE25	RJ1BYTE24	RJ1BYTE23	RJ1BYTE22	RJ1BYTE21	RJ1BYTE20
FF	11111111	RJ1BYTE17	RJ1BYTE16	RJ1BYTE15	RJ1BYTE14	RJ1BYTE13	RJ1BYTE12	RJ1BYTE11	RJ1BYTE10
When TJ1BYTE_RD = 1									
C0	11000000	TJ1BYTE647	TJ1BYTE646	TJ1BYTE645	TJ1BYTE644	TJ1BYTE643	TJ1BYTE642	TJ1BYTE641	TJ1BYTE640
C1	11000001	TJ1BYTE637	TJ1BYTE636	TJ1BYTE635	TJ1BYTE634	TJ1BYTE633	TJ1BYTE632	TJ1BYTE631	TJ1BYTE630
C2	11000010	TJ1BYTE627	TJ1BYTE626	TJ1BYTE625	TJ1BYTE624	TJ1BYTE623	TJ1BYTE622	TJ1BYTE621	TJ1BYTE620
C3	11000011	TJ1BYTE617	TJ1BYTE616	TJ1BYTE615	TJ1BYTE614	TJ1BYTE613	TJ1BYTE612	TJ1BYTE611	TJ1BYTE610
C4	11000100	TJ1BYTE607	TJ1BYTE606	TJ1BYTE605	TJ1BYTE604	TJ1BYTE603	TJ1BYTE602	TJ1BYTE601	TJ1BYTE600
C5	11000101	TJ1BYTE597	TJ1BYTE596	TJ1BYTE595	TJ1BYTE594	TJ1BYTE593	TJ1BYTE592	TJ1BYTE591	TJ1BYTE590
C6	11000110	TJ1BYTE587	TJ1BYTE586	TJ1BYTE585	TJ1BYTE584	TJ1BYTE583	TJ1BYTE582	TJ1BYTE581	TJ1BYTE580
C7	11000111	TJ1BYTE577	TJ1BYTE576	TJ1BYTE575	TJ1BYTE574	TJ1BYTE573	TJ1BYTE572	TJ1BYTE571	TJ1BYTE570
C8	11001000	TJ1BYTE567	TJ1BYTE566	TJ1BYTE565	TJ1BYTE564	TJ1BYTE563	TJ1BYTE562	TJ1BYTE561	TJ1BYTE560
C9	11001001	TJ1BYTE557	TJ1BYTE556	TJ1BYTE555	TJ1BYTE554	TJ1BYTE553	TJ1BYTE552	TJ1BYTE551	TJ1BYTE550
CA	11001010	TJ1BYTE547	TJ1BYTE546	TJ1BYTE545	TJ1BYTE544	TJ1BYTE543	TJ1BYTE542	TJ1BYTE541	TJ1BYTE540
CB	11001011	TJ1BYTE537	TJ1BYTE536	TJ1BYTE535	TJ1BYTE534	TJ1BYTE533	TJ1BYTE532	TJ1BYTE531	TJ1BYTE530
CC	11001100	TJ1BYTE527	TJ1BYTE526	TJ1BYTE525	TJ1BYTE524	TJ1BYTE523	TJ1BYTE522	TJ1BYTE521	TJ1BYTE520
CD	11001101	TJ1BYTE517	TJ1BYTE516	TJ1BYTE515	TJ1BYTE514	TJ1BYTE513	TJ1BYTE512	TJ1BYTE511	TJ1BYTE510
CE	11001110	TJ1BYTE507	TJ1BYTE506	TJ1BYTE505	TJ1BYTE504	TJ1BYTE503	TJ1BYTE502	TJ1BYTE501	TJ1BYTE500
CF	11001111	TJ1BYTE497	TJ1BYTE496	TJ1BYTE495	TJ1BYTE494	TJ1BYTE493	TJ1BYTE492	TJ1BYTE491	TJ1BYTE490
D0	11010000	TJ1BYTE487	TJ1BYTE486	TJ1BYTE485	TJ1BYTE484	TJ1BYTE483	TJ1BYTE482	TJ1BYTE481	TJ1BYTE480
D1	11010001	TJ1BYTE477	TJ1BYTE476	TJ1BYTE475	TJ1BYTE474	TJ1BYTE473	TJ1BYTE472	TJ1BYTE471	TJ1BYTE470
D2	11010010	TJ1BYTE467	TJ1BYTE466	TJ1BYTE465	TJ1BYTE464	TJ1BYTE463	TJ1BYTE462	TJ1BYTE461	TJ1BYTE460

Microprocessor Interface E1 Mode (continued)

Microprocessor Interface Register Architecture (continued)

Table 28. Device-Level Control, Alarm, and Mask Bits Register Set (continued)

Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D3	11010011	TJ1BYTE457	TJ1BYTE456	TJ1BYTE455	TJ1BYTE454	TJ1BYTE453	TJ1BYTE452	TJ1BYTE451	TJ1BYTE450
D4	11010100	TJ1BYTE447	TJ1BYTE446	TJ1BYTE445	TJ1BYTE444	TJ1BYTE443	TJ1BYTE442	TJ1BYTE441	TJ1BYTE440
D5	11010101	TJ1BYTE437	TJ1BYTE436	TJ1BYTE435	TJ1BYTE434	TJ1BYTE433	TJ1BYTE432	TJ1BYTE431	TJ1BYTE430
D6	11010110	TJ1BYTE427	TJ1BYTE426	TJ1BYTE425	TJ1BYTE424	TJ1BYTE423	TJ1BYTE422	TJ1BYTE421	TJ1BYTE420
D7	11010111	TJ1BYTE417	TJ1BYTE416	TJ1BYTE415	TJ1BYTE414	TJ1BYTE413	TJ1BYTE412	TJ1BYTE411	TJ1BYTE410
D8	11011000	TJ1BYTE407	TJ1BYTE406	TJ1BYTE405	TJ1BYTE404	TJ1BYTE403	TJ1BYTE402	TJ1BYTE401	TJ1BYTE400
D9	11011001	TJ1BYTE397	TJ1BYTE396	TJ1BYTE395	TJ1BYTE394	TJ1BYTE393	TJ1BYTE392	TJ1BYTE391	TJ1BYTE390
DA	11011010	TJ1BYTE387	TJ1BYTE386	TJ1BYTE385	TJ1BYTE384	TJ1BYTE383	TJ1BYTE382	TJ1BYTE381	TJ1BYTE380
DB	11011011	TJ1BYTE377	TJ1BYTE376	TJ1BYTE375	TJ1BYTE374	TJ1BYTE373	TJ1BYTE372	TJ1BYTE371	TJ1BYTE370
DC	11011100	TJ1BYTE367	TJ1BYTE366	TJ1BYTE365	TJ1BYTE364	TJ1BYTE363	TJ1BYTE362	TJ1BYTE361	TJ1BYTE360
DD	11011101	TJ1BYTE357	TJ1BYTE356	TJ1BYTE355	TJ1BYTE354	TJ1BYTE353	TJ1BYTE352	TJ1BYTE351	TJ1BYTE350
DE	11011110	TJ1BYTE347	TJ1BYTE346	TJ1BYTE345	TJ1BYTE344	TJ1BYTE343	TJ1BYTE342	TJ1BYTE341	TJ1BYTE340
DF	11011111	TJ1BYTE337	TJ1BYTE336	TJ1BYTE335	TJ1BYTE334	TJ1BYTE333	TJ1BYTE332	TJ1BYTE331	TJ1BYTE330
E0	11100000	TJ1BYTE327	TJ1BYTE326	TJ1BYTE325	TJ1BYTE324	TJ1BYTE323	TJ1BYTE322	TJ1BYTE321	TJ1BYTE320
E1	11100001	TJ1BYTE317	TJ1BYTE316	TJ1BYTE315	TJ1BYTE314	TJ1BYTE313	TJ1BYTE312	TJ1BYTE311	TJ1BYTE310
E2	11100010	TJ1BYTE307	TJ1BYTE306	TJ1BYTE305	TJ1BYTE304	TJ1BYTE303	TJ1BYTE302	TJ1BYTE301	TJ1BYTE300
E3	11100011	TJ1BYTE297	TJ1BYTE296	TJ1BYTE295	TJ1BYTE294	TJ1BYTE293	TJ1BYTE292	TJ1BYTE291	TJ1BYTE290
E4	11100100	TJ1BYTE287	TJ1BYTE286	TJ1BYTE285	TJ1BYTE284	TJ1BYTE283	TJ1BYTE282	TJ1BYTE281	TJ1BYTE280
E5	11100101	TJ1BYTE277	TJ1BYTE276	TJ1BYTE275	TJ1BYTE274	TJ1BYTE273	TJ1BYTE272	TJ1BYTE271	TJ1BYTE270
E6	11100110	TJ1BYTE267	TJ1BYTE266	TJ1BYTE265	TJ1BYTE264	TJ1BYTE263	TJ1BYTE262	TJ1BYTE261	TJ1BYTE260
E7	11100111	TJ1BYTE257	TJ1BYTE256	TJ1BYTE255	TJ1BYTE254	TJ1BYTE253	TJ1BYTE252	TJ1BYTE251	TJ1BYTE250
E8	11101000	TJ1BYTE247	TJ1BYTE246	TJ1BYTE245	TJ1BYTE244	TJ1BYTE243	TJ1BYTE242	TJ1BYTE241	TJ1BYTE240
E9	11101001	TJ1BYTE237	TJ1BYTE236	TJ1BYTE235	TJ1BYTE234	TJ1BYTE233	TJ1BYTE232	TJ1BYTE231	TJ1BYTE230
EA	11101010	TJ1BYTE227	TJ1BYTE226	TJ1BYTE225	TJ1BYTE224	TJ1BYTE223	TJ1BYTE222	TJ1BYTE221	TJ1BYTE220
EB	11101011	TJ1BYTE217	TJ1BYTE216	TJ1BYTE215	TJ1BYTE214	TJ1BYTE213	TJ1BYTE212	TJ1BYTE211	TJ1BYTE210
EC	11101100	TJ1BYTE207	TJ1BYTE206	TJ1BYTE205	TJ1BYTE204	TJ1BYTE203	TJ1BYTE202	TJ1BYTE201	TJ1BYTE200
ED	11101101	TJ1BYTE197	TJ1BYTE196	TJ1BYTE195	TJ1BYTE194	TJ1BYTE193	TJ1BYTE192	TJ1BYTE191	TJ1BYTE190
EE	11101110	TJ1BYTE187	TJ1BYTE186	TJ1BYTE185	TJ1BYTE184	TJ1BYTE183	TJ1BYTE182	TJ1BYTE181	TJ1BYTE180
EF	11101111	TJ1BYTE177	TJ1BYTE176	TJ1BYTE175	TJ1BYTE174	TJ1BYTE173	TJ1BYTE172	TJ1BYTE171	TJ1BYTE170
F0	11110000	TJ1BYTE167	TJ1BYTE166	TJ1BYTE165	TJ1BYTE164	TJ1BYTE163	TJ1BYTE162	TJ1BYTE161	TJ1BYTE160
F1	11110001	TJ1BYTE157	TJ1BYTE156	TJ1BYTE155	TJ1BYTE154	TJ1BYTE153	TJ1BYTE152	TJ1BYTE151	TJ1BYTE150
F2	11110010	TJ1BYTE147	TJ1BYTE146	TJ1BYTE145	TJ1BYTE144	TJ1BYTE143	TJ1BYTE142	TJ1BYTE141	TJ1BYTE140
F3	11110011	TJ1BYTE137	TJ1BYTE136	TJ1BYTE135	TJ1BYTE134	TJ1BYTE133	TJ1BYTE132	TJ1BYTE131	TJ1BYTE130
F4	11110100	TJ1BYTE127	TJ1BYTE126	TJ1BYTE125	TJ1BYTE124	TJ1BYTE123	TJ1BYTE122	TJ1BYTE121	TJ1BYTE120
F5	11110101	TJ1BYTE117	TJ1BYTE116	TJ1BYTE115	TJ1BYTE114	TJ1BYTE113	TJ1BYTE112	TJ1BYTE111	TJ1BYTE110
F6	11110110	TJ1BYTE107	TJ1BYTE106	TJ1BYTE105	TJ1BYTE104	TJ1BYTE103	TJ1BYTE102	TJ1BYTE101	TJ1BYTE100
F7	11110111	TJ1BYTE97	TJ1BYTE96	TJ1BYTE95	TJ1BYTE94	TJ1BYTE93	TJ1BYTE92	TJ1BYTE91	TJ1BYTE90
F8	11111000	TJ1BYTE87	TJ1BYTE86	TJ1BYTE85	TJ1BYTE84	TJ1BYTE83	TJ1BYTE82	TJ1BYTE81	TJ1BYTE80
F9	11111001	TJ1BYTE77	TJ1BYTE76	TJ1BYTE75	TJ1BYTE74	TJ1BYTE73	TJ1BYTE72	TJ1BYTE71	TJ1BYTE70
FA	11111010	TJ1BYTE67	TJ1BYTE66	TJ1BYTE65	TJ1BYTE64	TJ1BYTE63	TJ1BYTE62	TJ1BYTE61	TJ1BYTE60
FB	11111011	TJ1BYTE57	TJ1BYTE56	TJ1BYTE55	TJ1BYTE54	TJ1BYTE53	TJ1BYTE52	TJ1BYTE51	TJ1BYTE50
FC	11111100	TJ1BYTE47	TJ1BYTE46	TJ1BYTE45	TJ1BYTE44	TJ1BYTE43	TJ1BYTE42	TJ1BYTE41	TJ1BYTE40
FD	11111101	TJ1BYTE37	TJ1BYTE36	TJ1BYTE35	TJ1BYTE34	TJ1BYTE33	TJ1BYTE32	TJ1BYTE31	TJ1BYTE30
FE	11111110	TJ1BYTE27	TJ1BYTE26	TJ1BYTE25	TJ1BYTE24	TJ1BYTE23	TJ1BYTE22	TJ1BYTE21	TJ1BYTE20
FF	11111111	TJ1BYTE17	TJ1BYTE16	TJ1BYTE15	TJ1BYTE14	TJ1BYTE13	TJ1BYTE12	TJ1BYTE11	TJ1BYTE10

Microprocessor Interface E1 Mode
(continued)

Microprocessor Interface Register Architecture (continued)

Device-Level Control, Alarm, and Mask Bits (0x00—0x16)

Register 0x00. The reset bit in register 0x00 is used to reset all registers in the microprocessor interface as well as all of the state machines within the device. Activating this bit has the same effect as applying a logic 0 to the device input pin $\overline{\text{RESET}}$. Activating this bit **will** interrupt service. This bit must be written to a logic 1 to activate.

- The BIP2BLKCNT bit is used to determine whether the BIP2CNT counters count the number of BIP-2 errors (BIP2BLKCNT = 0) or the number of BIP-2 blocks that contain errors (BIP2BLKCNT = 1).
- The device can accept a blue signal clock at either the exact DS1 rate (BLUECLKSEL = 0), or at 16 times the DS1 rate (BLUECLKSEL = 1).
- The device has a number of BIP, FEBE, and pointer adjustment counters that are all updated when the LATCH_CNT bit is written from a 0 to a 1. Nothing happens when the bit is written from a 1 to a 0. The only internal counter that is not updated by this bit is the test pattern counter.
- B1ERRINS, B2ERRINS, and B3ERRINS all cause continuous BIP-8 errors to be transmitted in their respective BIP-8 values.
- TEST_CNT is used to put all internal counters into test mode.

The reset default value for this register is 00000000.

Register 0x01. The bits in register 0x01 are used to provision device level control bits. The reset default for this register is 00000000. The functions of these bits are described below:

- When FEBE_EN = 1, the device will automatically insert the appropriate FEBE into the transmitted Z2, G1, V5 overhead bytes whenever it receives BIP errors. If FEBE_EN = 0, then the automatic insertion of FEBE is disabled.
- When TXPAISINS = 1, the device will write all ones into the pointer bytes (H1—H3) and all of the synchronous payload envelope (SPE).
- The TXFSYNC is used to identify where the frame sync pulse is active. When TXFSYNC = 0, the device places the output frame sync on the first clock of the frame; otherwise, the frame sync pulse is active on the last clock of the frame.
- When AU3SCR = 1, the device scrambles the outgoing AU-3 frame according to the SDH frame synchronous scrambling sequence $x^7 + x^6 + 1$. The sequence is reset to 1111111 at the beginning of the byte following the C1 byte and scrambles all of the AU-3 data except the A1, A2, and C1 bytes. When this bit is 0, then the transmit data is not scrambled by the device.
- When AU3DSCR = 1, the device scrambles the incoming AU-3 frame according to the SDH frame synchronous descrambling sequence $x^7 + x^6 + 1$. The sequence is reset to 1111111 at the beginning of the byte following the C1 byte and descrambles all of the AU-3 data except the A1, A2, and C1 bytes. When this bit is 0, then the receive data is not descrambled by the device.
- When AU3LB = 1, the transmitted data is looped back to the receive side. When this bit is 0, the device uses the received data.

Register 0x02. The bits in register 0x02 are used to set the edges that retime data into and out of the device. The reset default for this register is 00000000.

- All of the edge registers act such that a logic 1 means that the data is retimed (either in or out) by the rising clock edge; a logic 0 means that the data is retimed by the falling edge.
- Both the TXPARITY and RXPARITY bits determine the type of parity for data buses. When these bits are written with a logic 1, then odd parity is used; even parity otherwise.
- Both the TXSERIAL and RXSERIAL bits are used to set the type of AU-3 data. When either serial bit is written to a logic 1, then the AU-3 rail is run serially; parallel mode is used otherwise.

Register 0x03. The bits in register 0x03 are used to report problems at the receive AU-3 level. The reset default for this register is 00000000.

- AU3OOF = 1 reports an out of frame condition on the receive AU-3 signal.
- AU3LOF = 1 reports an out of frame condition that persists for more than 3 ms.
- AU3LOP = 1 reports a loss of AU-3 pointer.
- AU3PAIS = 1 reports path AIS as detected by the receive pointer interpreter.
- RXPARER = 1 reports a parity violation on the receive AU-3 data bus. This signal is only meaningful when the parallel input mode is selected.

Microprocessor Interface E1 Mode (continued)

Microprocessor Interface Register Architecture (continued)

- The device monitors the incoming H4 byte for loss of multiframe indication (H4LOMF = 1).
- The device monitors the received J1 byte for path trace mismatches. When the received J1 byte pattern doesn't match the previously received pattern, then TRACEER = 1.
- The device monitors the received G1 byte for path RDI. The PATHRDI bit reflects the current state of this bit.

Register 0x04. The bits in register 0x04 are used to mask the contributions of the bits in register 0x03 to the microprocessor interrupt output, INT. The reset default for this register is 11111111. When any of these bits are at a logic 1 level, the corresponding bit in register 0x03 is masked from contributing to the output interrupt. The reset default for this register masks all of the bits in register 0x03.

Register 0x05. The bits in register 0x05 are used to report problems at the receive TU-12 level. The bits in this register are actually composite bits. The bits that report the problems at the TU-12 level are actually located in 21 separate registers (one for each TU12) as described below. These composite bits are placed in the register map as a convenience to determine which type of error was detected. Any time any of the 21 TU-12 bits reports an error, the corresponding composite bit will report an error. The reset default for this register is 00000000.

- E1AISCOM = 1 reports an AIS condition on E1.
- E1LOCCOM = 1 reports a loss of input E1 clock.
- TULABCOM = 1 reports change of state of the TU-12 label. In order for this bit to be set, the device must detect three consecutive consistent new values for the TU-12 label.
- TUAISCOM = 1 reports the fact that the V1 and V2 pointer bytes are all ones for three consecutive superframes.
- TURDICOM = 1 reports the fact that the TU RDI bit has been received as a logic 1 for three consecutive superframes.
- TULOPCOM = 1 reports TU loss of pointer.
- TUSIZECOM = 1 reports incorrect TU-12 size bits. The valid TU size bits for TU-12 are 10.
- ESOFCOM = 1 reports that the device has experienced a receive or a transmit elastic store overflow.

Register 0x06. The bits in register 0x06 are used to mask the contributions of the bits in register 0x05 to the microprocessor interrupt output, INT. The reset default for this register is 11111111. When any of these bits are at a logic 1 level, the corresponding bit in register 0x05 is masked from contributing to the output interrupt. The reset default for this register masks all of the bits in register 0x05.

Register 0x07. Bit 0 of register 0x07 is used to report the value of the DS1_E1N input pin.

Register 0x08. The bits in register 0x08 are not currently used.

Register 0x09. The bits in register 0x09 are used to determine which DS1 is selected to drop the test pattern. When TPDROPSIDE = 1, the test pattern is dropped from the SPE drop logic, and the DS1 output that is dropped is the same as described in VT Drop Selection (0x33—0x4E) section on page 36. When TPDROPSIDE = 0, the DS1 that is dropped is the same as described in DS1 Insertion Selection (0x17—0x32) section on page 36.

Register 0x0A. The bits in register 0x0A indicate the condition of the test pattern detector. If the test pattern detector has been able to sync on the dropped signal, then TPOOS = 0. When TPOOS = 0, then the TPERR bits are used to keep a count of the number of bit errors that the test pattern detector has seen. This error count is cleared when the register is read by the microprocessor. This byte defaults to 10000000.

Register 0x0B. The bits in register 0x0B are used to report the F2 receive byte in the path overhead. The default value for this register is 00000000.

Register 0x0C. The bits in register 0x0C are used to report the received C2 label byte in the path overhead. The default value for this register is 00000000 which indicates path unequipped.

Register 0x0D. The bits in register 0x0D are used to report the four least significant bits of the G1 path overhead byte and the three least significant bits of the K2 section overhead byte. The default value for this register is 00000000.

Register 0x0E—0x0F. The bits in register 0x0E—0x0F are used to set the number of consecutive, consistent values required by the previous three registers before updating their values. Valid values for these registers range from 3 to 15. Values less than 3 default to 3. These two registers default to 00110011.

Microprocessor Interface E1 Mode (continued)

Microprocessor Interface Register Architecture (continued)

The bits in registers 0x10—0x16 report the receive and transmit elastic store overflow condition. When any of these bits is 1, then the corresponding E1 input has experienced an elastic store overflow condition. This value is latched by these bits and cleared when read.

E1 Insertion Selection (0x17—0x2B)

The E1AISx bits in bit 7 report the received E1 AIS condition. When any of these bits are 1, then the corresponding E1 input has an AIS condition. This value represents the current received state, and the AIS condition is not latched by these bits.

The E1LOCx bits in bit 6 report the received E1 loss of clock condition. When any of these bits are 1, then the corresponding E1 input has a received loss of clock condition. This value represents the current received state, and the loss of clock condition is not latched by these bits.

The E1xLB bits in bit 5 are used to force E1 loopback from output to input. When any of these bits are 1, then the corresponding E1 input is overwritten by the outgoing E1 signal for that location.

The E1 selected corresponds to the decimal value of the programmed 5 bits. If these bits contain 00000, then the device will insert unequipped into the corresponding TU-12 slot. If these bits contain 11101—11110, then the device will insert TUAIS into the corresponding TU-12 slot. Since the device defaults all 21 of these registers to the value 00000, then all of the 21 TU-12 slots start off transmitting unequipped following reset. The value 11111 inserts the test pattern.

The E1_INSx[4:0] bits in register 0x17—0x2B are used to select the E1 input for the transmit TU-12 slots. The reset default for these registers is 00000000. Addresses 17—2B correspond to TU-12s as shown in Table 29.

Table 29. E1 Insertion Selection Format

			5 Programmed Data Bits				
TU-12 #	TU Group #	Address #	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	1	17	0	0	0	0	1
2	2	18	0	0	0	1	0
3	3	19	0	0	0	1	1
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
19	5	29	1	0	0	1	1
20	6	2A	1	0	1	0	0
21	7	2B	1	0	1	0	1

TU Drop Selection (0x33—0x47)

The RXESOFx bits in bit 6 report the receive elastic store overflow condition. When any of these bits are 1, then the corresponding E1 output has experienced an elastic store overflow. This value is latched by these bits until read by the microprocessor.

The TXESOFx bits in bit 5 report the transmit elastic store overflow condition. When any of these bits are 1, then the corresponding E1 input has experienced an elastic store overflow. This value is latched by these bits until read by the microprocessor.

The bits in register 0x33—0x47 are used to select the TU-12 slot for the E1 outputs. The reset default for these registers is 00000000. TUxDROP 00001—10101 correspond to TU12s as shown in Table 30.

Microprocessor Interface E1 Mode (continued)

Microprocessor Interface Register Architecture (continued)

Table 30. TU Drop Selection Format

		5 Programmed Data Bits				
TU-12 #	TU Group #	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	1	0	0	0	0	1
2	2	0	0	0	1	0
3	3	0	0	0	1	1
• •	• •	• •	• •	• •	• •	• •
19	5	1	0	0	1	1
20	6	1	0	1	0	0
21	7	1	0	1	0	1

Address 0x33—0x47 correspond to E1s as shown in Table 31.

Table 31. TU to E1 Mapping

E1 #	Address
1	33
2	34
3	35
• •	• •
19	45
20	46
21	47

If these addresses contain either 00000 or 10110—11110, then the device will insert E1 AIS into the corresponding E1 output. Since the device defaults all 21 of these registers to the value 00000, then all of the 21 E1 outputs start off transmitting E1 AIS following reset. The value of 11111 is used to select the test pattern into this TU-12 slot.

TX TU Overhead Insertion Control (0x4F—0x63)

The bits in register 0x4F—0x63 are used to select the TU-12 slot for the insertion control bits in the same way as described in E1 Insertion Selection (0x17—0x2B) section on page 77. The bits in these registers provision the transmitted TU-12 overhead byte, V5. The reset default for this register is 00000000.

- BIP2ERINSx = 1 forces the selected TU-12 to transmit inverted BIP-2 bits which causes the downstream receiver to declare continuous BIP-2 errors.
- TURDIINSx directly programs the transmitted TU RDI bit (i.e., a logic 1 in this position causes a logic 1 to be inserted).
- TUAISINSx = 1 forces TU AIS to be written into the corresponding TU-12 slot. This consists of writing all ones into the selected TU-12 slot.
- TULAB[2:0]INSx directly program the transmitted TU label bits. These bits are used to carry unequipped information (TULAB[2:0] = 000) as well as specific payload mappings and TUAIS.

Microprocessor Interface E1 Mode
(continued)

Microprocessor Interface Register Architecture (continued)

RX TU Drop Monitoring (0x6B—0x7F)

The bits in register 0x6B—0x7F are used to report the TU-12 slot status. The reset default for these registers is 00000000.

The bits in these registers correspond to the received TU-12 slot in the same way as described in E1 Insertion Selection (0x17—0x2B) section on page 77. The conditions that these bits report are described in Device-Level Control, Alarm, and Mask Bits (0x00—0x16) section on page 75 for the composite bits.

Block Control Register (0xBF)

The bits in register 0xBF control the information presented to the microprocessor from the registers 0xC0—0xFF. These last 64 bytes will display different results depending on the value programmed into this byte. There is a hierarchy of evaluation of these bytes; if BIP_CNTS = 1, then the data in these registers is BIP error information regardless of the values of the other bits in this register. Otherwise, if FEBE_CNTS = 1 the information displayed is the FEBE error information. Otherwise, if RJ1BYTE = 1 then the received J1 bytes are presented. All three of these previous sets of values are read only. The last setting, TJ1BYTE = 1, presents the transmit J1 byte values. These registers are read/write. Any values written into these registers will change the J1 byte values that are transmitted.

BIP_Cnts (0xC0—0xFF)

The bytes in registers 0xC0—0xFF are used to count the number of BIP errors detected by the device when BIP_CNTS = 1. The first six registers, 0xC0—0xC5, are the BIP errors detected by B1, B2, and B3. The remaining registers in the block are the errors seen by the BIP-2 error detectors in the individual TU-12 slots. In addition, since the BIP-2 errors only require 12 bits, the VT pointer increment counts are presented here. The values in all of these counters is latched by the LATCH_CNTS bit in register 0x00.

FEBE_Cnts (0xC0—0xFF)

The bytes in registers 0xC0—0xFF are used to count the number of FEBE errors detected by the device when FEBE_CNTS = 1 **and** BIP_CNTS = 0. The registers, 0xC2—0xC5, are the FEBE errors detected by B2, and B3. The remaining registers in the block are the errors seen by the FEBE error detectors in the individual TU-12 slots. In addition, since the TU FEBE errors only require 11 bits, the TU pointer decrement counts are presented here. The values in all of these counters is latched by the LATCH_CNTS bit in register 0x00.

Receive J1 Path Trace Bytes (0xC0—0xFF)

The bits in registers 0xC0—0xFE are used to read the received 64 path trace bytes when RJ1BYTE = 1 **and** BIP_CNTS = 0 **and** FEBE_CNTS = 0. The receive J1 path trace byte RJ1BYTE63[7:0] corresponds to the first byte in the 64-byte sequence, while the J1 path trace byte RJ1BYTE0[7:0] corresponds to the last byte in the 64-byte sequence. The default value for the 64-byte sequence is all zeros. These receive J1 byte values are continuously written into these registers modulo 64. If any received byte doesn't match the previously received byte for its location, TRACEER is set to 1.

Transmit J1 Path Trace Bytes (0xC0—0xFF)

The bits in registers 0xC0—0xFE are used to provision the transmit 64 path trace bytes when TJ1BYTE = 1 **and** RJ1BYTE = 0 **and** BIP_CNTS = 0 **and** FEBE_CNTS=0. The transmit J1 path trace byte TJ1BYTE63[7:0] corresponds to the first byte in the 64-byte sequence, while the J1 path trace byte TJ1BYTE0[7:0] corresponds to the last byte in the 64-byte sequence. The default value for the 64-byte sequence is all zeros. These registers can be written by the microprocessor.

Microprocessor Interface E1 Mode (continued)

I/O Timing

The I/O timing specifications for the microprocessor interface are given in Table 32. The microprocessor interface pins use CMOS I/O levels. All outputs, except the address/data bus AD[7:0], are rated for a capacitive load of 50 pF. The AD[7:0] outputs are rated for a 100 pF load. The minimum read and write cycle time is 200 ns for all device configurations.

Table 32. Microprocessor Interface I/O Timing Specifications

Symbol	Configuration	Parameter	Setup (ns) (Min)	Hold (ns) (Min)	Delay (ns) (Max)
t1	Modes 1 & 2	Address Valid to $\overline{AS}$ Asserted (Read, Write)	5	—	—
t2		$\overline{AS}$ Asserted to Address Invalid (Read, Write)	—	10	—
t3		$\overline{AS}$ Asserted to $\overline{DS}$ Asserted	0	—	—
t4		R/$\overline{W}$ High (Read) to $\overline{DS}$ Asserted	25	—	—
t5		$\overline{DS}$ Asserted (Read, Write) to $\overline{DTACK}$ Asserted	—	—	20
t6		$\overline{DTACK}$ Asserted to Data Valid (Read)	—	—	24
t7		$\overline{DS}$ Asserted (Read) to Data Valid	—	—	44
t8		$\overline{DS}$ Negated (Read, Write) to $\overline{AS}$ Negated	—	—	—
t9		$\overline{DS}$ Negated (Read) to Data Invalid	—	—	15
t10		$\overline{DS}$ Negated (Read) to $\overline{DTACK}$ Negated	—	—	15
t11		$\overline{AS}$ (Read, Write) Asserted Width	—	75	—
t12		$\overline{DS}$ (Read) Asserted Width	—	35	—
t13		$\overline{AS}$ Asserted to R/$\overline{W}$ Low (Write)	7	—	—
t14		R/$\overline{W}$ Low (Write) to $\overline{DS}$ Asserted	20	—	—
t15		Data Valid to $\overline{DS}$ Asserted (Write)	7.5	—	—
t16		$\overline{DS}$ Negated to $\overline{DTACK}$ Negated (Write)	—	—	20
t17		$\overline{DS}$ Negated to Data Invalid (Write)	—	—	7.5
t18		$\overline{DS}$ (Write) Asserted Width	—	35	—
t19	Modes 3 & 4	Address Valid to ALE Asserted Low (Read, Write)	15	—	—
t20		ALE Asserted Low (Read, Write) to Address Invalid	—	10	—
t21		ALE Asserted Low to $\overline{RD}$ Asserted (Read)	30	—	—
t22		$\overline{RD}$ Asserted (Read) to Data Valid	—	—	90
t23		$\overline{RD}$ Asserted (Read) to RDY Asserted	—	—	75
t24		$\overline{RD}$ Negated to Data Invalid (Read)	—	—	25
t25		$\overline{RD}$ Negated to RDY Negated (Read)	—	—	25
t26		ALE Asserted Low to $\overline{WR}$ Asserted (Write)	35	—	—
t27		$\overline{CS}$ Asserted to RDY Asserted Low	—	—	16
t28		Data Valid to $\overline{WR}$ Asserted (Write)	25	—	—
t29		$\overline{WR}$ Asserted (Write) to RDY Asserted	—	—	73
t30		$\overline{WR}$ Negated to RDY Negated (Write)	—	—	22
t31		$\overline{WR}$ Negated to Data Invalid	—	25	—
t32		ALE Asserted (Read, Write) Width	—	150	—
t33		$\overline{RD}$ Asserted (Read) Width	—	100	—
t34		$\overline{WR}$ Asserted (Write) Width	—	100	—

The read and write timing diagrams for all four microprocessor interface modes are shown in Figures 24—31.

Microprocessor Interface E1 Mode (continued)

I/O Timing (continued)

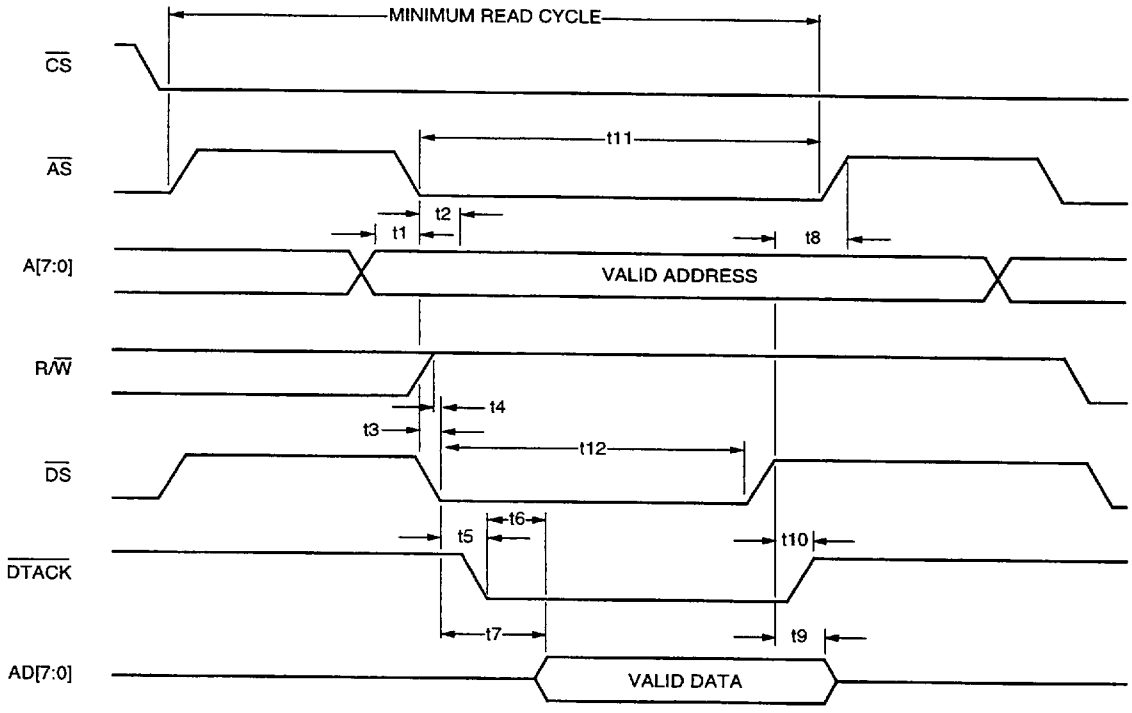

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Figure 24. Mode 1—Read Cycle Timing (MPMODE = 0, MPMUX = 0)

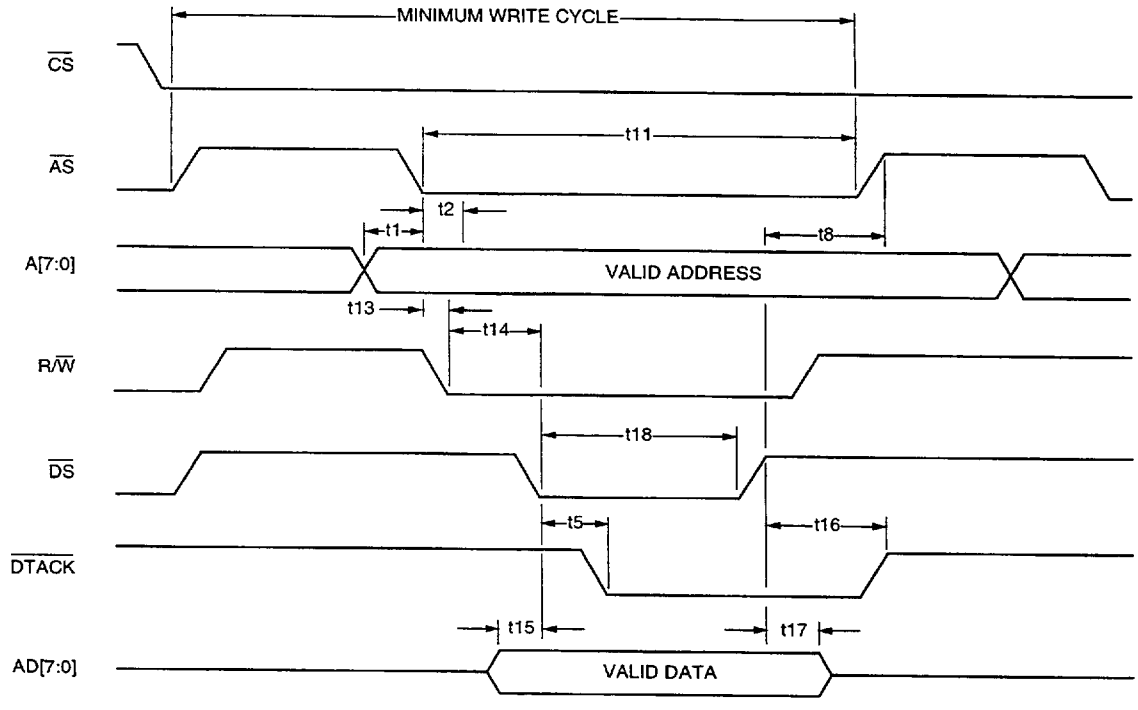

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Figure 25. Mode 1—Write Cycle Timing (MPMODE = 0, MPMUX = 0)

Microprocessor Interface E1 Mode (continued)

I/O Timing (continued)

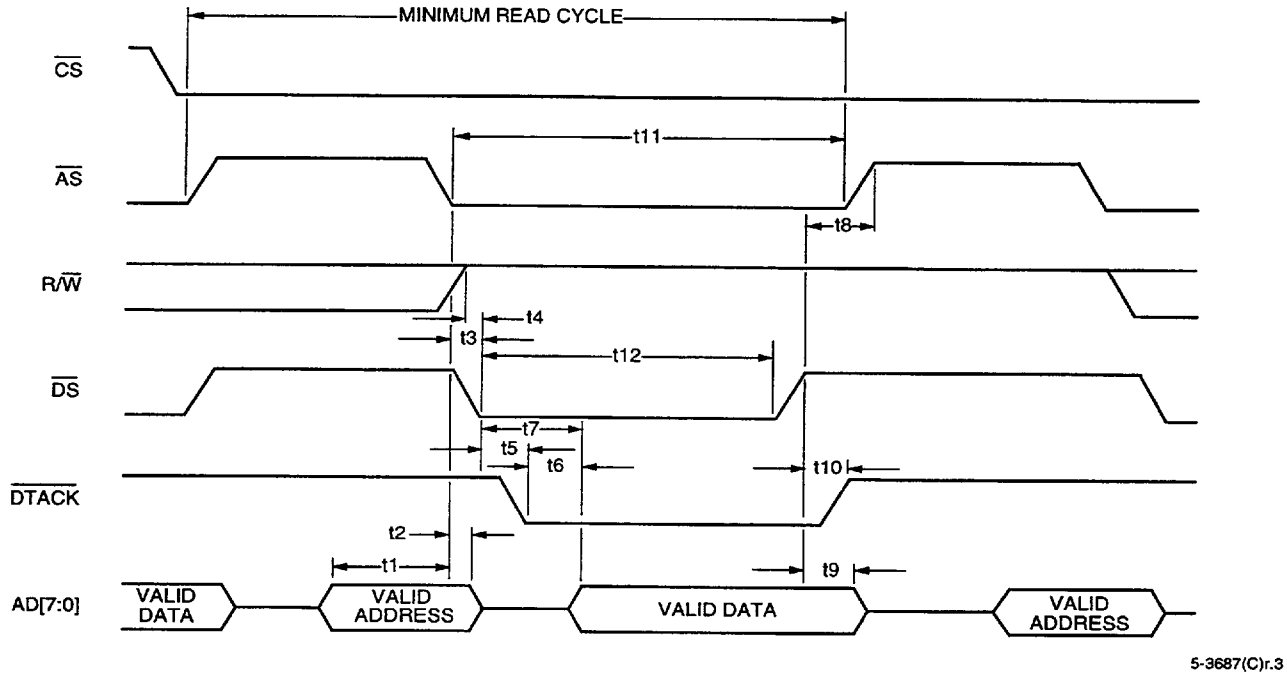

Figure 26. Mode 2—Read Cycle Timing (MPMODE = 0, MPMUX = 1)

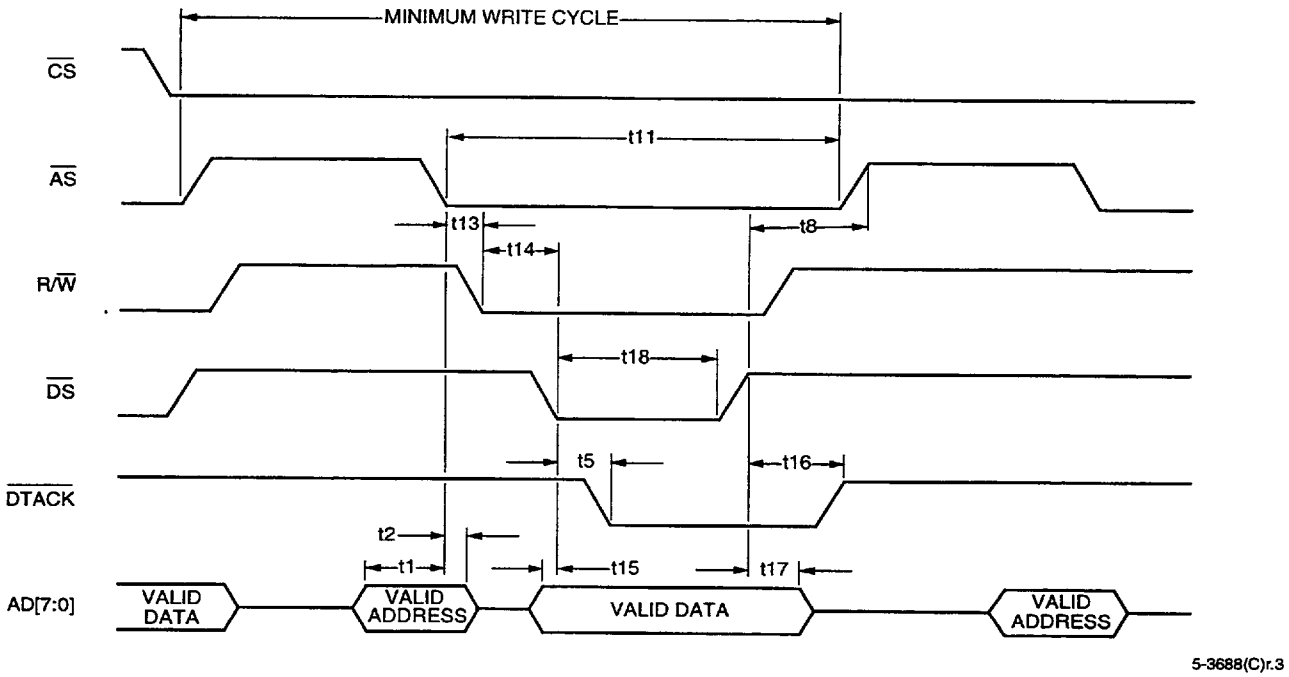

Figure 27. Mode 2—Write Cycle Timing (MPMODE = 0, MPMUX = 1)

Microprocessor Interface E1 Mode (continued)

I/O Timing (continued)

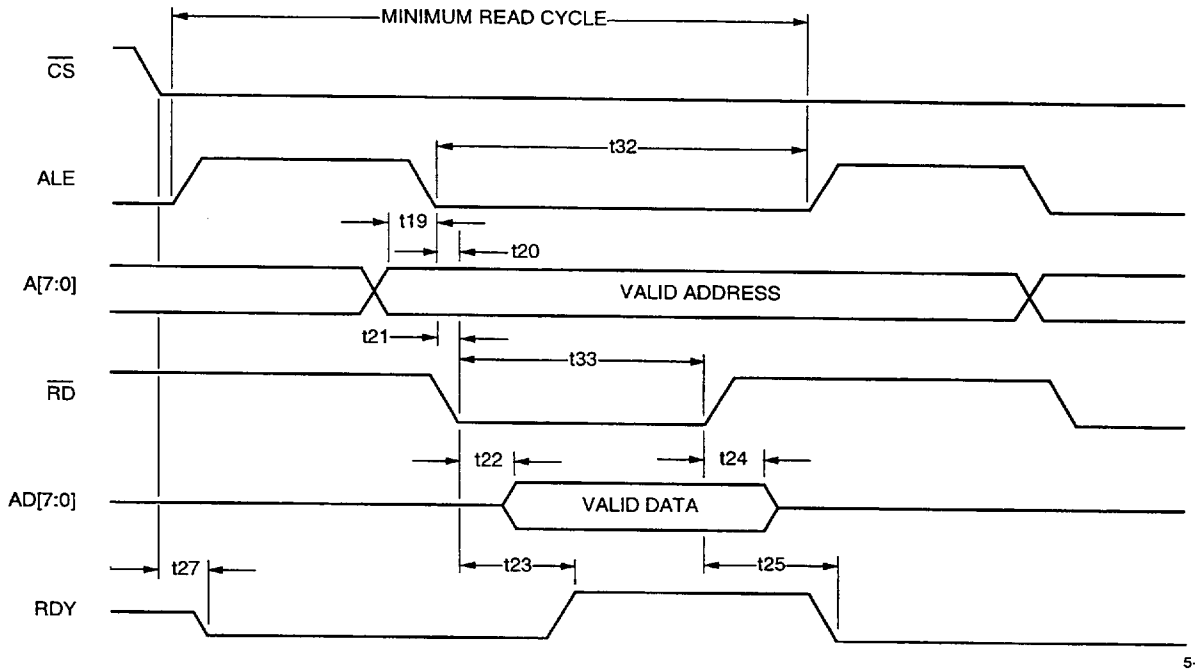

Figure 28. Mode 3—Read Cycle Timing (MPMODE = 1, MPMUX = 0)

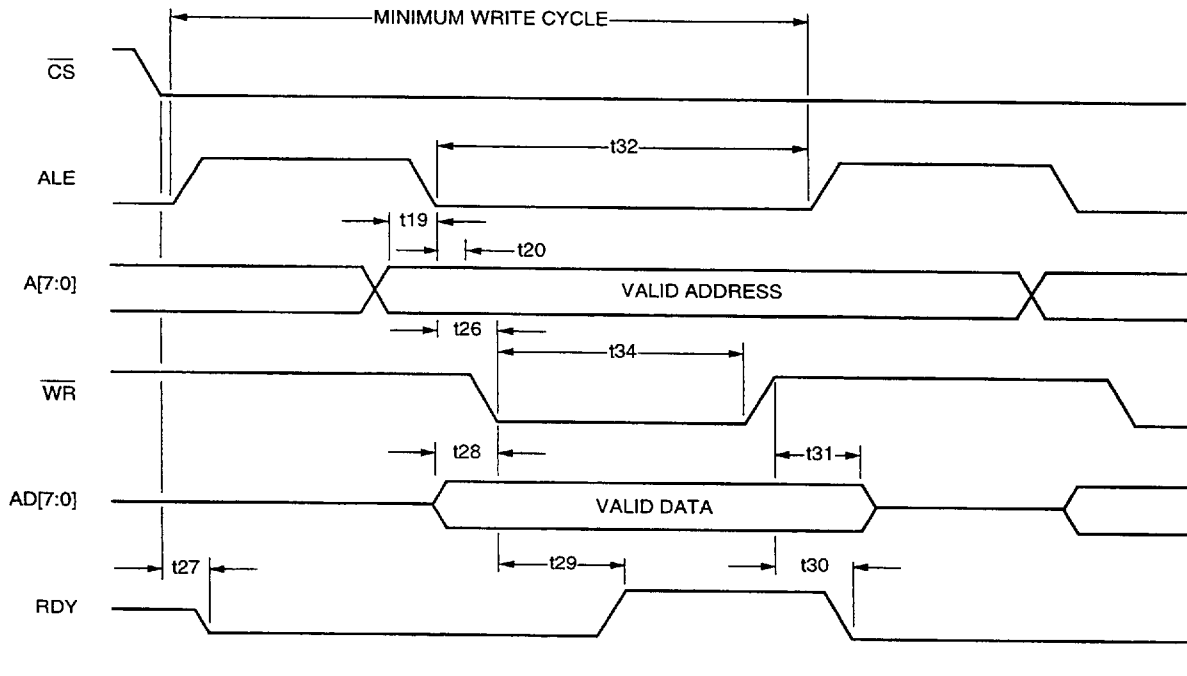

Figure 29. Mode 3—Write Cycle Timing (MPMODE = 1, MPMUX = 0)

Microprocessor Interface E1 Mode (continued)

I/O Timing (continued)

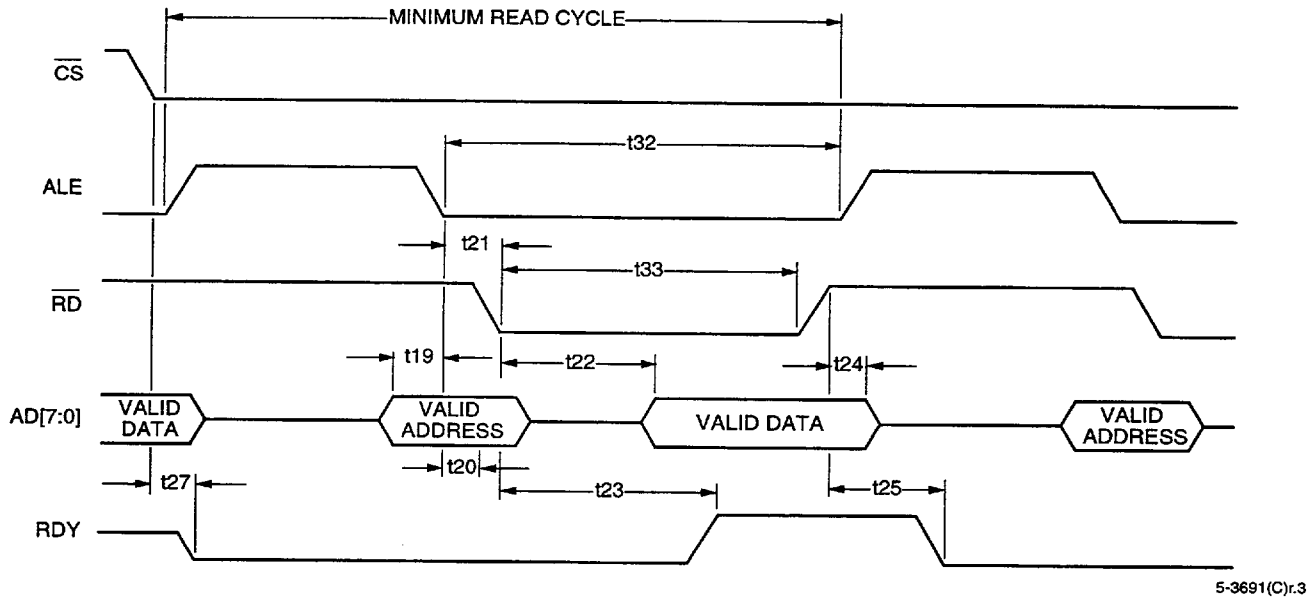

Figure 30. Mode 4—Read Cycle Timing (MPMODE = 1, MPMUX = 1)

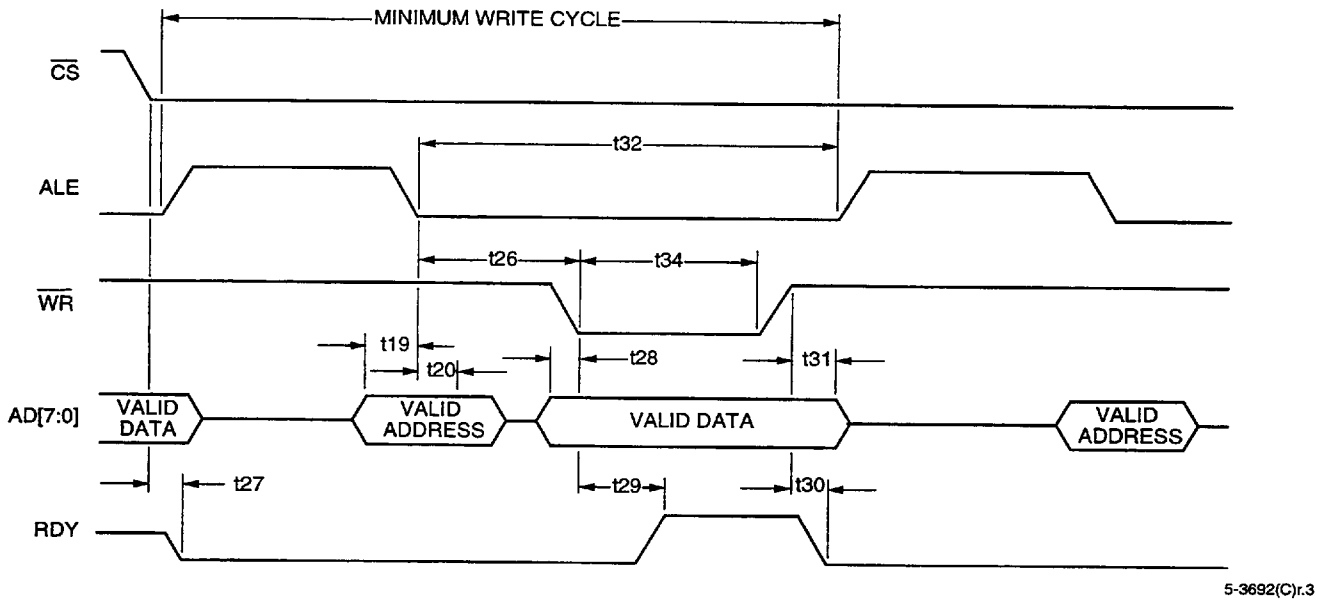

Figure 31. Mode 4—Write Cycle Timing (MPMODE = 1, MPMUX = 1)

Absolute Maximum Ratings E1 Mode

Stresses in excess of the absolute maximum ratings can cause permanent or latent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of this device specification. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Table 33. Absolute Maximum Ratings

Parameter	Min	Max	Unit
dc Supply Voltage	–0.5	6.5	V
Storage Temperature	–65	125	°C
Maximum Voltage with Respect to V_{DD}	—	0.5	V
Minimum Voltage with Respect to GND	–0.5	—	V

Handling Precautions E1 Mode

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. Lucent employs a human-body model (HBM) and charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used in the defined model. No industry-wide standard has been adopted for the CDM. However, a standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely used and, therefore, can be used for comparison purposes. The HBM ESD threshold presented here was obtained by using these circuit parameters.

Table 34. ESD Threshold Voltage

Device	Voltage
TMPR28051	TBD

Operating Conditions E1 Mode

Table 35. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Ambient Temperature	T_A	–40	—	85	°C
Power Supply	V_{DD}	4.75	5.0	5.25	V

Timing Characteristics E1 Mode

Table 36. Logic Interface Characteristics

An internal 100 kΩ pull-up is provided on the $\overline{ICT}$, $\overline{RESET}$, $\overline{CS}$, TCLK, TDI, TMS, $\overline{TRST}$, RSTS1DATA[7:0], RSTS1PAR, MPCLK, RCLKx, and RDATAx pins. This requires these input pins to sink no more than 20 µA. All buffers use CMOS levels.

Parameter	Symbol	Test Conditions	Min	Max	Unit
Input Voltage: Low High	 V_{IL} V_{IH}	—	 GND V_{DD} – 1.0	 1.0 V_{DD}	 V V
Input Leakage	I_L	—	—	1.0	µA
Output Voltage: Low High	 V_{OL} V_{OH}	 –5.0 mA 5.0 mA	 GND V_{DD} – 1.0	 0.5 V_{DD}	 V V
Input Capacitance	C_I	—	—	3.0	pF
Load Capacitance*	C_L	—	—	25	pF

* 100 pF allowed for AD[7:0] (pins 48 to 50 and 55 to 59).

Timing Characteristics E1 Mode (continued)

The generic digital system interface timing is shown in Figure 32. Table 37 lists the setup time (t_{SU}) and hold time (t_H) specifications for the transmission path data as well as the propagation delay (t_{PD}) information for the transmission path data.

Table 37. Generic Interface Data Timing

Symbol	Signal	Parameter	Min	Typ	Max	Unit
t_{SU}	RDATA[28:1]	RDATA[28:1]↑↓ to RCLK*[28:1]↑↓	50	—	—	ns
t_H		RDATA[28:1]↑↓ from RCLK*[28:1]↑↓	40	—	—	ns
t_{SU}	RAU3DATA[7:0]	RAU3DATA[7:0]↑↓ to RAU3CLK*↑↓	15	—	—	ns
t_H		RAU3DATA[7:0]↑↓ from RAU3CLK*↑↓	2	—	—	ns
t_{SU}	RAU3PAR	RAU3PAR↑↓ to RAU3CLK*↑↓	15	—	—	ns
t_H		RAU3PAR↑↓ from RAU3CLK*↑↓	2	—	—	ns
t_{SU}	RAU3SERIAL	RAU3SERIAL↑↓ to RAU3CLK*↑↓	5	—	—	ns
t_H		RAU3SERIAL↑↓ from RAU3CLK*↑↓	2	—	—	ns
t_{SU}	TAU3SYNC	TAU3SYNC↑↓ to TAU3CLKIN*↑↓	5	—	—	ns
t_H		TAU3SYNC↑↓ from TAU3CLKIN*↑↓	2	—	—	ns
t_{SU}	TDI	TDI↑↓ to TCLK↑	50	—	—	ns
t_H		TDI↑↓ from TCLK↑	50	—	—	ns
t_{PD}	TDATA[28:1]	From TCLK*[28:1]↑↓ to TDATA[28:1]↑↓	40	—	190	ns
t_{PD}	TAU3DATA[7:0]	From TAU3CLKIN↑ to TAU3DATA[7:0]↑↓	2	—	12	ns
t_{PD}	TAU3PAR	From TAU3CLKIN↑ to TAU3PAR↑↓	2	—	12	ns
t_{PD}	TAU3DATA7	From TAU3CLKOUT↑ to TAU3DATA7↑↓	0	—	3.5	ns
t_{PD}	TDO	From TCLK↓ to TDO↑↓	1.5	—	7	ns

* These clock edges are programable through the microprocessor interface.
† The duty cycle distortion added to the TAU3CLKOUT signal is ≤2 % worst case when measured from 1.5 V in to 1.5 V out with a 2 ns rise time input.

Notes:
↑ represents a low-to-high transition.
↓ represents a high-to-low transition.

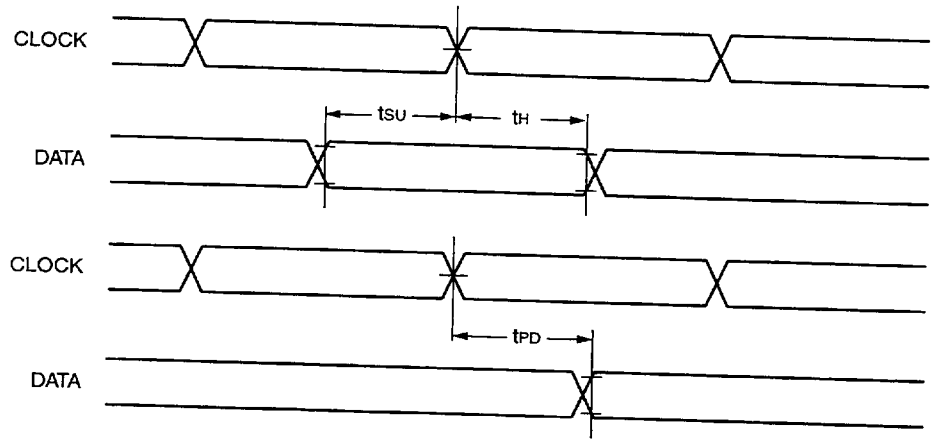

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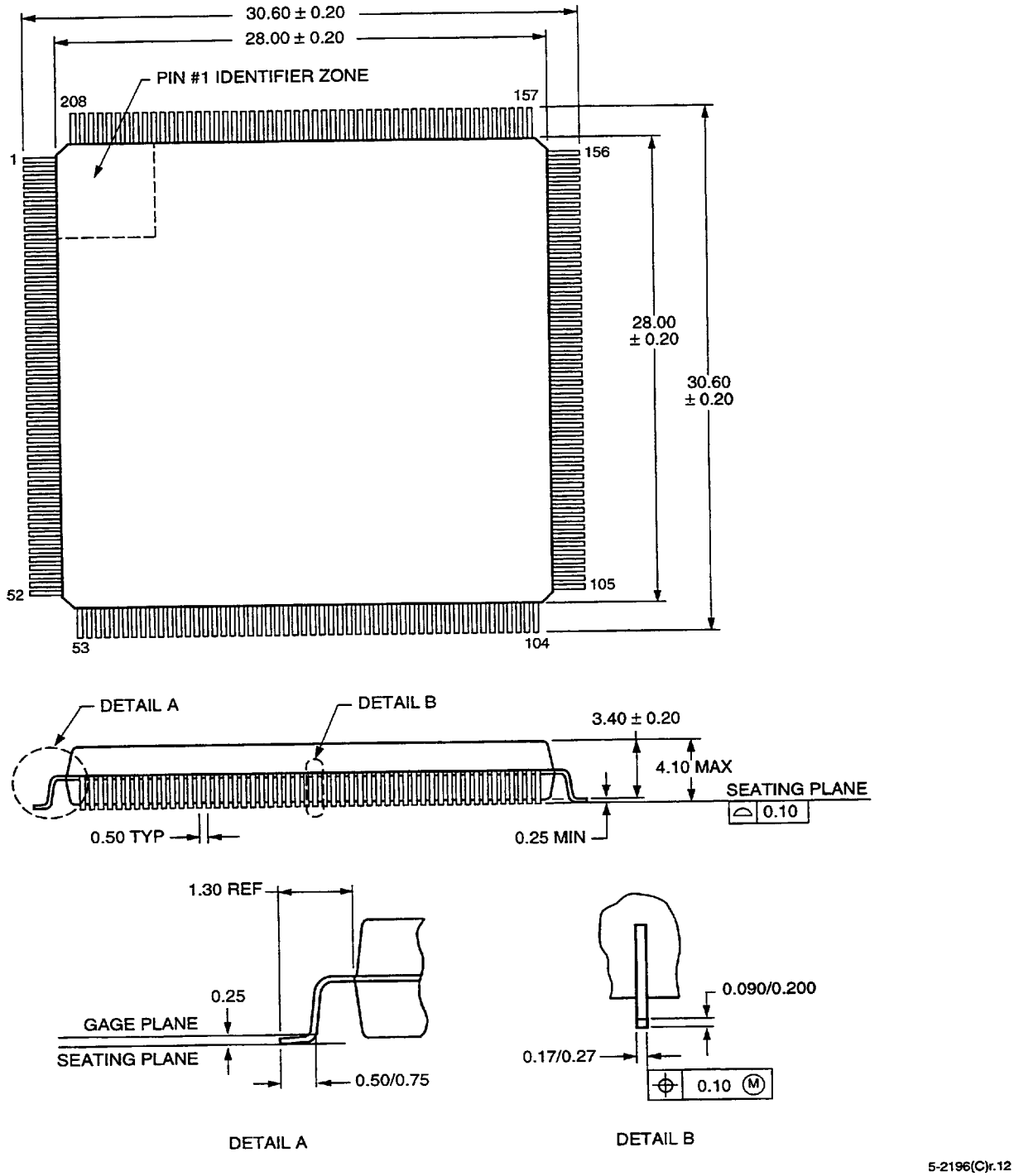
Figure 32. Generic Interface Data Timing

Outline Diagram

208-Pin SQFP

Dimensions are in millimeters.



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Ordering Information

Device Code	Package	Temperature	Comcode (Ordering Number)
TMPR28051 - SL	208-Pin SQFP	–40 °C to +85 °C	107892192

DS97-211TIC Replaces DS97-114TIC to Incorporate the Following Updates

1. Page 7, Figure 2, Device Pinout DS1 Mode, pins 88, 89, and 91.
2. Page 10, Table 1, Pin Descriptions DS1 Mode, pins 88, 89, 91, 92, 94—99.
3. Page 29, Table 10, Device-Level Control, Alarm, and Mask Bits Register Set, Address FE and FF bits 7—0.
4. Page 39, Table 14, Microprocessor Interface I/O Timing Specifications, updated parameters t1, t3, t6—t8, t11—t15, t17—t18.
5. Page 46, Table 19, Generic Interface Data Timing and Figure 16, Generic Interface Data Timing.
6. Page 48, Figure 18, Device Pinout E1 Mode, pins 88, 89, and 91.
7. Page 51, Table 20, Pin Descriptions E1 Mode, pins 88, 89, 91, 92, 94—99.
8. Page 70, Table 28, Device-Level Control, Alarm, and Mask Bits Register Set, Address FE and FF bits 7—0.
9. Page 80, Table 32, Microprocessor Interface I/O Timing Specifications, updated parameters t1, t3, t6—t8, t11—t15, t17—t18.
10. Page 87, Table 37, Generic Interface Data Timing and Figure 32, Generic Interface Data Timing.