TMS28F210
1048576-BIT FLASH MEMORY

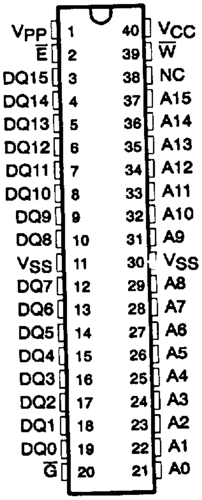
SMJS210B – DECEMBER 1992 – REVISED JUNE 1995

- **Organization . . . 64K × 16 Flash Memory**
- **Pin Compatible With Existing 1-Megabit EPROMs**
- **All Inputs/Outputs TTL Compatible**
- **V_{CC} Tolerance ±10%**
- **Maximum Access/Minimum Cycle Time**

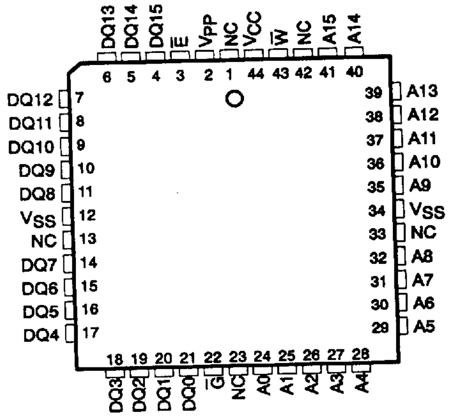
'28F210-10	**100 ns**
'28F210-12	**120 ns**
'28F210-15	**150 ns**
'28F210-17	**170 ns**

- **Industry-Standard Programming Algorithm**
- **PEP4 Version Available With 168-Hour Burn-In and Choice of Operating Temperature Ranges**
- **Chip Erase Before Reprogramming**
- **10000 and 1000 Program/Erase Cycles**
- **Low Power Dissipation (V_{CC} = 5.5 V)**
  - **–Active Write . . . 55 mW**
  - **–Active Read . . . 165 mW**
  - **–Electrical Erase . . . 82.5 mW**
  - **–Standby . . . 0.55 mW (CMOS-Input Levels)**
- **Automotive Temperature Range – 40°C to 125°C**

N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



description

The TMS28F210 is a 1048576-bit, programmable read-only memory that can be electrically bulk erased and reprogrammed. It is available in 10000 and 1000 program/erase endurance cycle versions.

The TMS28F210 flash memory is offered in a dual-in-line plastic package (N suffix) designed for insertion in mounting-hole rows on 15,2 mm (600-mil) center and a 44-lead plastic leaded-chip carrier package using 1,25 mm (50-mil) lead spacing (FN suffix).

The TMS28F210 is characterized for operation in temperature ranges of 0°C to 70°C (NL and FNL suffixes), –40°C to 85°C (NE and FNE suffixes), and –40°C to 125°C (NQ and FNQ suffixes). All packages are offered with 168-hour burn-in (4 suffix).

PIN NOMENCLATURE	
A0–A15	Address Inputs
DQ0–DQ15	Inputs (programming)/Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
NC	No Internal Connection
V_{CC}	5-V Power Supply
V_{SS}	Ground
V_{PP}	12-V Power Supply†
$\overline{W}$	Program

† Only in program mode

PRODUCT PREVIEW

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251–1443

device symbol nomenclature

TMS28F210 -12 C4 FN L 4

PEP4 Burn-In
4 = 168-Hour Burn-In
(blank if no burn-in)

Temperature Range Designator
L = 0°C to 70°C
E = −40°C to 85°C
Q = −40°C to 125°C

Package Designator
N = Plastic Dual-In-Line Package
FN = Plastic Leaded Chip Carrier

Program/Erase Endurance
C4 = 10 000 Cycles
C3 = 1 000 Cycles

Speed Designator
-10 = 100 ns
-12 = 120 ns
-15 = 150 ns
-17 = 170 ns

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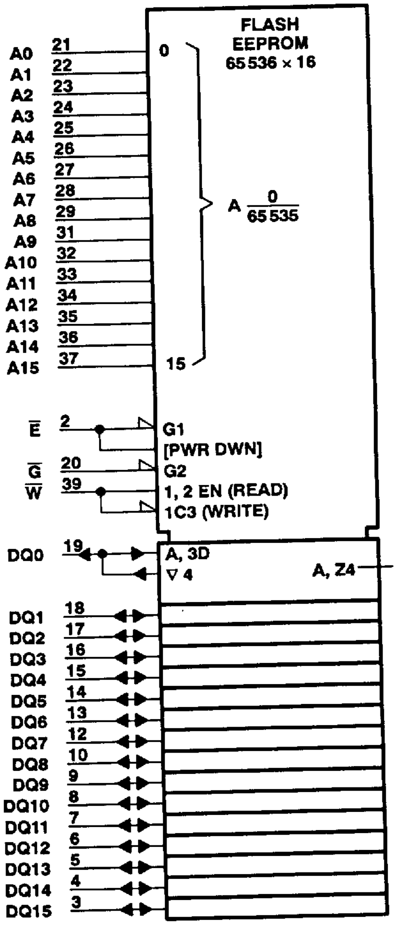
logic symbol[†]



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the N package.

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functional block diagram

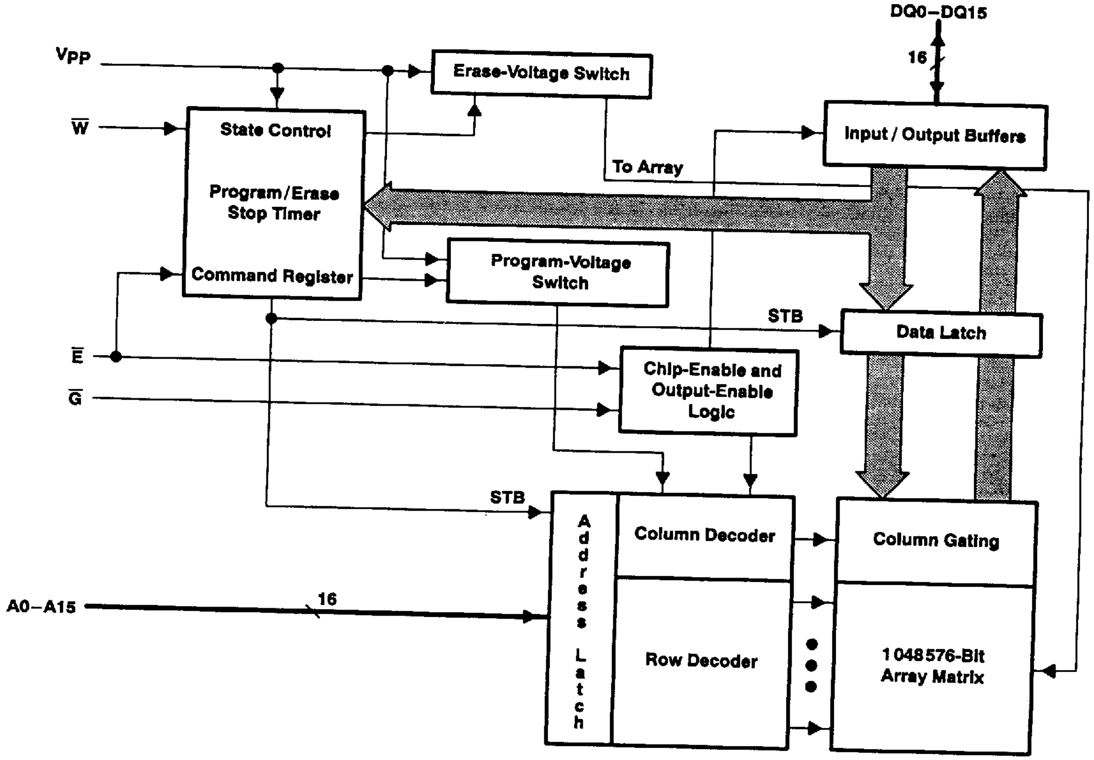

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Table 1. Operation Modes

MODE			FUNCTION†						
		N PACKAGE	V_{PP}‡	$\overline{E}$	$\overline{G}$	A0	A9	$\overline{W}$	DQ0–DQ15
			1	2	20	21	31	39	3–10, 12–19
		FN PACKAGE	2	3	22	24	35	43	21–14, 11–4
Read	Read		V_{PPL}	V_{IL}	V_{IL}	X	X	V_{IH}	Data Out
	Output Disable		V_{PPL}	V_{IL}	V_{IH}	X	X	V_{IH}	Hi-Z
	Standby and Write Inhibit		V_{PPL}	V_{IH}	X	X	X	X	Hi-Z
	Algorithm-Selection Mode		V_{PPL}	V_{IL}	V_{IL}	V_{IL}	V_{ID}	V_{IH}	Mfr Equivalent Code 0097h
						V_{IH}			Device Equivalent Code 00E5h
Read/ Write	Read		V_{PPH}	V_{IL}	V_{IL}	X	X	V_{IH}	Data Out
	Output Disable		V_{PPH}	V_{IL}	V_{IH}	X	X	V_{IH}	Hi-Z
	Standby and Write Inhibit		V_{PPH}	V_{IH}	X	X	X	X	Hi-Z
	Write		V_{PPH}	V_{IL}	V_{IH}	X	X	V_{IL}	Data In

† X can be V_{IL} or V_{IH}.
‡ $V_{PPL} \leq V_{CC} + 2$ V; V_{PPH} is the programming voltage specified for the device. For more details, see the recommended operating conditions.

operation

read/output disable

When the outputs of two or more TMS28F210s are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of other devices. To read the output of the TMS28F210, a low-level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins.

standby and write inhibit

Active I_{CC} current can be reduced from 50 mA to 1 mA by applying a high TTL level on $\overline{E}$ or to 100 μA with a high CMOS level on $\overline{E}$. In this mode, all outputs are in the high-impedance state. The TMS28F210 draws active current when it is deselected during programming, erasure, or program/erase verification. It continues to draw active current until the operation is terminated.

algorithm-selection mode

The algorithm-selection mode provides access to a binary code identifying the correct programming and erase algorithms. This mode is activated when A9 is forced to V_{ID}. Two identifier bytes are accessed by toggling A0. All other addresses must be held low. A0 low selects the manufacturer-equivalent code 0097h, and A0 high selects the device-equivalent code 00E5h, as shown in the algorithm-selection mode table below:

IDENTIFIER¶	PINS§									
	A0	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	HEX
Manufacturer-Equivalent Code	V_{IL}	1	0	0	1	0	1	1	1	0097
Device-Equivalent Code	V_{IH}	1	1	1	0	0	1	0	1	00E5

§ D8–D15 are not shown in the table because the upper 8 data bits read 0.
¶ $\overline{E} = \overline{G} = A1–A8 = A10–A15 = V_{IL}$, $A_9 = V_{ID}$, $V_{PP} = V_{PPL}$

programming and erasure

In the erased state, all bits are at a logic 1. Before erasing the device, all memory bits must be programmed to a logic 0. Afterwards, the entire chip is erased. At this point, the bits, now logic 1s, can be programmed accordingly. Refer to the Fastwrite and Fasterase algorithms for further detail.

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command register

The command register controls the program and erase functions of the TMS28F210. The algorithm-selection mode can be activated using the command register in addition to the previously described method. When V_{PP} is high, the contents of the command register and the function being performed can be changed. The command register is written to when $\overline{E}$ is low and $\overline{W}$ is pulsed low. The address is latched on the leading edge of the pulse, while the data is latched on the trailing edge. Accidental programming or erasure is minimized because two commands must be executed to invoke either operation.

power supply considerations

Each device should have a 0.1-µF ceramic capacitor connected between V_{CC} and V_{SS} to suppress circuit noise. Changes in current drain on V_{PP} require it to have a bypass capacitor as well. Printed circuit traces for both power supplies should be appropriate to handle the current demand.

Table 2. Command Definitions

COMMAND	REQUIRED BUS CYCLES	FIRST BUS CYCLE			SECOND BUS CYCLE		
		OPERATION†	ADDRESS	DATA	OPERATION†	ADDRESS	DATA
Read	1	Write	X	0000h	Read	RA	RD
Algorithm-Selection Mode	3	Write	X	0090h	Read	0000 0001	0097h 00E5h
Set-Up-Erase/Erase	2	Write	X	0020h	Write	X	20h
Erase Verify	2	Write	EA	00A0h	Read	X	EVD
Set-Up-Program/Program	2	Write	X	0040h	Write	PA	PD
Program Verify	2	Write	X	00C0h	Read	X	PVD
Reset	2	Write	X	00FFh	Write	X	00FFh

† Modes of operation are defined in Table 1.

Legend:

EA	Address of memory location to be read during erase verify
RA	Address of memory location to be read
PA	Address of memory location to be programmed. Address is latched on the falling edge of $\overline{W}$.
RD	Data read from location RA during the read operation
EVD	Data read from location EA during erase verify
PD	Data to be programmed at location PA. Data is latched on the rising edge of $\overline{W}$.
PVD	Data read from location PA during program verify

command definitions

read command

Memory contents can be accessed while V_{PP} is high or low. When V_{PP} is high, writing 0000h into the command register invokes the read operation. When the device is powered up, the default contents of the command register are 0000h and the read operation is enabled. The read operation remains enabled until a different valid command is written to the command register.

algorithm-selection-mode command

The algorithm-selection mode is activated by writing 0090h into the command register. The manufacturer equivalent code (0097h) is identified by the value read from address location 0000h, and the device equivalent code (00E5h) is identified by the value read from address location 0001h.

set-up-program/program commands

The programming algorithm initiates with $\overline{E} = V_{IL}$, $\overline{W} = V_{IL}$, $\overline{G} = V_{IH}$, $V_{PP} = V_{PPH}$, and $V_{CC} = 5$ V. To enter the programming mode, write the set-up-program command, 0040h, into the command register. The programming operation is invoked by the next write-enable pulse. Addresses are latched internally on the falling edge of $\overline{W}$, and data is latched internally on the rising edge of $\overline{W}$. The programming operation begins on the rising edge of $\overline{W}$ and ends on the rising edge of the next $\overline{W}$ pulse. The program operation requires 10 µs for completion before the program-verify command, 00C0h, can be loaded.

Maximum program timing is controlled by the internal stop timer. When the stop timer terminates the program operation, the device enters an inactive state and remains inactive until a valid program-verify, read, or reset command is received.

program-verify command

The TMS28F210 can be programmed sequentially or randomly because it is programmed one word at a time. Each word must be verified after it is programmed. The program-verify operation prepares the device to verify the most recently programmed word. To invoke the program-verify operation, 00C0h must be written into the command register. The program-verify operation ends on the rising edge of $\overline{W}$.

While verifying a word, the TMS28F210 applies an internal margin voltage to the designated word. If the true data and programmed data match, programming continues to the next designated word location; otherwise, the word must be reprogrammed. Figure 1 shows how commands and bus operations are combined for word programming.

set-up-erase/erase commands

The erase algorithm initiates with $\overline{E} = V_{IL}$, $\overline{W} = V_{IL}$, $\overline{G} = V_{IH}$, $V_{PP} = V_{PPH}$, and $V_{CC} = 5$ V. To enter the erase mode, write the set-up-erase command, 0020h, into the command register. After the TMS28F210 is in the erase mode, writing a second erase command, 0020h, into the command register invokes the erase operation. The erase operation begins on the rising edge of $\overline{W}$ and ends on the rising edge of the next $\overline{W}$. The erase operation requires 10 ms to complete before the erase-verify command, 00A0h, can be loaded.

Maximum erase timing is controlled by the internal stop timer. When the stop timer terminates the erase operation, the device enters an inactive state and remains inactive until a valid erase-verify, read, or reset command is received.

erase-verify command

All words must be verified following an erase operation. After the erase operation is complete, an erased word can be verified by writing the erase-verify command, 00A0h, into the command register. This command causes the device to exit the erase mode on the rising edge of $\overline{W}$. The address of the word to be verified is latched on the falling edge of $\overline{W}$. The erase-verify operation remains enabled until a valid command is written to the command register.

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erase-verify command (continued)

To determine whether or not all the words have been erased, the TMS28F210 applies a margin voltage to each word. If FFFFh is read from the word, all bits in the designated word have been erased. The erase-verify operation continues until all of the words have been verified. If FFFFh is not read from a word, an additional erase operation needs to be executed. Figure 2 shows the combination of commands and bus operations for electrically erasing the TMS28F210.

reset command

To reset the TMS28F210 after set-up-erase command or set-up-program command operations without changing the contents in memory, write 00FFh into the command register two consecutive times. After executing the reset command, a valid command must be written into the command register to change to a new state.

Fastwrite algorithm

The TMS28F210 is programmed using the Texas Instruments Fastwrite algorithm shown in Figure 1. This algorithm programs in a nominal time of two seconds.

Fasterase algorithm

The TMS28F210 is erased using the Texas Instruments Fasterase algorithm shown in Figure 2. The memory array needs to be completely programmed (using the Fastwrite algorithm) before erasure begins. Erasure typically occurs in one second.

parallel erasure

To reduce total erase time, several devices can be erased in parallel. Since each Flash EEPROM can erase at a different rate, every device must be verified separately after each erase pulse. After a given device has been successfully erased, the erase command should not be issued to this device again. All devices that complete erasure should be masked until the parallel erasure process is finished (see Figure 3).

Examples of how to mask a device during parallel erase include driving the $\overline{E}$ pin high, writing the read command (0000h) to the device when the others receive a set-up-erase or erase command, or disconnecting it from all electrical signals with relays or other types of switches.

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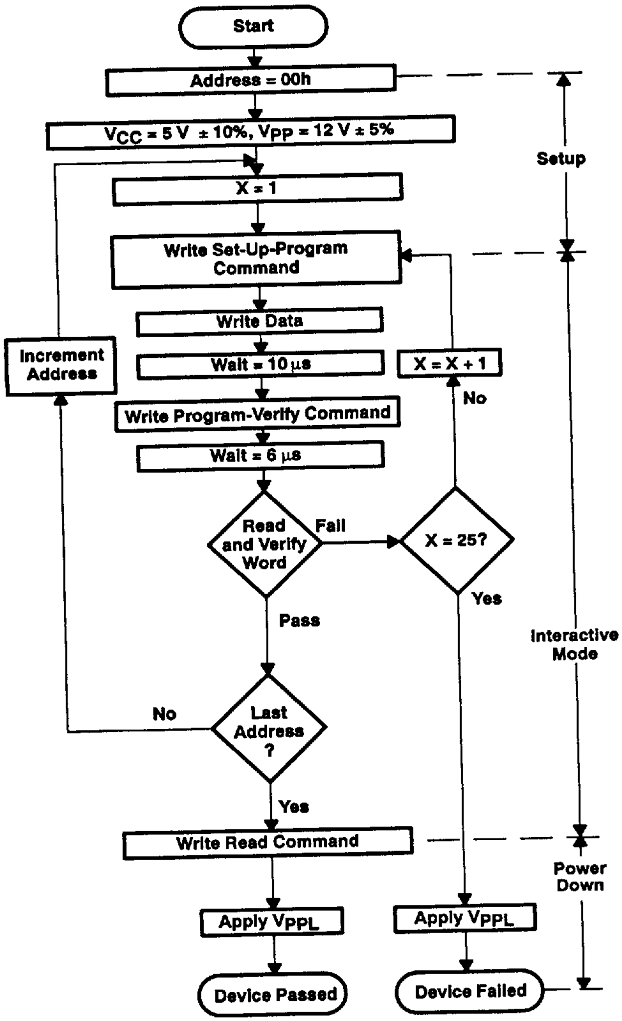

Bus Operation	Command	Comments
Initialize Address		
Standby		Wait for V_{PP} to ramp to V_{PPH} (see Note A) Initialize pulse count
Write	Set-Up-Program	Data = 0040h
Write	Write Data	Valid address / data
Standby		Wait = 10 µs
Write	Program-Verify	Data = 00C0h; ends program operation
Standby		Wait = 6 µs
Read		Read word to verify programming; compare output to expected output
Write	Read	Data = 0000h; resets register for read operations
Standby		Wait for V_{PP} to ramp to V_{PPL} (see Note B)

NOTES: A. Refer to the recommended operating conditions for the value of V_{PPH}.
B. Refer to the recommended operating conditions for the value of V_{PPL}.

Figure 1. Programming Flowchart: Fastwrite Algorithm

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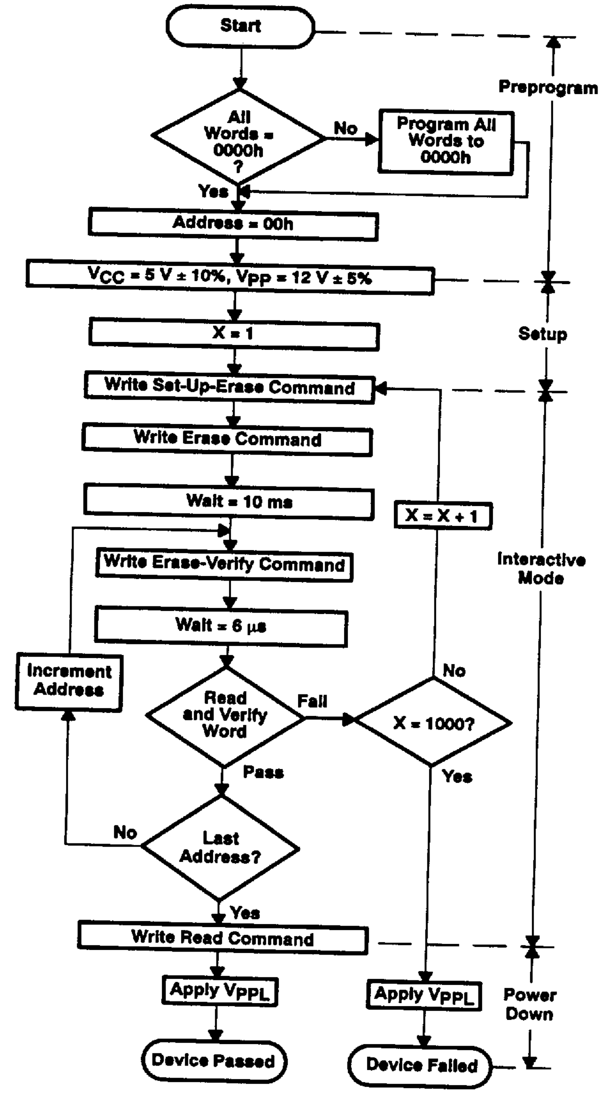
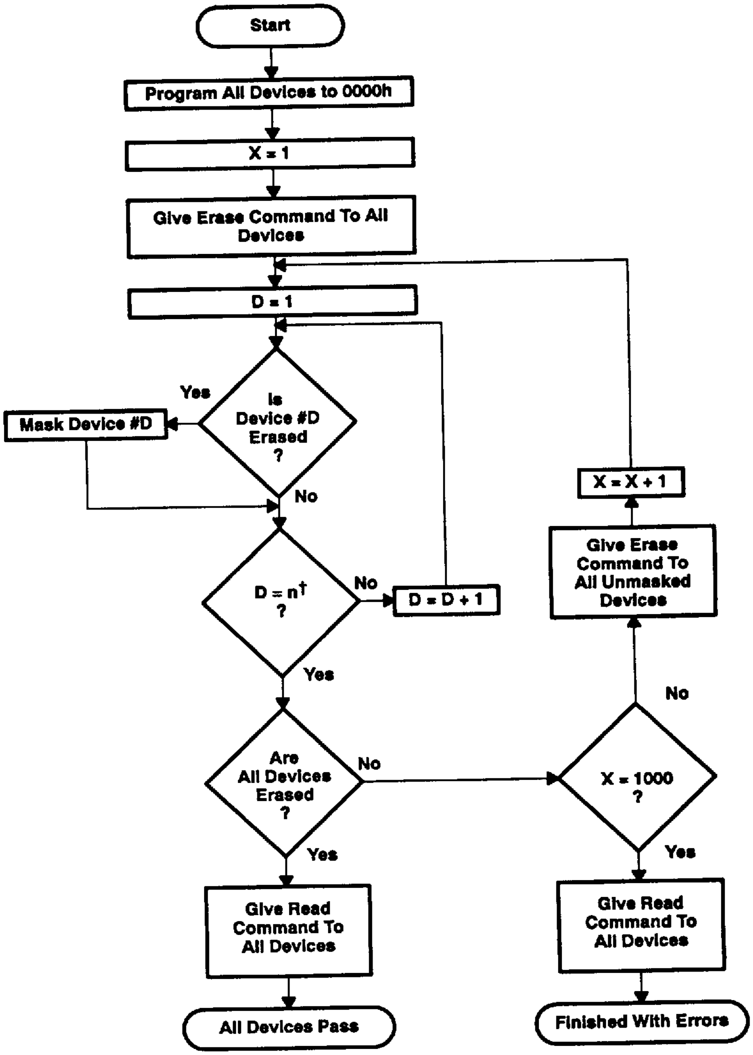


Bus Operation	Command	Comments
		Entire memory must = 0000h before erasure Use Fastwrite programming algorithm
		Initialize addresses
Standby		Wait for Vpp to ramp to V_{PPH} (see Note A)
		Initialize pulse count
Write	Set-Up-Erase	Data = 0020h
Write	Erase	Data = 0020h
Standby		Wait = 10 ms
Write	Erase Verify	Addr = Word to verify; data = 00A0h; ends the erase operation
Standby		Wait = 6 µs
Read		Read word to verify erasure; compare output to FFFFh
Write	Read	Data = 0000h; resets register for read operations
Standby		Wait for Vpp to ramp to V_{PPL} (see Note B)

NOTES: A. Refer to the recommended operating conditions for the value of V_{PPH}.
B. Refer to the recommended operating conditions for the value of V_{PPL}.

Figure 2. Flash-Erase Flowchart: Fasterase Algorithm



† n = number of devices being erased

Figure 3. Parallel-Erase Flow Diagram

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)	−0.6 V to 7 V
Programming supply voltage range, V_{PP}	−0.6 V to 14 V
Input voltage range (see Note 2): All inputs except A9	−0.6 V to V_{CC} + 1 V
A9	−0.6 V to 13.5 V
Output voltage range (see Note 3)	−0.6 V to V_{CC} + 1 V
Operating free-air temperature range during read/erase/program, T_A	
NL, FNL	0°C to 70°C
NE, FNE	– 40°C to 85°C
NQ, FNQ	– 40° C to 125°C
Storage temperature range, T_{stg}	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltage values are with respect to V_{SS}.
2. The voltage on any input can undershoot to −2 V for periods less than 20 ns.
3. The voltage on any output can overshoot to 7 V for periods less than 20 ns.

recommended operating conditions

			MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage	During write/read/flash erase	4.5	5	5.5	V
V_{PP}	Programming supply voltage	During read only (V_{PPL})	0		V_{CC}+2	V
		During write/read/flash erase (V_{PPH})	11.4	12	12.6	V
V_{ID}	Voltage level on A9 for algorithm-selection mode		11.5		13	V
V_{IH}	High-level dc input voltage	TTL	2		V_{CC}+0.5	V
		CMOS	V_{CC} – 0.5		V_{CC}+0.5	
V_{IL}	Low-level dc input voltage	TTL	−0.5		0.8	V
		CMOS	GND – 0.2		GND+0.2	
T_A	Operating free-air temperature	NL, FNL suffix	0		70	°C
		NE, FNE suffix	– 40		85	
		NQ, FNQ suffix	– 40		125	

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	TTL	$I_{OH} = -2.5$ mA	2.4		V
		CMOS	$I_{OH} = -100\ \mu A$	$V_{CC} - 0.4$		
V_{OL}	Low-level output voltage	TTL	$I_{OL} = 5.8$ mA		0.45	V
		CMOS	$I_{OL} = 100\ \mu A$		0.1	
I_I	Input current (leakage)	All except A9	$V_I = 0$ V to 5.5 V		±1	µA
		A9	$V_I = 0$ V to 13 V		± 200	
I_O	Output current (leakage)		$V_O = 0$ V to V_{CC}		±10	µA
I_{ID}	A9 algorithm-selection-mode current		A9 = V_{ID} max		TBD	mA
I_{PP1}	V_{PP} supply current (read/standby)		$V_{PP} = V_{PPH}$, Read mode		200	µA
			$V_{PP} = V_{PPL}$		±10	µA
I_{PP2}	V_{PP} supply current (during program pulse) (see Note 4)		$V_{PP} = V_{PPH}$		50	mA
I_{PP3}	V_{PP} supply current (during flash erase) (see Note 4)		$V_{PP} = V_{PPH}$		50	mA
I_{PP4}	V_{PP} supply current (during program/erase verify) (see Note 4)		$V_{PP} = V_{PPH}$		5.0	mA
I_{CCS}	V_{CC} supply current (standby)	TTL-input level	$V_{CC} = 5.5$ V, $\overline{E} = V_{IH}$		1	mA
		CMOS-input level	$V_{CC} = 5.5$ V, $\overline{E} = V_{CC}$		100	µA
I_{CC1}	V_{CC} supply current (active read)		$V_{CC} = 5.5$ V, $\overline{E} = V_{IL}$, f = 6 MHz, Outputs open		50	mA
I_{CC2}	V_{CC} average supply current (active write) (see Note 4)		$V_{CC} = 5.5$ V, $\overline{E} = V_{IL}$, Programming in progress		10	mA
I_{CC3}	V_{CC} average supply current (flash erase) (see Note 4)		$V_{CC} = 5.5$ V, $\overline{E} = V_{IL}$, Erasure in progress		15	mA
I_{CC4}	V_{CC} average supply current (program/erase verify) (see Note 4)		$V_{CC} = 5.5$ V, $\overline{E} = V_{IL}$, $V_{PP} = V_{PPH}$, Program/erase verify in progress		15	mA

NOTE 4: Not 100% tested; characterization data available

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz†

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
C_I	Input capacitance	$V_I = 0$ V, f = 1 MHz		6	pF
C_O	Output capacitance	$V_O = 0$ V, f = 1 MHz		12	pF

† Capacitance measurements are made on sample basis only.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature

		TEST CONDITIONS	ALTERNATE SYMBOL	'28F210-10		'28F210-12		'28F210-15		'28F210-17		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL load, Input $t_r \le 20$ ns, Input $t_f \le 20$ ns	t_{AVQV}		100		120		150		170	ns
$t_{a(E)}$	Access time from $\overline{E}$		t_{ELQV}		100		120		150		170	ns
$t_{a(G)}$	Access time from $\overline{G}$		t_{GLQV}		45		50		55		60	ns
$t_{c(R)}$	Cycle time, read		t_{AVAV}	100		120		150		170		ns
$t_{d(E)}$	Delay time, chip enable low to low-Z output		t_{ELQX}	0		0		0		0		ns
$t_{d(G)}$	Delay time, $\overline{G}$ low to low-Z output		t_{GLQX}	0		0		0		0		ns
$t_{dis(E)}$	Chip disable to Hi-Z output		t_{EHQZ}	0	55	0	55	0	55	0	55	ns
$t_{dis(G)}$	Hold time, output enable to Hi-Z output		t_{GHQZ}	0	30	0	30	0	35	0	35	ns
$t_{h(D)}$	Hold time, data valid from address, $\overline{E}$, or $\overline{G}$†		t_{AXQX}	0		0		0		0		ns
$t_{rec(W)}$	Write recovery time before read		t_{WHGL}	6		6		6		6		µs

† Whichever occurs first

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timing requirements—write/erase/program operations

		ALTERNATE SYMBOL	'28F210-10			'28F210-12			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
$t_{c(W)}$	Cycle time, write using $\overline{W}$	t_{AVAV}	100			120			ns
$t_{c(W)PR}$	Cycle time, programming operation	t_{WHWH1}	10			10			µs
$t_{c(W)ER}$	Cycle time, erase operation	t_{WHWH2}	9.5	10		9.5	10		ms
$t_{h(A)}$	Hold time, address	t_{WLAX}	55			60			ns
$t_{h(E)}$	Hold time, $\overline{E}$	t_{WHEH}	0			0			ns
$t_{h(WHD)}$	Hold time, data valid after $\overline{W}$ high	t_{WHDX}	10			10			ns
$t_{su(A)}$	Setup time, address	t_{AVWL}	0			0			ns
$t_{su(D)}$	Setup time, data	t_{DVWH}	50			50			ns
$t_{su(E)}$	Setup time, $\overline{E}$ before $\overline{W}$	t_{ELWL}	20			20			ns
$t_{su(EHVPP)}$	Setup time, $\overline{E}$ high to V_{PP} ramp	t_{EHVP}	100			100			ns
$t_{su(VPPEL)}$	Setup time, V_{PP} to $\overline{E}$ low	t_{VPEL}	1			1			µs
$t_{rec(W)}$	Recovery time, $\overline{W}$ before read	t_{WHGL}	6			6			µs
$t_{rec(R)}$	Recovery time, read before $\overline{W}$	t_{GHWL}	0			0			µs
$t_{w(W)}$	Pulse duration, $\overline{W}$ (see Note 5)	t_{WLWH}	60			60			ns
$t_{w(WH)}$	Pulse duration, $\overline{W}$ high	t_{WHWL}	20			20			ns
$t_{r(VPP)}$	Rise time, V_{PP}	t_{VPPR}	1			1			µs
$t_{f(VPP)}$	Fall time, V_{PP}	t_{VPPF}	1			1			µs

		ALTERNATE SYMBOL	'28F210-15			'28F210-17			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
$t_{c(W)}$	Cycle time, write using $\overline{W}$	t_{AVAV}	150			170			ns
$t_{c(W)PR}$	Cycle time, programming operation	t_{WHWH1}	10			10			µs
$t_{c(W)ER}$	Cycle time, erase operation	t_{WHWH2}	9.5	10		9.5	10		ms
$t_{h(A)}$	Hold time, address	t_{WLAX}	60			70			ns
$t_{h(E)}$	Hold time, $\overline{E}$	t_{WHEH}	0			0			ns
$t_{h(WHD)}$	Hold time, data valid after $\overline{W}$ high	t_{WHDX}	10			10			ns
$t_{su(A)}$	Setup time, address	t_{AVWL}	0			0			ns
$t_{su(D)}$	Setup time, data	t_{DVWH}	50			50			ns
$t_{su(E)}$	Setup time, $\overline{E}$ before $\overline{W}$	t_{ELWL}	20			20			ns
$t_{su(EHVPP)}$	Setup time, $\overline{E}$ high to V_{PP} ramp	t_{EHVP}	100			100			ns
$t_{su(VPPEL)}$	Setup time, V_{PP} to $\overline{E}$ low	t_{VPEL}	1			1			µs
$t_{rec(W)}$	Recovery time, $\overline{W}$ before read	t_{WHGL}	6			6			µs
$t_{rec(R)}$	Recovery time, read before $\overline{W}$	t_{GHWL}	0			0			µs
$t_{w(W)}$	Pulse duration, $\overline{W}$ (see Note 5)	t_{WLWH}	60			60			ns
$t_{w(WH)}$	Pulse duration, $\overline{W}$ high	t_{WHWL}	20			20			ns
$t_{r(VPP)}$	Rise time, V_{PP}	t_{VPPR}	1			1			µs
$t_{f(VPP)}$	Fall time, V_{PP}	t_{VPPF}	1			1			µs

NOTE 5: Rise/fall time ≤ 10 ns.

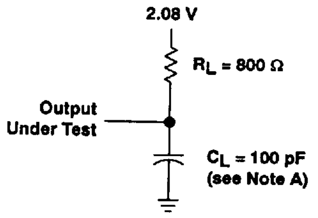
PRODUCT PREVIEW

timing requirements—alternative $\overline{E}$-controlled writes

		ALTERNATE SYMBOL	'28F210-10		'28F210-12		'28F210-15		'28F210-17		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(W)}$	Cycle time, write using $\overline{E}$	t_{AVAV}	100		120		150		170		ns
$t_{c(E)PR}$	Cycle time, programming operation	t_{EHEH}	10		10		10		10		µs
$t_{h(EA)}$	Hold time, address	t_{ELAX}	75		80		80		90		ns
$t_{h(ED)}$	Hold time, data	t_{EHDX}	10		10		10		10		ns
$t_{h(W)}$	Hold time, $\overline{W}$	t_{EHWH}	0		0		0		0		ns
$t_{su(A)}$	Setup time, address	t_{AVEL}	0		0		0		0		ns
$t_{su(D)}$	Setup time, data	t_{DVEH}	50		50		50		50		ns
$t_{su(W)}$	Setup time, $\overline{W}$ before $\overline{E}$	t_{WLEL}	0		0		0		0		ns
$t_{su(VPPEL)}$	Setup time, V_{PP} to $\overline{E}$ low	t_{VPEL}	1		1		1		1		µs
$t_{rec(E)R}$	Recovery time, write using $\overline{E}$ before read	t_{EHGL}	6		6		6		6		µs
$t_{rec(E)W}$	Recovery time, read before write using $\overline{E}$	t_{GHEL}	0		0		0		0		µs
$t_{w(E)}$	Pulse duration, write using $\overline{E}$	t_{ELEH}	70		70		70		80		ns
$t_{w(EH)}$	Pulse duration, write, $\overline{E}$ high	t_{EHEL}	20		20		20		20		ns

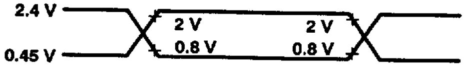
PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

NOTE A: C_L includes probe and fixture capacitance.



VOLTAGE WAVEFORMS

Figure 4. Load Circuit and Voltage Waveforms

AC testing inputs are driven at 2.4 V for logic high and 0.45 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low on both inputs and outputs. Each device should have a 0.1-µF ceramic capacitor connected between V_{CC} and V_{SS} as close as possible to the device pins.

PARAMETER MEASUREMENT INFORMATION

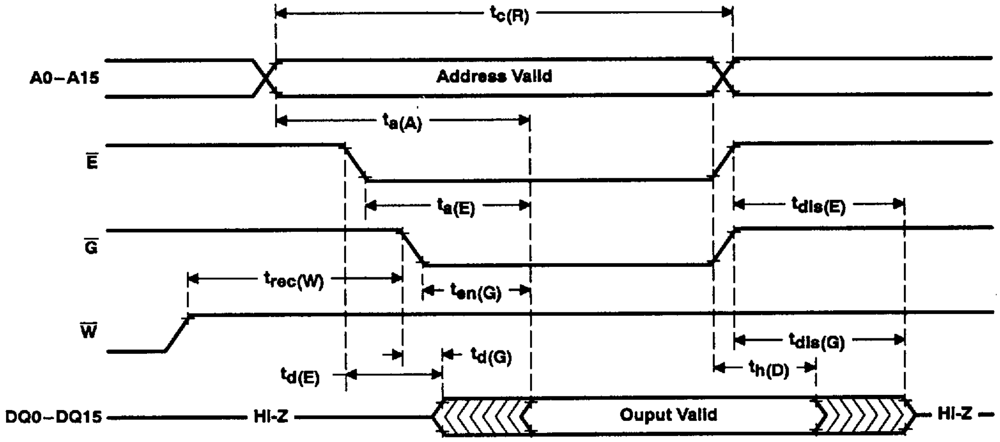


Figure 5. Read-Cycle Timing

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

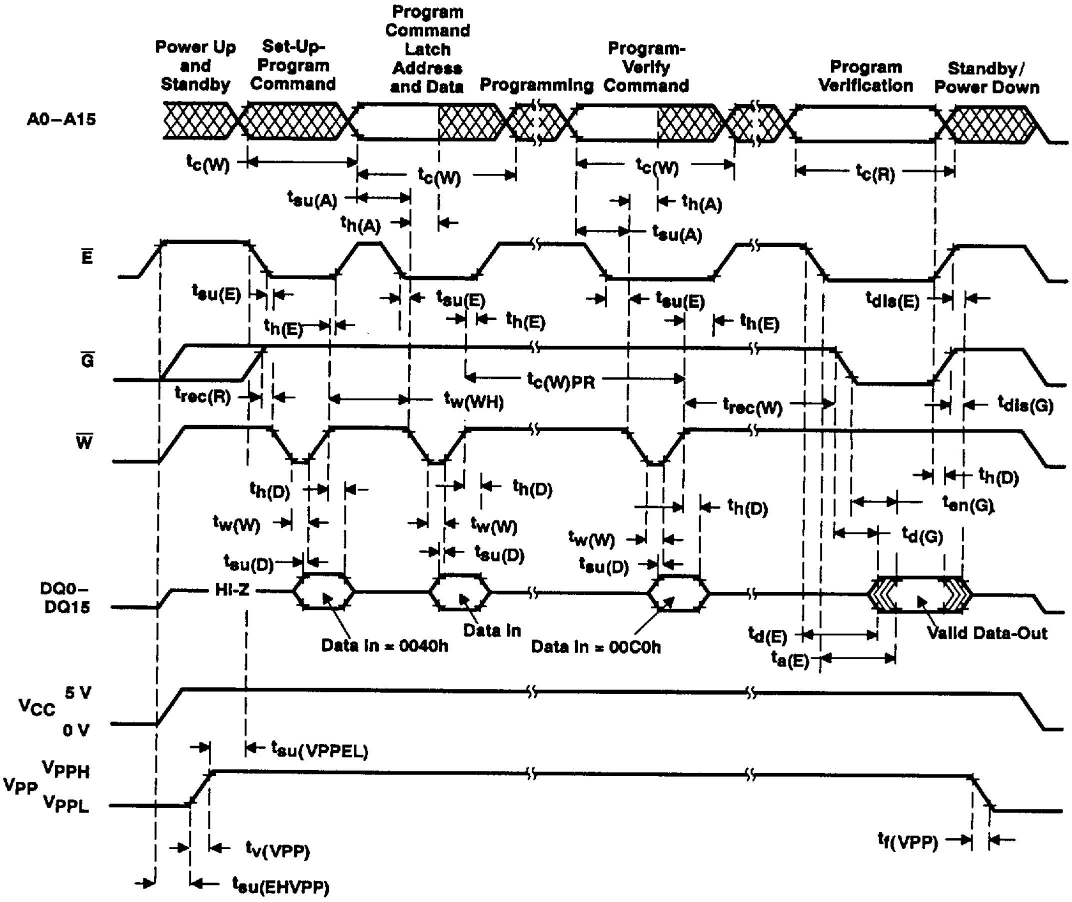


Figure 6. Write-Cycle Timing

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

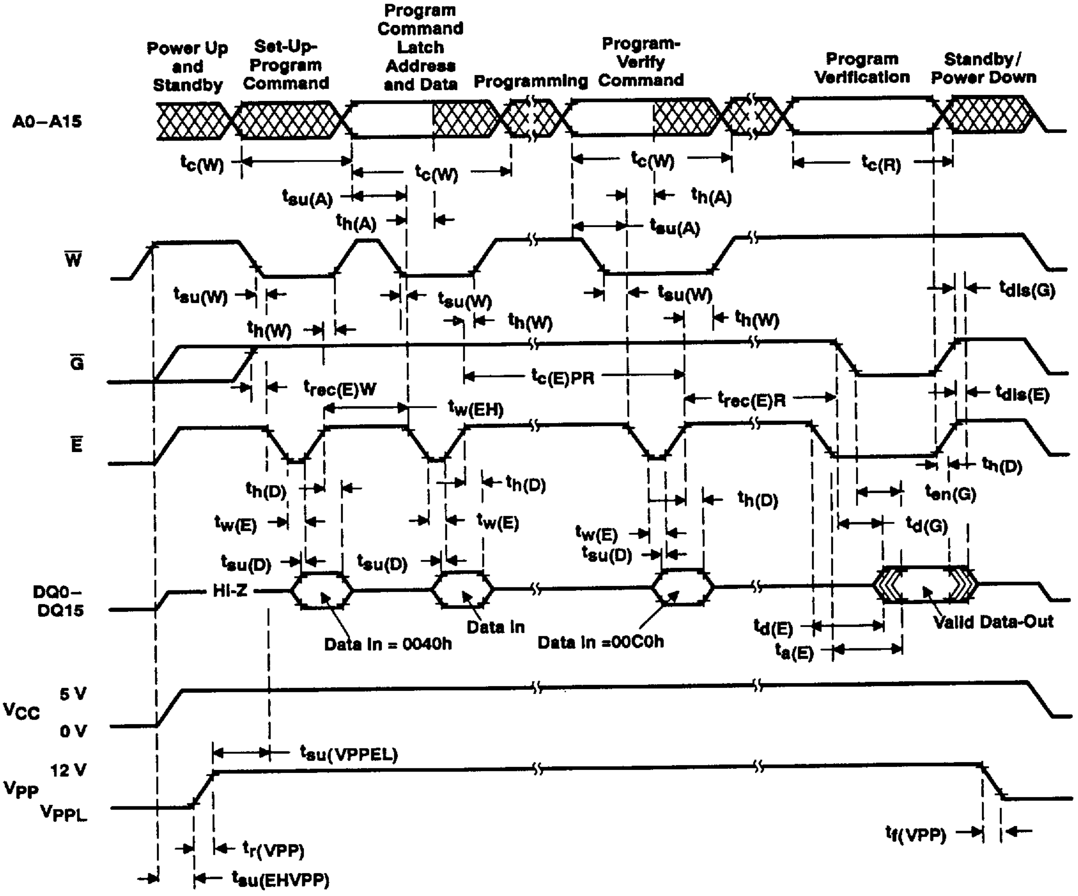


Figure 7. Write-Cycle (Alternative $\overline{E}$-Controlled Writes) Timing

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

PRODUCT PREVIEW

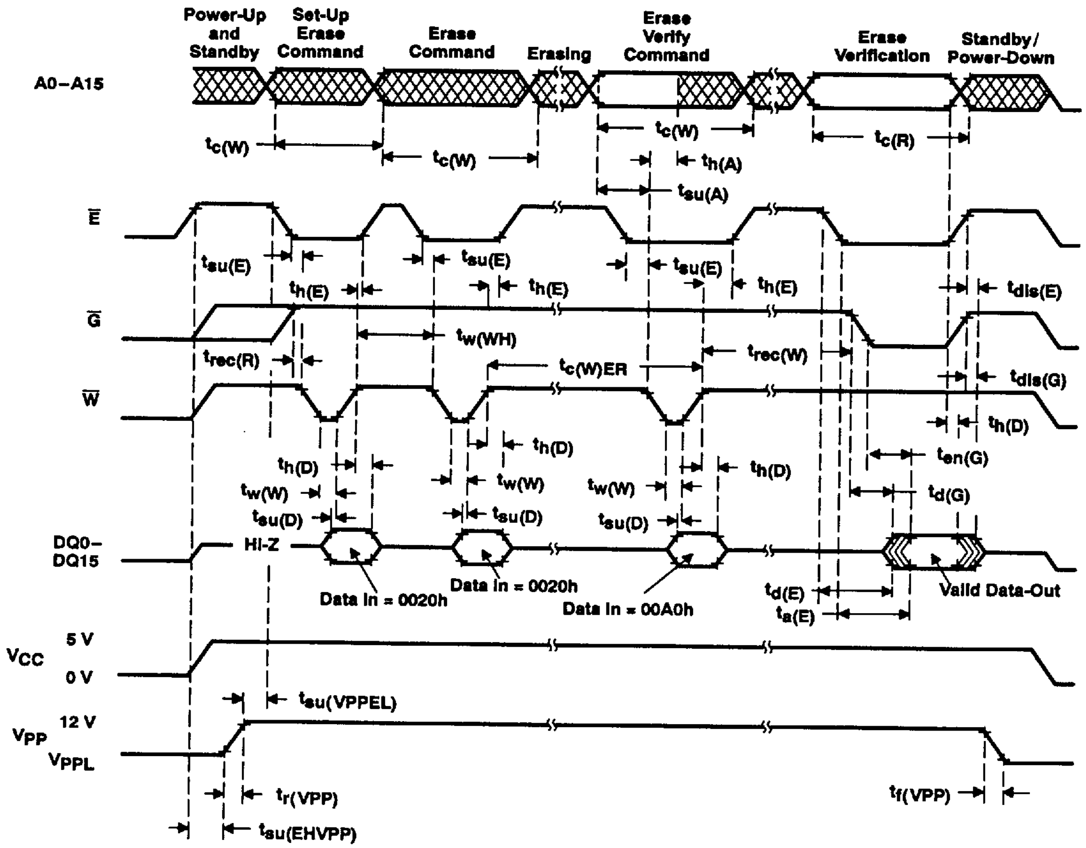


Figure 8. Flash-Erase-Cycle Timing