REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
F	Figure 1; changed case outline M to be available in either a single or dual cavity package. Added vendor cage code 0EU86 for device types 05 through 10. -sld	99-04-22	K. A. Cottongim
G	Added device types 11 through 16.	99-08-18	Ray Monnin

REV																				
SHEET																				
REV	G	G	G	G	G	G	G	G	G	G	G	G								
SHEET	15	16	17	18	20	21	22	23	24	25	26	27								

REV STATUS OF SHEETS	REV	G	G	G	G	G	G	G	G	G	G	G	G	G	G
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Gary Zahn

CHECKED BY
Michael C. Jones

APPROVED BY
Kendall A. Cottongim

DRAWING APPROVAL DATE
95-11-13

REVISION LEVEL
G

DEFENSE SUPPLY CENTER COLUMBUS
P. O. BOX 3990
COLUMBUS, OHIO 43216-5000

MICROCIRCUIT, HYBRID, MEMORY, DIGITAL, 512K x 32-BIT, STATIC RANDOM ACCESS MEMORY, CMOS

SIZE	CAGE CODE	
A	**67268**	**5962-94611**

SHEET 1 OF 27

DSCC FORM 2233
APR 97

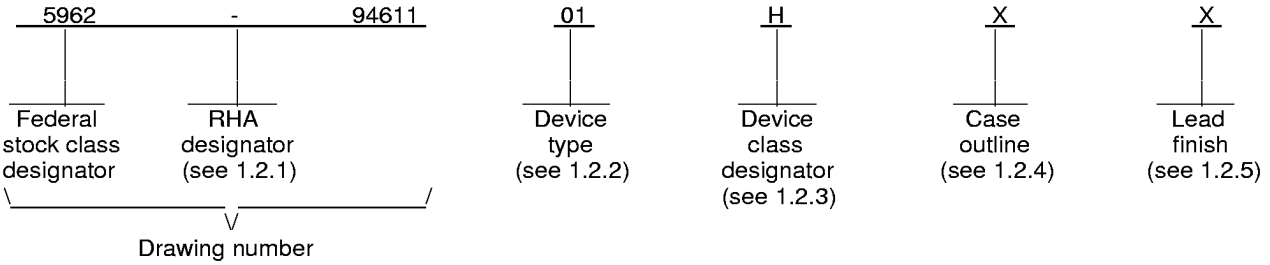
5962-E389-99

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents five product assurance classes, class D (lowest reliability), class E, (exceptions), class G (lowest high reliability), class H (high reliability), and class K, (highest reliability) and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of radiation hardness assurance levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. Device classes H and K RHA marked devices shall meet the MIL-PRF-38534 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type 1/	Generic number	Circuit function	Access time
01	WS512K32-120Q	512K X 32-BIT SRAM	120 ns
02	WS512K32-100Q	512K X 32-BIT SRAM	100 ns
03	WS512K32-85Q	512K X 32-BIT SRAM	85 ns
04	WS512K32-70Q	512K X 32-BIT SRAM	70 ns
05	ACT-S512K32N-055Q, WS512K32-55Q, AS8S512K32Q-55L/Q	512K X 32-BIT SRAM	55 ns
06	ACT-S512K32N-045Q, WS512K32-45Q, AS8S512K32Q-45L/Q	512K X 32-BIT SRAM	45 ns
07	ACT-S512K32N-035Q, WS512K32-35Q, AS8S512K32Q-35L/Q	512K X 32-BIT SRAM	35 ns
08	ACT-S512K32N-025Q, WS512K32-25Q, AS8S512K32Q-25L/Q	512K X 32-BIT SRAM	25 ns
09	ACT-S512K32N-020Q, WS512K32-20Q, AS8S512K32Q-20L/Q	512K X 32-BIT SRAM	20 ns
10	ACT-S512K32N-017Q, WS512K32-17Q, AS8S512K32Q-17L/Q	512K X 32-BIT SRAM	17 ns
11	AS8S512K32Q-55/Q, WS512K32D-55Q	512K X 32-BIT SRAM	55 ns
12	AS8S512K32Q-45/Q, WS512K32D-45Q	512K X 32-BIT SRAM	45 ns
13	AS8S512K32Q-35/Q, WS512K32D-35Q	512K X 32-BIT SRAM	35 ns
14	AS8S512K32Q-25/Q, WS512K32D-25Q	512K X 32-BIT SRAM	25 ns
15	AS8S512K32Q-20/Q, WS512K32D-20Q	512K X 32-BIT SRAM	20 ns
16	AS8S512K32Q-17/Q, WS512K32D-17Q	512K X 32-BIT SRAM	17 ns

1.2.3 Device class designator. This device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device performance documentation
D, E, G, H, or K	Certification and qualification to MIL-PRF-38534

1/ Device types 11 through 16 are not tested to data retention supply voltage (V_{DR}) and data retention current (I_{CCDR1}). See table I.

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
M	See figure 1	68	Co-fired ceramic, single/dual cavity, quad flatpack
T	See figure 1	66	Hex-in-line, single cavity, with standoffs
U	See figure 1	66	Hex-in-line, single cavity, with standoffs
X	See figure 1	66	Hex-in-line, single cavity, with standoffs
Y	See figure 1	68	Ceramic, quad flatpack, single cavity

1.2.5 Lead finish. The lead finish shall be as specified in MIL-PRF-38534.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
Signal voltage range (V_g)	-0.5 V dc to V_{CC} +0.5 V dc
Power dissipation (P_D):	
Device types 01-04	2.2 W
Device types 05, 06, 11, and 12	3.2 W
Device types 07, 08, 13, and 14	3.6 W
Device types 09, 10, 15, and 16	4.4 W
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Junction temperature (T_J)	+150°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Input low voltage range (V_{IL})	-0.3 V dc to +0.8 V dc
Input high voltage range (V_{IH})	+2.2 V dc to V_{CC} +0.3 V dc
Output low voltage, maximum (V_{OL})	+0.4 V dc
Output high voltage, minimum (V_{OH})	+2.4 V dc
Ambient operating temperature range (T_A)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38534 - Hybrid Microcircuits, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Interface Standard For Microcircuit Case Outlines.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item performance requirements for device classes D, E, G, H, and K shall be in accordance with MIL-PRF-38534. Compliance with MIL-PRF-38534 may include the performance of all tests herein or as designated in the device manufacturer's Quality Management (QM) plan or as designated for the applicable device class. Therefore, the tests and inspections herein may not be performed for the applicable device class (see MIL-PRF-38534). Furthermore, the manufacturers may take exceptions or use alternate methods to the tests and inspections herein and not perform them. However, the performance requirements as defined in MIL-PRF-38534 shall be met for the applicable device class.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38534 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3.

3.2.4 Timing diagram(s). The timing diagram(s) shall be as specified on figures 4 and 5.

3.2.5 Block diagram. The block diagram shall be as specified on figure 6.

3.2.6 Output load circuit. The output load circuit shall be as specified on figure 7.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full specified operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking of device(s). Marking of device(s) shall be in accordance with MIL-PRF-38534. The device shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's vendor similar PIN may also be marked as listed in MIL-HDBK-103 and QML-38534.

3.6 Data. In addition to the general performance requirements of MIL-PRF-38534, the manufacturer of the device described herein shall maintain the electrical test data (variables format) from the initial quality conformance inspection group A lot sample, for each device type listed herein. Also, the data should include a summary of all parameters manually tested, and for those which, if any, are guaranteed. This data shall be maintained under document revision level control by the manufacturer and be made available to the preparing activity (DSCC-VA) upon request.

3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to supply to this drawing. The certificate of compliance (original copy) submitted to DSCC-VA shall affirm that the manufacturer's product meets the performance requirements of MIL-PRF-38534 and herein.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38534 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V dc +4.5 V dc $\le V_{CC} \le$ +5.5 V dc unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
DC parameters							
Operating supply current	I_{CC}	$\overline{CS} = V_{IL}$, $\overline{OE} = V_{IH}$, V_{CC} = 5.5 V dc 2/					
		f = 5 MHz	1,2,3	01,02		200	mA
		f = 5 MHz		03,04		200	
		f = 5 MHz		05-10, 11-16		540	
		f = 18.2 MHz		05,11		550	
		f = 22.2 MHz		06,12		570	
		f = 28.6 MHz		07,13		570	
		f = 40 MHz		08,14		600	
		f = 50 MHz		09,15		650	
		f = 58.8 MHz		10,16		700	
Standby current	I_{SB}	$\overline{CS} = V_{IH}$, $\overline{OE} = V_{IH}$, f = 5 MHz, V_{CC} = 5.5 V dc 2/	1,2,3	01,02		4	mA
				03,04		4	
				05-10, 11-16		80	
		f = 18.2 MHz		05,11		150	
		f = 22.2 MHz		06,12		150	
		f = 28.6 MHz		07,13		190	
		f = 40 MHz		08,14		190	
		f = 50 MHz		09,15		240	
		f = 58.8 MHz		10,16		240	
Input Leakage current	I_{LI}	V_{CC} = 5.5 V dc, V_{IN} = GND or V_{CC}	1,2,3	All		10	µA
Output Leakage current	I_{LO}	$\overline{CS} = V_{IH}$, $\overline{OE} = V_{IH}$, V_{OUT} = GND or V_{CC}	1,2,3	All		10	µA
Output Low voltage	V_{OL}	V_{CC} = +4.5 V dc, I_{OL} = 2.1 mA	1,2,3	01-06, 11,12		0.4	V
		V_{CC} = +4.5 V dc, I_{OL} = 8mA	1,2,3	07-10, 13-16		0.4	V
Output high voltage	V_{OH}	V_{CC} = +4.5 V dc, I_{OH} = -1.0 mA	1,2,3	01-06, 11,12	2.4		V
		V_{CC} = +4.5 V dc, I_{OH} = -4.0 mA	1,2,3	07-10, 13-16	2.4		V

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V dc +4.5 V dc $\le V_{CC} \le$ +5.5 V dc unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Data retention characteristics							
Data retention supply voltage	V_{DR}	$\overline{CS} \ge V_{CC}$ - 0.2 V dc	1,2,3	01-10	2.0	5.5	V
Data retention current	I_{CCDR1}	V_{CC} = 3 V dc	1,2,3	01-04 05-10		1.6 28	mA
Capacitance							
$\overline{OE}$ capacitance 3/	C_{OE}	V_{IN} = 0 V dc , f = 1.0 MHz T_A = +25°C	4	All		50	pF
$\overline{WE}$ 1-4 capacitance 3/	C_{WE}	V_{OUT} = 0 V dc , f = 1.0 MHz T_A = +25°C	4	All		20	pF
$\overline{CS}$ capacitance 3/	C_{CS}	V_{IN} = 0 V dc , f = 1.0 MHz T_A = +25°C	1,2,3	All		20	pF
D_{0-31} capacitance 3/	$C_{I/O}$	V_{OUT} = 0 V dc , f = 1.0 MHz T_A = +25°C	1,2,3	All		20	pF
A_{0-16} capacitance 3/	C_{AD}	VOUT = 0 V dc , f = 1.0 MHz T_A = +25°C	1,2,3	All		50	pF
Functional tests							
Functional tests		See 4.3.1c	7,8A,8B	All			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V dc $+4.5$ V dc $\le V_{CC} \le +5.5$ V dc unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Read cycle timing characteristics							
Read cycle time	t_{RC}	See figure 4.	9,10,11	01 02 03 04 05,11 06,12 07,13 08,14 09,15 10,16	120 100 85 70 55 45 35 25 20 17		ns
Address access time	t_{AA}	See figure 4.	9,10,11	01 02 03 04 05,11 06,12 07,13 08,14 09,15 10,16		120 100 85 70 55 45 35 25 20 17	ns
Output hold from Address change	t_{OH}	See figure 4.	9,10,11	01-04 05-10, 11-16	5 0		ns
Chip select access time	t_{ACS}	See figure 4.	9,10,11	01 02 03 04 05,11 06,12 07,13 08,14 09,15 10,16		120 100 85 70 55 45 35 25 20 17	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ V_{SS} = 0 V dc +4.5 V dc $\le V_{CC} \le$ +5.5 V dc unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Read cycle timing characteristics - Continued.							
Output Enable to Output valid	t_{OE}	See figure 4.	9,10,11	01 02 03 04 05-07, 11-13 08,14 09,15 10,16		60 50 40 35 25 12 10 9	ns
Chip Select to output In low impedance 3/	t_{CLZ}	See figure 4.	9,10,11	01,02 03,04 05-07, 11-13 08-10, 14-16	10 10 4 2		ns
Output Enable to output In low impedance 3/	t_{OLZ}	See figure 4.	9,10,11	01-04 05,16	5 0		ns
Chip Select high to Output in high Impedance 3/	t_{CHZ}	See figure 4.	9,10,11	01,02 03,04 05,06, 11,12 07,13 08-10, 14-16		35 25 20 15 12	ns
Output Enable high to Output in high Impedance 3/	t_{OHZ}	See figure 4.	9,10,11	01,02 03,04 05,06, 11,12 07-13 08-10, 14-16		35 25 20 15 12	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V dc $+4.5$ V dc $\le V_{CC} \le +5.5$ V dc unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Write cycle AC timing.							
Write cycle time	t_{WC}	See figure 5.	9,10,11	01 02 03 04 05,11 06,12 07,13 08,14 09,15 10,16	120 100 85 70 55 45 35 25 20 17		ns
Chip select to end of write	t_{CW}	See figure 5.	9,10,11	01 02 03 04 05,11 06,12 07,13 08,14 09,10, 15,16	100 80 75 60 50 35 30 20 15		ns
Address valid to end of write	t_{AW}	See figure 5.	9,10,11	01 02 03 04 05,11 06,12 07,13 08,14 09,10, 15,16	100 80 75 60 50 35 30 20 15		ns
Data valid to end of write	t_{DW}	See figure 5.	9,10,11	01,02 03,04 05,06, 11,12 07,13 08,14 09,10, 15,16	40 30 25 20 15 12		ns
Address setup time	t_{AS}	See figure 5.	9,10,11	01-04 05-10, 11-16	0 2		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$, V_{SS} = 0 V dc, +4.5 Vdc $\le V_{CC} \le$ +5.5 Vdc unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Write cycle AC timing - Continued.							
Write pulse width	t_{WP}	See figure 5.	9,10,11	01,02 03,04 05,11 06,12 07,13 08,14 09,10, 15,16	60 50 40 35 25 17 15		ns
Write enable to output in high impedance 3/	t_{WHZ}	See figure 5.	9,10,11	01,02 03,04 05,06, 11,12 07,13 08,14 09,15 10,16		35 25 20 15 13 11 9	ns
Address hold time	t_{AH}	See figure 5.	9,10,11	01-06, 11,12 07,08, 13,14 09,15 10,16	5 2 1 0		ns
Output active from end of write 3/	t_{OW}	See figure 5.	9,10,11	01-04 05-16	5 0		ns
Data hold time	t_{DH}	See figure 5.	9,10,11	All	0		ns

1/ Unless otherwise specified, the AC test conditions are as follows:
Input pulse levels: V_{IL} = 0 V and V_{IH} = 3.0 V
Input rise and fall times: 5 nanoseconds
Input and output timing reference level: 1.5 V ± 0.5 V
Output loading: See Figure 7
Unless otherwise specified, the DC test conditions are as follows:
V_{IL} = 0.3 V and $V_{IH} = V_{CC}$ - 0.3 V

2/ $f = 1 / t_{AA}$.

3/ Parameters shall be tested as part of device characterization and after design and process change. Parameters shall be to the limits specified in table 1 for all lots not specifically tested.

Case outline M.

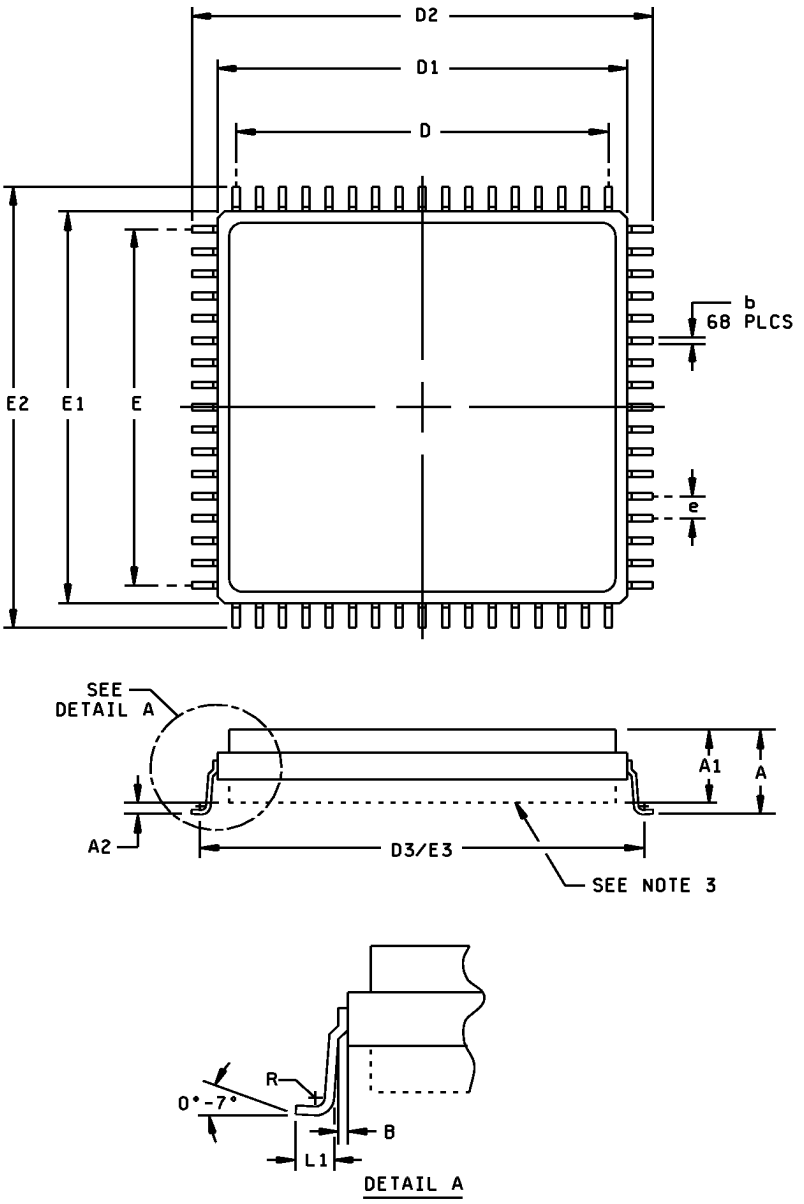


FIGURE 1. Case outline(s).

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE **A**		**5962-94611**
		REVISION LEVEL G	SHEET **11**

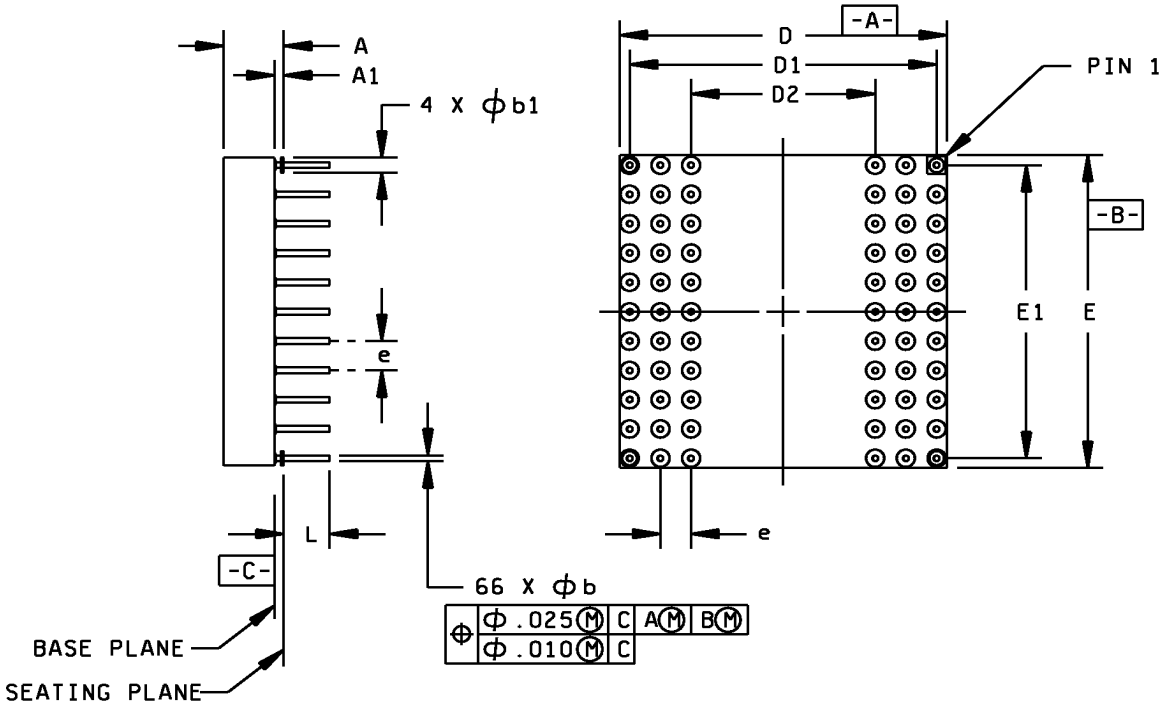
DSCC FORM 2234
APR 97

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	3.12	5.10	.123	.200
A1	2.30	4.72	.118	.186
A2	0.00	0.38	.000	.020
b	0.33	0.43	.013	.017
B	0.25 REF		.010 REF	
D/E	20.3 BSC		.800 BSC	
D1/E1	22.10	22.65	.870	.890
D2/E2	24.89	25.35	.980	1.000
D3/E3	23.75	24.28	.936	.956
e	1.27 BSC		.050 BSC	
R	0.13		.005	
L1	0.89	1.14	.035	.045

NOTES:
1. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Pin numbers are for reference only.
3. Case outline M may either be a single cavity or a dual cavity package.

FIGURE 1. Case outline(s) - Continued.

Case outline T.

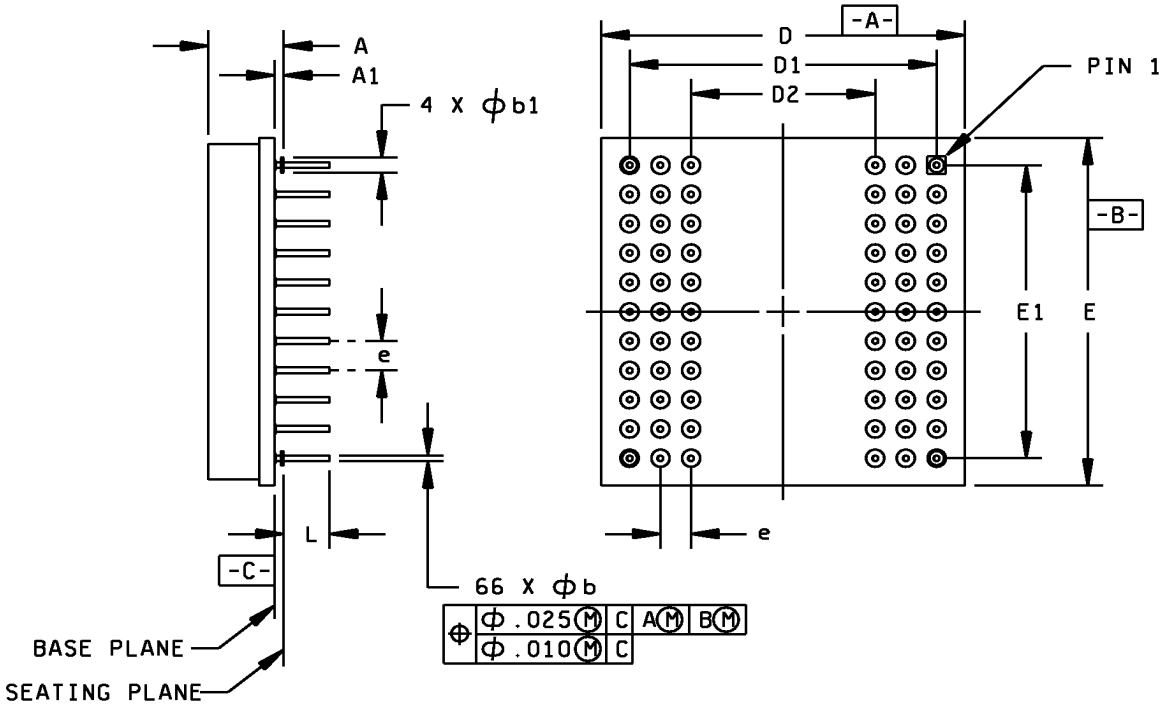


Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	3.65	4.60	.144	.181
A1	0.64	0.89	.025	.035
ϕb	0.41	0.51	.016	.020
ϕb1	1.14	1.40	.045	.055
D/E	27.05	27.56	1.065	1.085
D1/E1	25.40 TYP		1.000 TYP	
D2	15.24 TYP		.600 TYP	
e	2.54 TYP		.100 TYP	
L	3.68	3.94	.145	.155

NOTES:
1. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Pin numbers are for reference only.

FIGURE 1. Case outline(s) - Continued.

Case outline U.

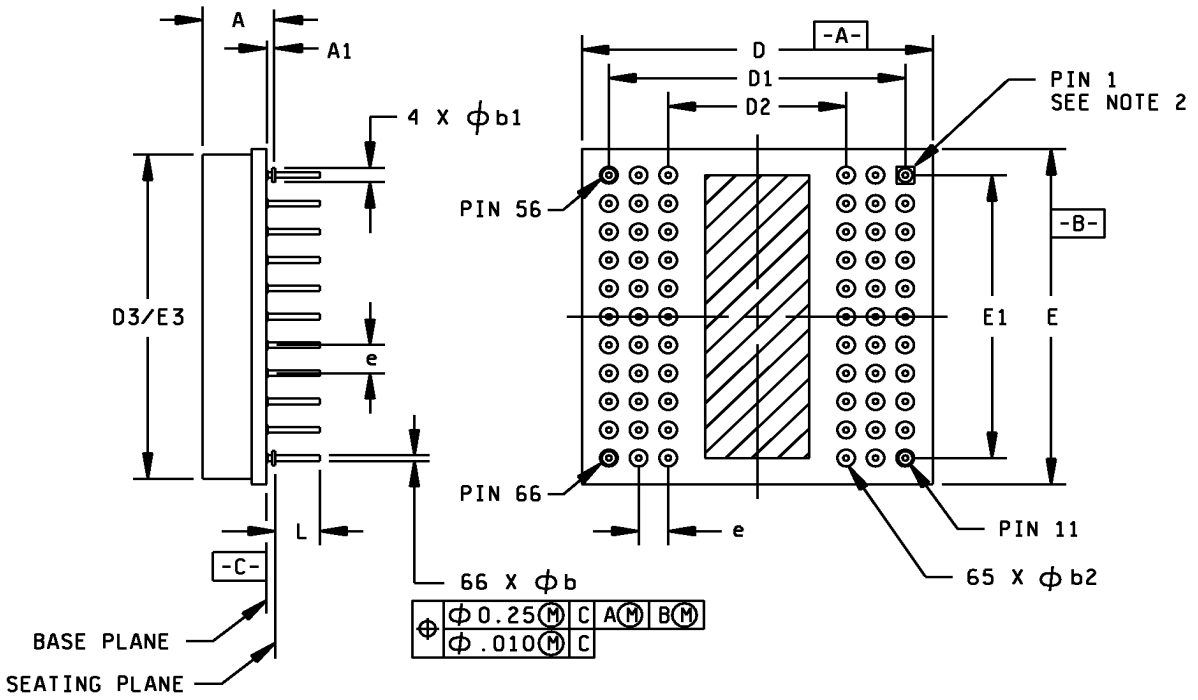


Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	5.08	6.22	.200	.245
A1	0.64	0.89	.025	.035
ϕb	0.41	0.51	.016	.020
ϕb1	1.14	1.40	.045	.055
D/E	29.72	30.48	1.170	1.200
D1/E1	25.40 TYP		1.000 TYP	
D2	15.24 TYP		.600 TYP	
e	2.54 TYP		.100 TYP	
L	3.68	3.94	.145	.155

NOTES:
1. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Pin numbers are for reference only.

FIGURE 1. Case outline(s) - Continued.

Case outline X.



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	4.83	6.22	.190	.245
A1	0.64	0.89	.025	.035
ϕb	0.41	0.51	.016	.020
ϕb1	1.14	1.40	.045	.055
ϕb2	1.65	1.91	.065	.075
D/E	34.80	35.56	1.370	1.400
D1/E1	25.40 BSC		1.000 BSC	
D2	15.24 BSC		.600 BSC	
D3/E3	34.04	34.29	1.340	1.350
e	2.54 BSC		.100 BSC	
L	3.68	3.94	.145	.155

NOTES:
1. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Pin numbers are for reference only. Pin 1 is identified by .070 " square pad.
3. For solder lead finish, dimension ϕb will increase by +.003" (+0.008 mm).

FIGURE 1. Case outline(s) - Continued.

Case outline Y.

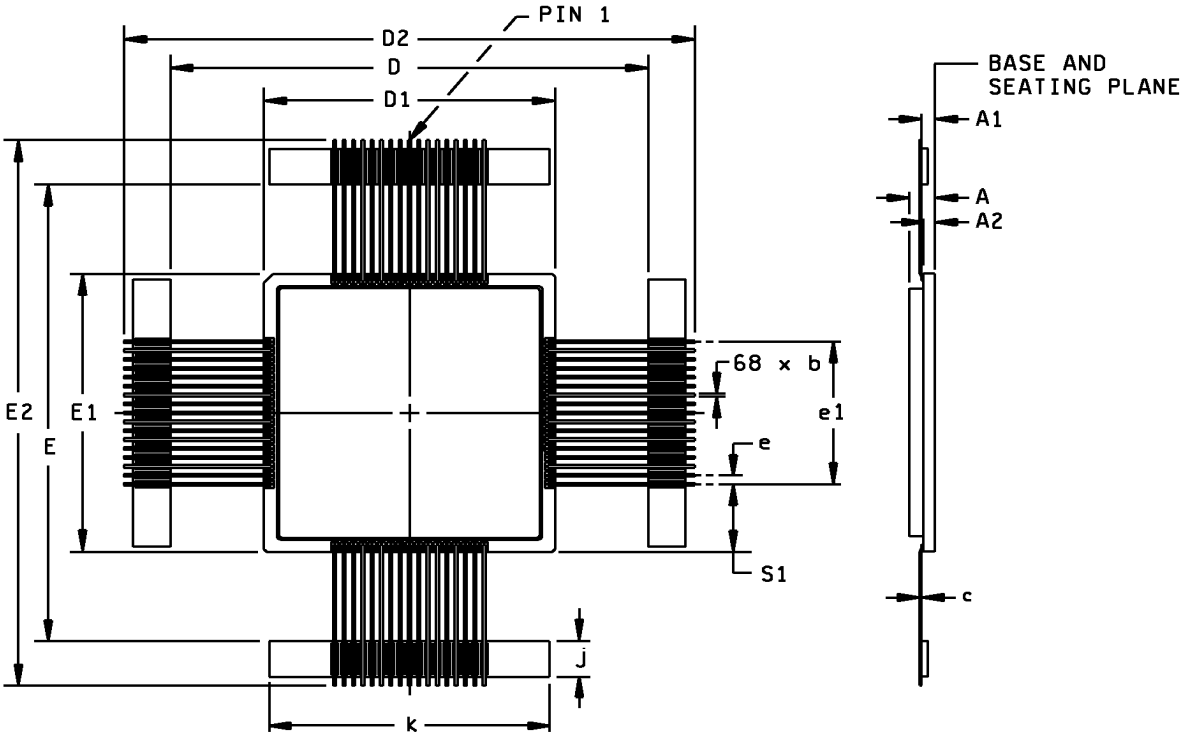


FIGURE 1. Case outline(s) - Continued.

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	2.92	3.56	.115	.140
A1	1.14	1.91	.045	.075
A2	1.14	1.39	.045	.055
b	0.31	0.46	.012	.018
c	0.23	0.31	.009	.012
D/E	63.63	66.42	2.505	2.615
D1/E1	39.24	40.01	1.545	1.575
D2/E2	73.28	79.63	2.885	3.135
e	1.27 BSC		.050 BSC	
e1	20.32 BSC		.800 BSC	
j	4.83	5.33	.190	.210
k	37.72	38.48	1.485	1.515
S1	9.65 BSC		.380 BSC	

NOTES:
1. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Pin numbers are for reference only.
3. For solder lead finish, dimension b will increase by +.003" (+0.008 mm).

FIGURE 1. Case outline(s) - Continued.

Device types	All	Device types	All	Device types	All	Device types	All
Case outline	M	Case outline	M	Case outline	M	Case outline	M
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	GND	18	GND	35	$\overline{OE}$	52	GND
2	$\overline{CS3}$	19	I/O8	36	$\overline{CS2}$	53	I/O23
3	A5	20	I/O9	37	A17	54	I/O22
4	A4	21	I/O10	38	$\overline{WE2}$	55	I/O21
5	A3	22	I/O11	39	$\overline{WE3}$	56	I/O20
6	A2	23	I/O12	40	$\overline{WE4}$	57	I/O19
7	A1	24	I/O13	41	A18	58	I/O18
8	A0	25	I/O14	42	NC	59	I/O17
9	NC	26	I/O15	43	NC	60	I/O16
10	I/O0	27	V_{CC}	44	I/O31	61	V_{CC}
11	I/O1	28	A11	45	I/O30	62	A10
12	I/O2	29	A12	46	I/O29	63	A9
13	I/O3	30	A13	47	I/O28	64	A8
14	I/O4	31	A14	48	I/O27	65	A7
15	I/O5	32	A15	49	I/O26	66	A6
16	I/O6	33	A16	50	I/O25	67	$\overline{WE1}$
17	I/O7	34	$\overline{CS1}$	51	I/O24	68	$\overline{CS4}$

FIGURE 2. Terminal connections.

Device types	All	Device types	All	Device types	All	Device types	All
Case outline	T, U, X	Case outline	T, U, X	Case outline	T, U, X	Case outline	T, U, X
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	I/O8	18	A12	35	I/O25	52	$\overline{WE3}$
2	I/O9	19	V_{CC}	36	I/O26	53	$\overline{CS3}$
3	I/O10	20	$\overline{CS1}$	37	A6	54	GND
4	A13	21	NC	38	A7	55	I/O19
5	A14	22	I/03	39	NC	56	I/O31
6	A15	23	I/015	40	A8	57	I/O30
7	A16	24	I/O14	41	A9	58	I/O29
8	A17	25	I/O13	42	I/O16	59	I/O28
9	I/O0	26	I/O12	43	I/O17	60	A0
10	I/O1	27	$\overline{OE}$	44	I/O18	61	A1
11	I/O2	28	A18	45	V_{CC}	62	A2
12	$\overline{WE2}$	29	$\overline{WE1}$	46	$\overline{CS4}$	63	I/O23
13	$\overline{CS2}$	30	I/O7	47	$\overline{WE4}$	64	I/O22
14	GND	31	I/O6	48	I/O27	65	I/O21
15	I/O11	32	I/O5	49	A3	66	I/O20
16	A10	33	I/O4	50	A4		
17	A11	34	I/O24	51	A5		

FIGURE 2. Terminal connections - Continued.

Device types	All	Device types	All	Device types	All	Device types	All
Case outline	Y	Case outline	Y	Case outline	Y	Case outline	Y
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	GND	18	GND	35	$\overline{OE}$	52	GND
2	$\overline{CS1}$	19	I/O8	36	$\overline{CS4}$	53	I/O23
3	A5	20	I/O9	37	A17	54	I/O22
4	A4	21	I/O10	38	A18	55	I/O21
5	A3	22	I/O11	39	NC	56	I/O20
6	A2	23	I/O12	40	NC	57	I/O19
7	A1	24	I/O13	41	NC	58	I/O18
8	A0	25	I/O14	42	NC	59	I/O17
9	NC	26	I/O15	43	NC	60	I/O16
10	I/O0	27	V_{CC}	44	I/O31	61	V_{CC}
11	I/O1	28	A11	45	I/O30	62	A10
12	I/O2	29	A12	46	I/O29	63	A9
13	I/O3	30	A13	47	I/O28	64	A8
14	I/O4	31	A14	48	I/O27	65	A7
15	I/O5	32	A15	49	I/O26	66	A6
16	I/O6	33	A16	50	I/O25	67	$\overline{WE}$
17	I/O7	34	$\overline{CS2}$	51	I/O24	68	$\overline{CS3}$

FIGURE 2. Terminal connections - Continued.

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O	MODE
V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Read
V_{IH}	X	X	High Z	Standby
V_{IL}	V_{IH}	V_{IH}	High Z	Output disable
V_{IL}	V_{IH}	V_{IL}	D_{IN}	Write

NOTES:
1. V_{IH} = High logic level
2. V_{IL} = Low logic level
3. X = Do not care (either high or low)
4. High Z = High impedance state

FIGURE 3. Truth table.

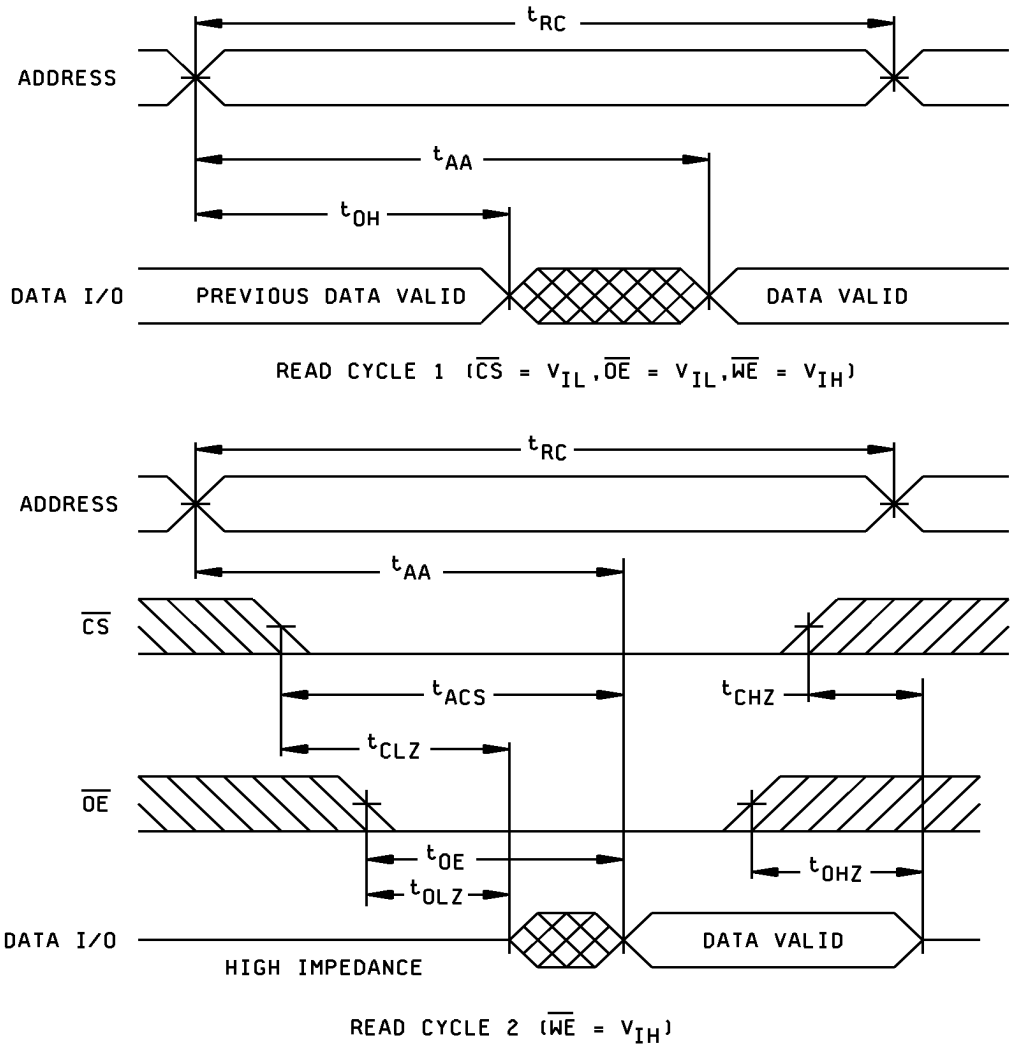
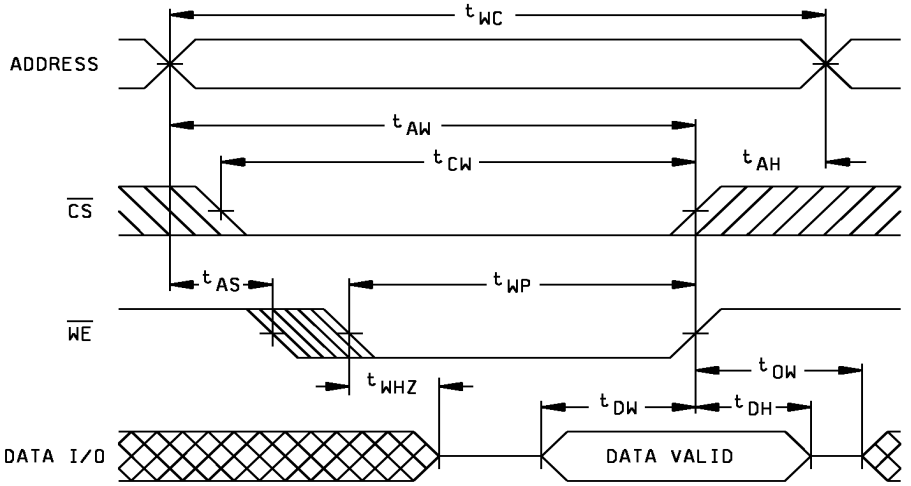
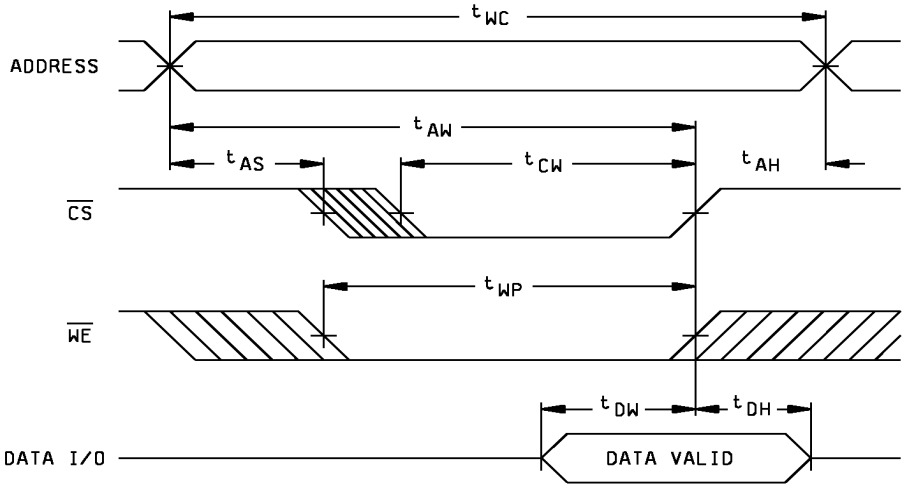


FIGURE 4. Read cycle timing diagram.



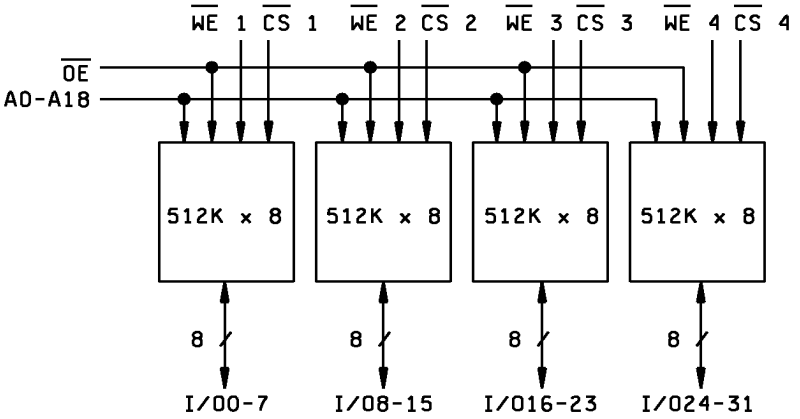
WRITE CYCLE 1 $\overline{WE}$ CONTROLLED



WRITE CYCLE 2 $\overline{CS}$ CONTROLLED

FIGURE 5. Write cycle timing diagram.

Case outlines M, T, U, and X.



Case outline Y.

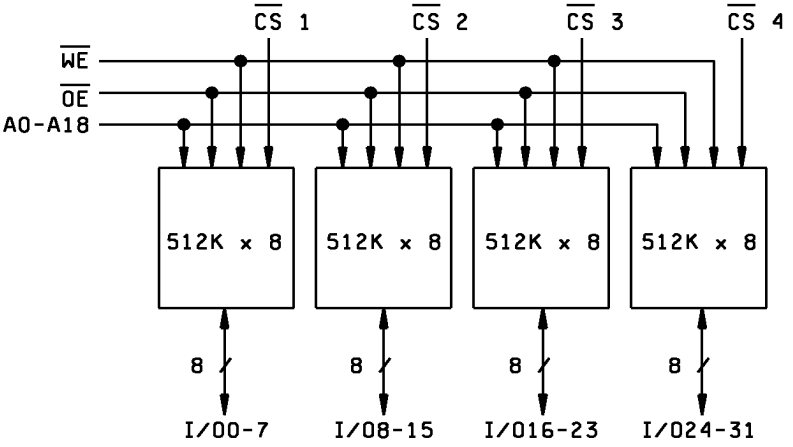
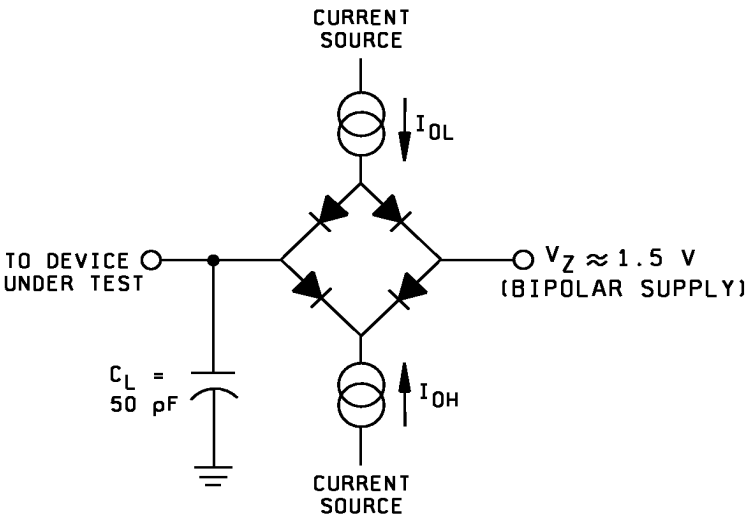


FIGURE 6. Block diagram(s).



Parameter	Typ.	Unit
Input pulse level	0 - 3.0	V
Input rise and fall	5	ns
Input and output reference level	1.5	V
Output load capacitance	50	pF

NOTES:
1. V_Z is programmable from +2 V to +7 V
2. I_{OL} and I_{OH} are programmable from 0 to 16 mA.
3. Tester impedance is Z_0 = 75 ohms.
4. V_Z is typically the midpoint of V_{OL} and V_{OH}.
5. I_{OL} and I_{OH} are adjusted to simulate a typical resistive load circuit.
6. ATE tester includes jig capacitance.

FIGURE 7. Output load circuit.

TABLE II. Electrical test requirements.

MIL-PRF-38534 test requirements	Subgroups (in accordance with MIL-PRF-38534, group A test table)
Interim electrical parameters	1,4,7,9
Final electrical parameters	1*,2,3,4,7,8A,8B,9,10,11
Group A test requirements	1,2,3,4,7,8A,8B,9,10,11
Group C end-point electrical parameters	1,2,3,4,7,8A,8B,9,10,11
End-point electrical parameters for radiation hardness assurance (RHA) devices	Not applicable.

* PDA applies to subgroup 1.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38534 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. Screening shall be in accordance with MIL-PRF-38534. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition B. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Conformance and periodic inspections. Conformance inspection (CI) and periodic inspection (PI) shall be in accordance with MIL-PRF-38534 and as specified herein.

4.3.1 Group A inspection (CI). Group A inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 shall be omitted.

c. Subgroups 7 and 8 shall include verification of the truth table on figure 3.

4.3.2 Group B inspection (PI). Group B inspection shall be in accordance with MIL-PRF-38534.

4.3.3 Group C inspection (PI). Group C inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test, method 1005 of MIL-STD-883.

(1) Test condition B. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1005 of MIL-STD-883.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.3.4 Group D inspection (PI). Group D inspection shall be in accordance with MIL-PRF-38534.

4.3.5 Radiation hardness assurance (RHA) insepction. RHA inspection is currently not applicable to this drawing.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38534.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, P. O. Box 3990, Columbus, Ohio 43216-5000 or telephone (614) 692-0512.

6.6 Sources of supply. Sources of supply are listed in MIL-HDBK-103 and QML-38534. The vendors listed in MIL-HDBK-103 and QML-38534 have submitted a certificate of compliance (see 3.7 herein) to DSCC-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 99-08-18

Approved sources of supply for SMD 5962-94611 are listed below for immediate acquisition only and shall be added to MIL-HDBK-103 and QML-38534 during the next revision. MIL-HDBK-103 and QML-38534 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38534.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9461101HMA	54230	WS512K32-120G2Q
5962-9461101HMC	54230	WS512K32-120G2Q
5962-9461101HXA	54230	WS512K32N-120H2Q
5962-9461101HXC	54230	WS512K32N-120H2Q
5962-9461101HYC	54230	WS512K32-120G4TQ
5962-9461101HUA	54230	WS512K32N-120HQ
5962-9461101HUC	54230	WS512K32N-120HQ
5962-9461102HMA	54230	WS512K32-100G2Q
5962-9461102HMC	54230	WS512K32-100G2Q
5962-9461102HXA	54230	WS512K32N-100H2Q
5962-9461102HXC	54230	WS512K32N-100H2Q
5962-9461102HYC	54230	WS512K32-100G4TQ
5962-9461102HUA	54230	WS512K32N-100HQ
5962-9461102HUC	54230	WS512K32N-100HQ
5962-9461103HMA	54230	WS512K32-85G2Q
5962-9461103HMC	54230	WS512K32-85G2Q
5962-9461103HXA	54230	WS512K32N-85H2Q
5962-9461103HXC	54230	WS512K32N-85H2Q
5962-9461103HYC	54230	WS512K32-85G4TQ
5962-9461103HUA	54230	WS512K32N-85HQ
5962-9461103HUC	54230	WS512K32N-85HQ
5962-9461104HMA	54230	WS512K32-70G2Q
5962-9461104HMC	54230	WS512K32-70G2Q
5962-9461104HXA	54230	WS512K32N-70H2Q
5962-9461104HXC	54230	WS512K32N-70H2Q
5962-9461104HYC	54230	WS512K32-70G4TQ
5962-9461104HUA	54230	WS512K32N-70HQ
5962-9461104HUC	54230	WS512K32N-70HQ
5962-9461105HMA	0EU86	AS8S512K32Q-55L/Q
5962-9461105HMC	0EU86	AS8S512K32Q-55L/Q
5962-9461105HMA	54230	WS512K32-55G2Q
5962-9461105HMC	54230	WS512K32-55G2Q
5962-9461105HMA	88379	ACT-S512K32N-055F2Q
5962-9461105HMC	88379	ACT-S512K32N-055F2Q
5962-9461105HTA	0EU86	AS8S512K32P-55L/Q
5962-9461105HTC	0EU86	AS8S512K32P-55L/Q
5962-9461105HTA	54230	WS512K32N-55H1Q
5962-9461105HTC	54230	WS512K32N-55H1Q
5962-9461105HTA	88379	ACT-S512K32N-055P7Q
5962-9461105HTC	88379	ACT-S512K32N-055P7Q
5962-9461105HXA	54230	WS512K32N-55H2Q
5962-9461105HXC	54230	WS512K32N-55H2Q
5962-9461105HXA	88379	ACT-S512K32N-055P1Q
5962-9461105HXC	88379	ACT-S512K32N-055P1Q
5962-9461105HYA	88379	ACT-S512K32N-055F1Q
5962-9461105HYC	88379	ACT-S512K32N-055F1Q
5962-9461105HYC	54230	WS512K32-55G4TQ

See footnotes at end of table.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9461106HMA	0EU86	AS8S512K32Q-45L/Q
5962-9461106HMC	0EU86	AS8S512K32Q-45L/Q
5962-9461106HMA	54230	WS512K32-45G2Q
5962-9461106HMC	54230	WS512K32-45G2Q
5962-9461106HMA	88379	ACT-S512K32N-045F2Q
5962-9461106HMC	88379	ACT-S512K32N-045F2Q
5962-9461106HTA	0EU86	AS8S512K32P-45L/Q
5962-9461106HTC	0EU86	AS8S512K32P-45L/Q
5962-9461106HTA	54230	WS512K32N-45H1Q
5962-9461106HTC	54230	WS512K32N-45H1Q
5962-9461106HTA	88379	ACT-S512K32N-045P7Q
5962-9461106HTC	88379	ACT-S512K32N-045P7Q
5962-9461106HXA	54230	WS512K32N-45H2Q
5962-9461106HXC	54230	WS512K32N-45H2Q
5962-9461106HXA	88379	ACT-S512K32N-045P1Q
5962-9461106HXC	88379	ACT-S512K32N-045P1Q
5962-9461106HYA	88379	ACT-S512K32N-045F1Q
5962-9461106HYC	88379	ACT-S512K32N-045F1Q
5962-9461106HYC	54230	WS512K32-45G4TQ
5962-9461107HMA	0EU86	AS8S512K32Q-35L/Q
5962-9461107HMC	0EU86	AS8S512K32Q-35L/Q
5962-9461107HMA	54230	WS512K32-35G2Q
5962-9461107HMC	54230	WS512K32-35G2Q
5962-9461107HMA	88379	ACT-S512K32N-035F2Q
5962-9461107HMC	88379	ACT-S512K32N-035F2Q
5962-9461107HTA	0EU86	AS8S512K32P-35L/Q
5962-9461107HTC	0EU86	AS8S512K32P-35L/Q
5962-9461107HTA	54230	WS512K32N-35H1Q
5962-9461107HTC	54230	WS512K32N-35H1Q
5962-9461107HTA	88379	ACT-S512K32N-035P7Q
5962-9461107HTC	88379	ACT-S512K32N-035P7Q
5962-9461107HXA	54230	WS512K32N-35H2Q
5962-9461107HXC	54230	WS512K32N-35H2Q
5962-9461107HXA	88379	ACT-S512K32N-035P1Q
5962-9461107HXC	88379	ACT-S512K32N-035P1Q
5962-9461107HYA	88379	ACT-S512K32N-035F1Q
5962-9461107HYC	88379	ACT-S512K32N-035F1Q
5962-9461107HYC	54230	WS512K32-35G4TQ
5962-9461108HMA	0EU86	AS8S512K32Q-25L/Q
5962-9461108HMC	0EU86	AS8S512K32Q-25L/Q
5962-9461108HMA	54230	WS512K32-25G2Q
5962-9461108HMC	54230	WS512K32-25G2Q
5962-9461108HMA	88379	ACT-S512K32N-025F2Q
5962-9461108HMC	88379	ACT-S512K32N-025F2Q
5962-9461108HTA	0EU86	AS8S512K32P-25L/Q
5962-9461108HTC	0EU86	AS8S512K32P-25L/Q
5962-9461108HTA	54230	WS512K32N-25H1Q
5962-9461108HTC	54230	WS512K32N-25H1Q
5962-9461108HTA	88379	ACT-S512K32N-025P7Q
5962-9461108HTC	54230	ACT-S512K32N-025P7Q
5962-9461108HXA	54230	WS512K32N-25H2Q
5962-9461108HXC	54230	WS512K32N-25H2Q
5962-9461108HXA	88379	ACT-S512K32N-025P1Q
5962-9461108HXC	88379	ACT-S512K32N-025P1Q
5962-9461108HYA	88379	ACT-S512K32N-025F1Q
5962-9461108HYC	88379	ACT-S512K32N-025F1Q
5962-9461108HYC	54230	WS512K32-25G4TQ

See footnotes at end of table.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9461109HMA	0EU86	AS8S512K32Q-20L/Q
5962-9461109HMC	0EU86	AS8S512K32Q-20L/Q
5962-9461109HMA	54230	WS512K32-20G2Q
5962-9461109HMC	54230	WS512K32-20G2Q
5962-9461109HMA	88379	ACT-S512K32N-020F2Q
5962-9461109HMC	88379	ACT-S512K32N-020F2Q
5962-9461109HTA	0EU86	AS8S512K32P-20L/Q
5962-9461109HTC	0EU86	AS8S512K32P-20L/Q
5962-9461109HTA	54230	WS512K32N-20H1Q
5962-9461109HTC	54230	WS512K32N-20H1Q
5962-9461109HTA	88379	ACT-S512K32N-020P7Q
5962-9461109HTC	88379	ACT-S512K32N-020P7Q
5962-9461109HXA	54230	WS512K32N-20H2Q
5962-9461109HXC	54230	WS512K32N-20H2Q
5962-9461109HXA	88379	ACT-S512K32N-020P1Q
5962-9461109HXC	88379	ACT-S512K32N-020P1Q
5962-9461109HYA	88379	ACT-S512K32N-020F1Q
5962-9461109HYC	88379	ACT-S512K32N-020F1Q
5962-9461109HYC	54230	WS512K32-20G4TQ
5962-9461110HMA	0EU86	AS8S512K32Q-17L/Q
5962-9461110HMC	0EU86	AS8S512K32Q-17L/Q
5962-9461110HMA	54230	WS512K32-17G2Q
5962-9461110HMC	54230	WS512K32-17G2Q
5962-9461110HMA	88379	ACT-S512K32N-017F2Q
5962-9461110HMC	88379	ACT-S512K32N-017F2Q
5962-9461110HTA	0EU86	AS8S512K32P-17L/Q
5962-9461110HTC	0EU86	AS8S512K32P-17L/Q
5962-9461110HTA	54230	WS512K32N-17H1Q
5962-9461110HTC	54230	WS512K32N-17H1Q
5962-9461110HTA	88379	ACT-S512K32N-017P7Q
5962-9461110HTC	88379	ACT-S512K32N-017P7Q
5962-9461110HXA	54230	WS512K32N-17H2Q
5962-9461110HXC	54230	WS512K32N-17H2Q
5962-9461110HXA	88379	ACT-S512K32N-017P1Q
5962-9461110HXC	88379	ACT-S512K32N-017P1Q
5962-9461110HYA	88379	ACT-S512K32N-017F1Q
5962-9461110HYC	88379	ACT-S512K32N-017F1Q
5962-9461110HYC	54230	WS512K32-17G4TQ
5962-9461111HMA	0EU86	AS8S512K32Q-55/Q
5962-9461111HMC	0EU86	AS8S512K32Q-55/Q
5962-9461111HMA	54230	WS512K32D-55G2Q
5962-9461111HMC	54230	WS512K32D-55G2Q
5962-9461111HTA	0EU86	AS8S512K32P-55/Q
5962-9461111HTC	0EU86	AS8S512K32P-55/Q
5962-9461111HTA	54230	WS512K32ND-55H1Q
5962-9461111HTC	54230	WS512K32ND-55H1Q
5962-9461111HXA	54230	WS512K32ND-55H2Q
5962-9461111HXC	54230	WS512K32ND-55H2Q
5962-9461111HYC	54230	WS512K32D-55G4TQ

See footnotes at end of table.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9461112HMA	0EU86	AS8S512K32Q-45/Q
5962-9461112HMC	0EU86	AS8S512K32Q-45/Q
5962-9461112HMA	54230	WS512K32D-45G2Q
5962-9461112HMC	54230	WS512K32D-45G2Q
5962-9461112HTA	0EU86	AS8S512K32P-45/Q
5962-9461112HTC	0EU86	AS8S512K32P-45/Q
5962-9461112HTA	54230	WS512K32ND-45H1Q
5962-9461112HTC	54230	WS512K32ND-45H1Q
5962-9461112HXA	54230	WS512K32ND-45H2Q
5962-9461112HXC	54230	WS512K32ND-45H2Q
5962-9461112HYC	54230	WS512K32D-45G4TQ
5962-9461113HMA	0EU86	AS8S512K32Q-35/Q
5962-9461113HMC	0EU86	AS8S512K32Q-35/Q
5962-9461113HMA	54230	WS512K32D-35G2Q
5962-9461113HMC	54230	WS512K32D-35G2Q
5962-9461113HTA	0EU86	AS8S512K32P-35/Q
5962-9461113HTC	0EU86	AS8S512K32P-35/Q
5962-9461113HTA	54230	WS512K32ND-35H1Q
5962-9461113HTC	54230	WS512K32ND-35H1Q
5962-9461113HXA	54230	WS512K32ND-35H2Q
5962-9461113HXC	54230	WS512K32ND-35H2Q
5962-9461113HYC	54230	WS512K32D-35G4TQ
5962-9461114HMA	0EU86	AS8S512K32Q-25/Q
5962-9461114HMC	0EU86	AS8S512K32Q-25/Q
5962-9461114HMA	54230	WS512K32D-25G2Q
5962-9461114HMC	54230	WS512K32D-25G2Q
5962-9461114HTA	0EU86	AS8S512K32P-25/Q
5962-9461114HTC	0EU86	AS8S512K32P-25/Q
5962-9461114HTA	54230	WS512K32ND-25H1Q
5962-9461114HTC	54230	WS512K32ND-25H1Q
5962-9461114HXA	54230	WS512K32ND-25H2Q
5962-9461114HXC	54230	WS512K32ND-25H2Q
5962-9461114HYC	54230	WS512K32D-25G4TQ
5962-9461115HMA	0EU86	AS8S512K32Q-20/Q
5962-9461115HMC	0EU86	AS8S512K32Q-20/Q
5962-9461115HMA	54230	WS512K32D-20G2Q
5962-9461115HMC	54230	WS512K32D-20G2Q
5962-9461115HTA	0EU86	AS8S512K32P-20/Q
5962-9461115HTC	0EU86	AS8S512K32P-20/Q
5962-9461115HTA	54230	WS512K32ND-20H1Q
5962-9461115HTC	54230	WS512K32ND-20H1Q
5962-9461115HXA	54230	WS512K32ND-20H2Q
5962-9461115HXC	54230	WS512K32ND-20H2Q
5962-9461115HYC	54230	WS512K32D-20G4TQ

See footnotes at end of table.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9461116HMA	0EU86	AS8S512K32Q-17/Q
5962-9461116HMC	0EU86	AS8S512K32Q-17/Q
5962-9461116HMA	54230	WS512K32D-17G2Q
5962-9461116HMC	54230	WS512K32D-17G2Q
5962-9461116HTA	0EU86	AS8S512K32P-17/Q
5962-9461116HTC	0EU86	AS8S512K32P-17/Q
5962-9461116HTA	54230	WS512K32ND-17H1Q
5962-9461116HTC	54230	WS512K32ND-17H1Q
5962-9461116HXA	54230	WS512K32ND-17H2Q
5962-9461116HXC	54230	WS512K32ND-17H2Q
5962-9461116HYC	54230	WS512K32D-17G4TQ

1/ The lead finish shown for each PIN, representing a hermetic package, is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
0EU86	Austin Semicondutor, Incorporated 8701 Cross Park Drive Austin, TX 78754-4566
54230	White Electronic Designs Corporation 3601 East University Drive Phoenix, AZ 85034-7217
88379	Aeroflex Circuit Technology Corporation 35 South Service Road Plainview, NY 11803-4101