Monolithic MMI Memories

16x16 Bit CMOS Multiplier
67C7016 - 35/- 45/- 55
67C7017 - 35/- 45/- 55

ADVANCE INFORMATION

Features/Benefits

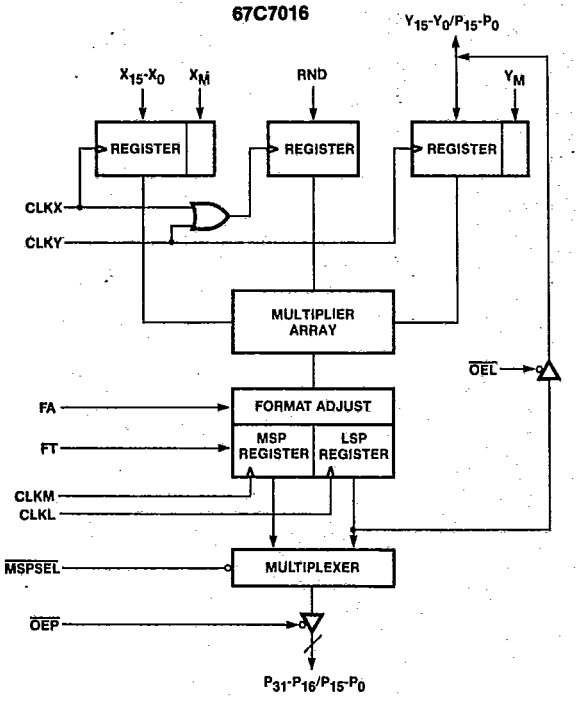
- 16x16 parallel multiplier
- High speed multiply
  - 35 ns Max '7016-35/'7017-35
  - 45 ns Max '7016-45/'7017-45
  - 55 ns Max '7016-55/'7017-55
- Low power CMOS technology
  - Zero standby power
  - 7 mA per MHz active I_{CC} (Typical)
- Mixed mode 2's complement, unsigned or mixed operand
- '7017 is optimized for microprocessor systems, single clock with register enables
- Plug-in compatible with TRW MFY016H/K, AMD29516/A, 29517/A
- Single 5 V supply
- Available in DIP or PLCC

Packaging Information

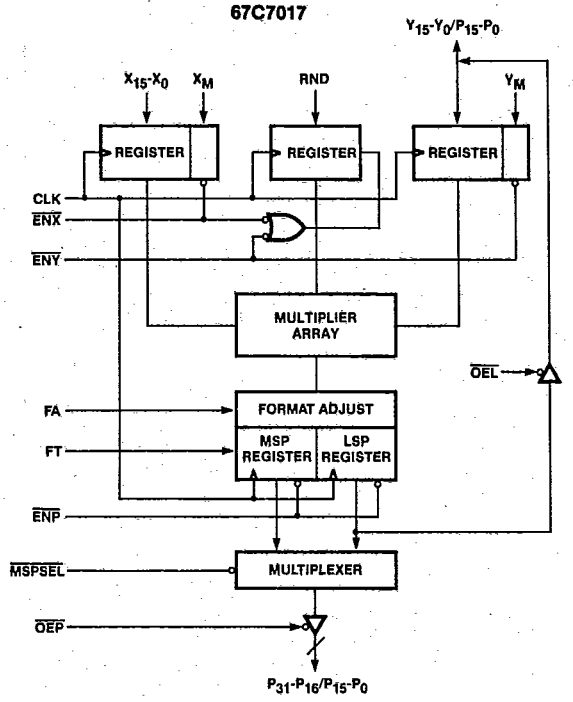
PART NUMBER	SPEED (T_{MC})	PACKAGE	TEMP
67C7016-35	35 ns	J,N,NL(68)	Com
67C7017-35	35 ns	J,N,NL(68)	Com
67C7016-45	45 ns	J,N,NL(68)	Com
67C7017-45	45 ns	J,N,NL(68)	Com
67C7016-55	55 ns	J,N,NL(68)	Com
67C7017-55	55 ns	J,N,NL(68)	Com

Functional Block Diagrams

67C7016



67C7017



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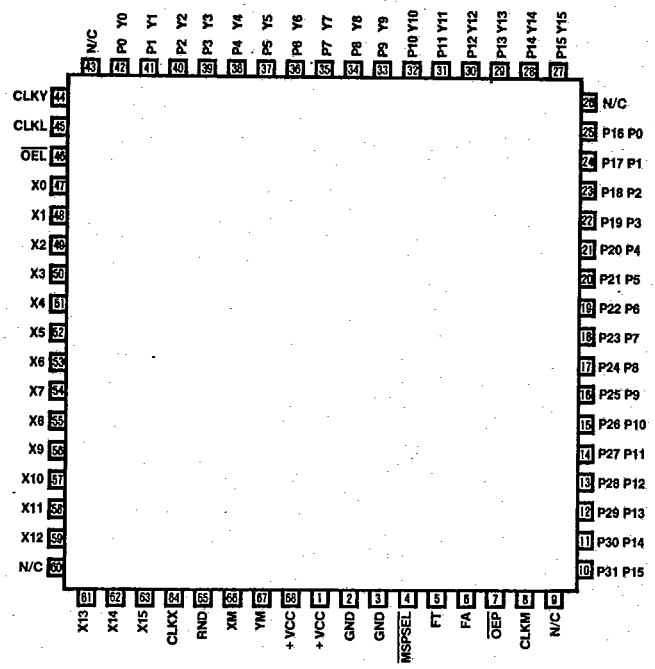
This document contains information on a product under development at Monolithic Memories Inc. The information is intended to help you to evaluate this product. Monolithic Memories reserves the right to change or discontinue work on this proposed product without notice.

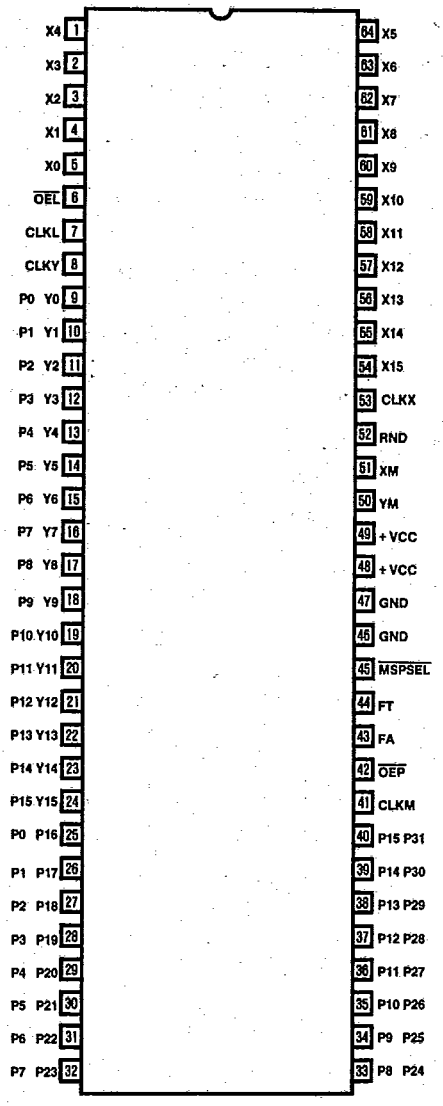
2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
TWX: 910-338-2376
Monolithic Memories MMI

Pin Configurations

67C7016
68 Pin PLCC

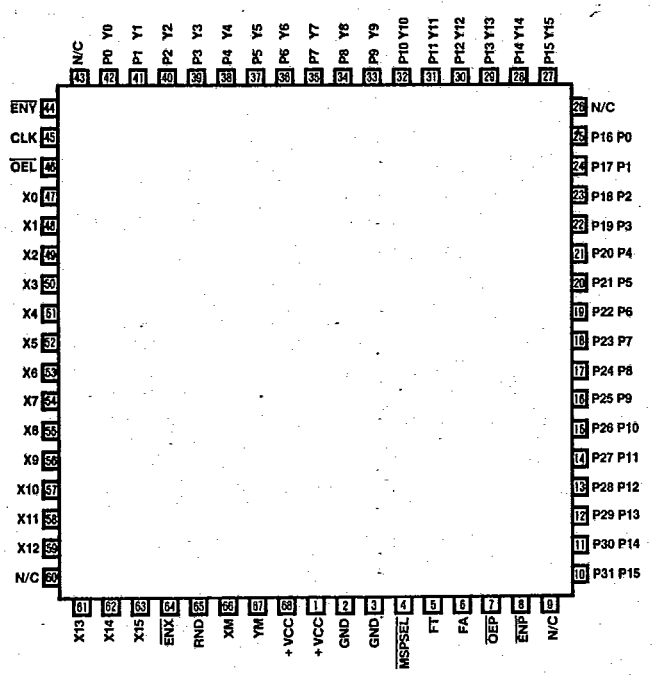


67C7016
64 Pin DIP

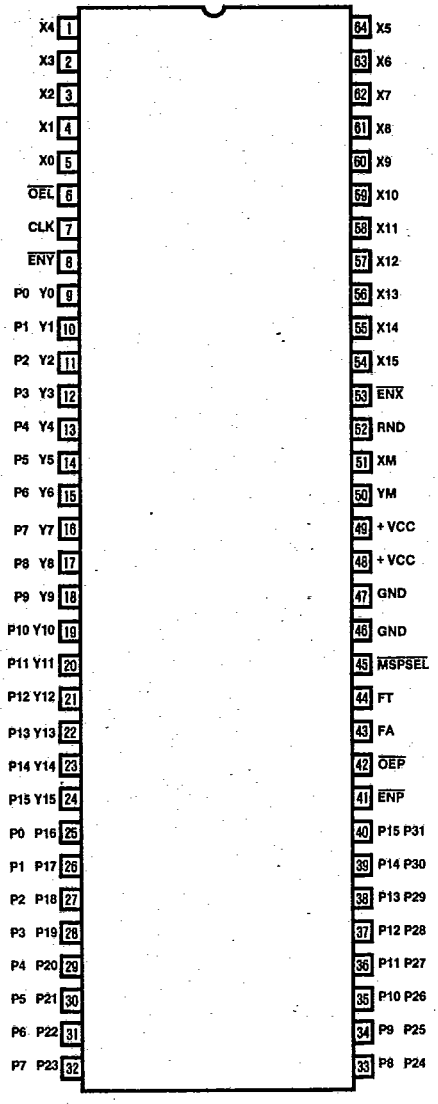


Pin Configurations

67C7017
68 Pin DIP



67C7017
64 Pin DIP



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Descriptions

The '7016/7017 are CMOS 16x16 high speed parallel multipliers. Designed with state-of-the-art CMOS technology and a multiplication scheme based on modified Booth's algorithm, these devices can achieve bipolar TTL speed at a significantly reduced power level. In addition, the product is designed to be pin-for-pin replacement for the TRW MPY016H/K and the AMD 29516/A, 29517/A.

The architecture of the '7016/7017 family generates a 32-bit product of two 16-bit input operands. Two 16-bit registers are provided for the X and Y operands. These operands can be specified as either 2's complement or unsigned numbers through the XM and the YM control inputs. These two signals are registered simultaneously at their respective operand clocks.

At the output of the multiplier array a format adjust control (FA) allows the user to select either a full 32-bit product or a left shifted 31-bit product. Two 16-bit output registers are provided to hold the most and least significant halves of the result (MSP and LSP) as defined by FA. For asynchronous output these registers may be made transparent by taking the feed through control (FT) high. A round control (RND) allows the rounding of the MSP. This control is registered, and is entered at the rising edge of the logical OR of both CLKX and CLKY for the '7016 and is enabled by a LOW signal in either ENX or ENY in the '7017. the two halves of the product may be routed to a 16-bit three-state output port (P) via a multiplexer. In addition the LSP is connected to the Y-input port through a separate three-state buffer so that a 32-bit product can be available simultaneously.

In the '7016, the X, Y, MSP and LSP registers have independent clocks (CLKX, CCLKY, CLKM, CLKL). The output multiplexer control ($\overline{\text{MSPSEL}}$) uses a pin which is a supply ground in the TRW MPY16H. When this control is LOW the function is that of the MPY16H, thus allowing full compatibility.

The '7017 differs in that it has a single clock input (CLK) and three register enables ($\overline{\text{ENX}}$, $\overline{\text{ENY}}$, $\overline{\text{ENP}}$) for the two input registers and the entire product. This facilitates the use of the part in microprocessor systems. In both parts data is entered into the registers on the positive edge of the clock.

The '7016/7017 family has a wide variety of applications in high performance computers and digital signal processing. In computer applications this multiplier can be used to construct numerical processing functional units (e.g., array processors, matrix processors, floating point multiplier/dividers etc.). In digital signal processing the multiplier can be used to construct special algorithm engines for applications like digital filtering, FFT, speech recognition and synthesis, adaptive controls and image processing.

Signal Description

Input/Output data

X15-X0: 16 bit data inputs.

Y15-Y0: 16 bit data inputs. These inputs are multiplexed with the least significant product (LSP) outputs.

P15-P0: The least significant product (LSP) outputs. These signals are multiplexed with the Y data inputs. The product term is available when OEL is low. Alternatively, these outputs can be accessed from the MSP output port when MSPSEL is high.

P31-P16: The most significant product (MSP) outputs.

Input Clocks (67C7016 only)

CLKX: The rising edge of this clock loads the input data (X15-X0) and the associated mode control signal XM into the input register.

CLKY: The rising edge of this clock loads the input data (Y15-Y0) and the associated mode control signal YM into the input register.

CLKM: The rising edge of this clock loads the most significant product (MSP) output register.

CLKL: The rising edge of this clock loads the least significant product (LSP) output register.

Input Clocks (67C7017 only)

CLK: The rising edge of this clock loads all input/output registers.

$\overline{\text{ENX}}$: Clock enable for the X15-X0 input register, XM input register and the round register.

$\overline{\text{ENY}}$: Clock enable for the Y15-Y0 input register, YM input register and the round register.

$\overline{\text{ENP}}$: Clock enable for the most significant product (MSP) and least significant product (LSP) register.

Control Signals

XM, YM: Mode control signals for the input data word. A low input indicates unsigned data format and a high input represents 2's complement data format.

FA: Format Adjust. When this input is high, a full 32-bit product is produced in MSP and LSP registers. When this input is low, the sign bit will appear in the most significant bit of both the MSP and the LSP. In such cases only a 31-bit product is provided. The FA input is required to be a high when either integer unsigned magnitude or mixed mode formats are used. (See the DATA FORMATS section for further detail.)

FT: Flow-through. When this input is high, both the MSP register and the LSP register are transparent.

$\overline{\text{OEL}}$: Three-state enable signal for routing LSP to the Y/LSP I/O ports.

$\overline{\text{OEP}}$: Three-state enable signal for the product output port.

RND: Round control signal for the most significant product (MSP). When this input is high, a one will be added to the most significant bit of the least significant product (LSP). This rounding operation is done before the output is sent to the format adjust clock. As a result, the location of this round bit in the final product depends on the FA input. When FA = 0, the round bit is added to location P14; when FA = 1, the round bit is added to location P15. The RND input is registered at the rising edge of the logical OR of both the CLKX and CLKY. In the single clock architecture, the RND register is enabled when either the X register or the Y register is enabled.

$\overline{\text{MSPSEL}}$: When the $\overline{\text{MSPSEL}}$ input is low, the MSP is available for the output port. When this input is high, the LSP is available at the output port.