Low Cost PC Clock Generator

Features

- Generates up to 8 preset frequencies, 2 peripheral clocks, and buffers the input reference frequency
- Additional general purpose buffers
- Low skew output buffers
- Slow down feature supporting "Green PC" applications
- Supports Pentium™ and all x86-based designs
- External loop filter provides exceptionally smooth, glitch-free frequency transitions
- Low, short-term and long-term jitter
- Supports ISA, VESA, and PCI-based designs
- CMOS technology in 28-pin SSOP (209 mil) package
- 5V or 3.3V supply

Description

CH9471 is a dual PLL clock generator designed for high performance computer motherboards used in portable computers, notebooks, and handheld PDAs.

CH9471 buffers the 14.318 MHz reference frequency, generates a CPU clock from a preset ROM table, and provides two peripheral clocks. The CPU output frequencies are selected with the frequency select inputs, FS[2:0]. In addition, CH9471 has built-in on-chip buffers to provide the necessary buffering for PCI or VESA applications.

CH9471's slow down mode allows the system to run slower than the normal CPU speed, reducing power consumption. The need for multiple oscillators is also eliminated, since CH9471 generates all essential clock signals for personal computer motherboards.

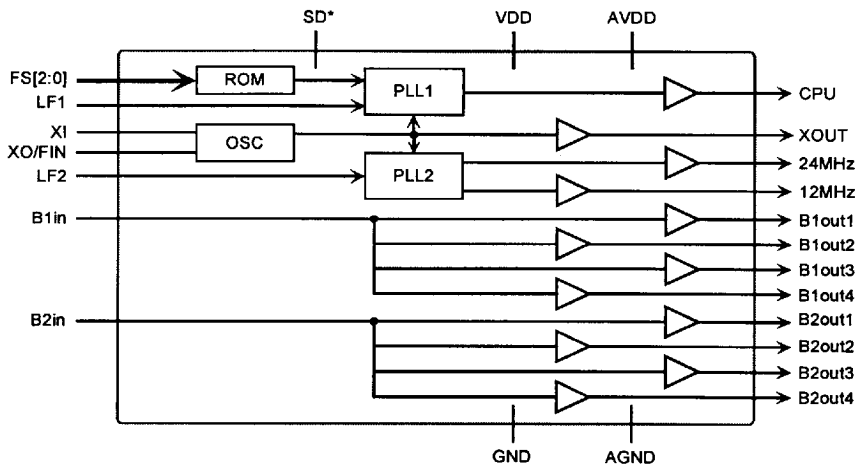

Figure 1: Block Diagram

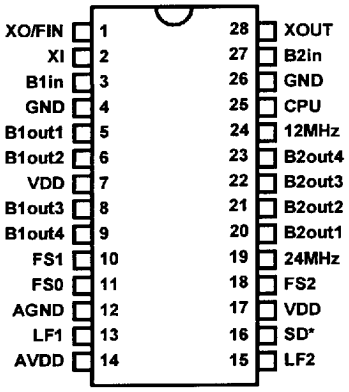

Figure 2: CH9471A

Table 1 • Pin Description CH9471A

Pin	Type	Symbol	Description
1	Out / In	XO / FIN	Crystal output or external FREF input
2	In	XI	Crystal input
3, 27	In	B1in, B2in	On-chip buffer inputs (internal pull-up)
4, 26	Power	GND	Ground
5, 6, 8, 9	Out	B1out1, B1out2 B1out3, B1out4	Buffered output pins of B1in capable of sinking or sourcing 12 mA. These pins can be used to buffer critical clock lines for PCI or VESA applications.
7, 17	Power	VDD	5V or 3.3V supply
10, 11, 18	In	FS1, FS0, FS2	Frequency select inputs for CPU (internal pull-up)
12	Power	AGND	Analog ground
13, 15	Out	LF1, LF2	External loop filters
14	Power	AVDD	Analog power supply
16	In	SD*	Slow down input (active low, internal pull-up)
19	Out	24 MHz	24 MHz clock output
20, 21, 22, 23	Out	B2out1, B2out2 B2out3, B2out4	Buffered output pins of B2in capable of sinking or sourcing 12 mA. These pins can be used to buffer critical clock lines for PCI or VESA applications.
24	Out	12 MHz	12 MHz clock output
25	Out	CPU	CPU clock output
28	Out	XOUT	Buffered reference (14.318 MHz) clock output

Table 2 • Frequencies for CH9471A (in MHz)

Frequency Select Inputs			CPU Output	
FS2	FS1	FS0	SD* = 1	SD* = 0
0	0	0	66.6	16.0
0	0	1	80.0	16.0
0	1	0	60.0	33.3
0	1	1	30.0	8.0
1	0	0	33.3	8.0
1	0	1	40.0	8.0
1	1	0	50.0	16.0
1	1	1	25.0	8.0

Table 3 • Absolute Maximum Ratings

Symbol	Description	Value	Unit
V_{DD}	Power supply voltage with respect to GND	–0.5 TO +7.0	V
V_{IN}	Input voltage on any pin with respect to GND	–0.5 TO V_{DD}+0.5	V
T_{STOR}	Storage temperature	–55 TO +150	°C

Note: Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated under the normal operating conditions is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

5

Table 4 • DC Specifications (Operating Conditions: T_A = 0°C – 70°C, V_{DD} = 5V ±5%)

Symbol	Description	Test Condition @T_A = 25°C	Min	Typ	Max	Unit
V_{OH}	Output high voltage	V_{DD} = 4.75V, I_{OH} = 12mA	2.4			V
V_{OL}	Output low voltage	V_{DD} = 4.75V, I_{OL} = 12mA			0.4	V
V_{IH}	Input high voltage		2.0			V
V_{IL}	Input low voltage				0.8	V
I_{PU}	Input pull-up current			5	20	µA
I_{LK}	Input leakage current		–10		10	µA
C_I	Input capacitance	Except XO / FIN, XI			10	pF
C_I	Input capacitance	Pins XO / FIN, XI		20		pF
I_{SD}[1]	Slow down supply current	SD* = Low, V_{DD} = 5.0V, No load		10		mA
I_{DD}[1]	Operating current	V_{DD} = 5V CPU = 40 MHz, No load CPU = 80 MHz, No load		20 25		mA

Note: 1 Indicates values when on-chip buffers are inactive

Table 5 • AC Specifications (Operating Conditions: T_A = 0°C – 70°C, V_{DD} = 5V ±5%)

Symbol	Description	Test Condition @T_A = 25°C	Min	Typ	Max	Unit
FXTAL	Crystal frequency			14.318		MHz
FIN	Input frequency (crystal pin)		1	14.318	32	MHz
FIN	Input frequency (buffer pin)				100	MHz
TR	Output clock rise time	30 pF load, V_{OUT} = 0.8V to 2.0V			2	ns
TF	Output clock fall time	30 pF load, V_{OUT} = 0.8V to 2.0V			2	ns
TDC	Duty cycle		45	50	55	%
TJCC	Jitter, cycle to cycle	CPU = 50 MHz		100		ps
TFT	Frequency transition time	8 – 80 MHz with 0.1 µF LF capacitor		10		ms
TPU	Power up time	From OFF to 100 MHz with 0.1 µF LF capacitor		15		ms
TPLH, TPHL	Propagation delay (Bin to Bout)			3.2		ns
TSKEW	Buffer out skew				0.7	ns

Table 6 • DC Specifications (Operating Conditions: T_A = 0°C – 70°C, V_{DD} = 3.3V ± 0.3V)

Symbol	Description	Test Condition @T_A = 25°C	Min	Typ	Max	Unit
V_{OH}	Output high voltage	V_{DD} = 3.0V, I_{OH} = 1.5mA	V_{DD} – 0.5			V
V_{OL}	Output low voltage	V_{DD} = 3.0V, I_{OL} = 3mA			0.5	V
V_{IH}	Input high voltage		2.0			V
V_{IL}	Input low voltage				0.8	V
I_{PU}	Input pull-up current			3		µA
I_{LK}	Input leakage current		–10		10	µA
C_I	Input capacitance	Except XO / FIN, XI			10	pF
C_I	Input capacitance	Pins XO / FIN, XI		20		pF
I_{SD}[1]	Slow down supply current	SD* = Low, V_{DD} = 3.3V, No load		10		mA
I_{DD}[1]	Operating current	V_{DD} = 3.3V CPU = 40 MHz, No load CPU = 80 MHz, No load		15 18		mA

Note: 1 Indicates values when on-chip buffers are inactive

Table 7 • AC Specifications (Operating Conditions: T_A = 0°C – 70°C, V_{DD} = 3.3V ± 0.3V)

Symbol	Description	Test Condition @T_A = 25°C	Min	Typ	Max	Unit
FXTAL	Crystal frequency			14.318		MHz
FIN	Input frequency (crystal pin)		1	14.318	20	MHz
FIN	Input frequency (buffer pin)				100	MHz
TR	Output clock rise time	30 pF load, V_{OUT} = 0.8V to 2.0V			5	ns
TF	Output clock fall time	30 pF load, V_{OUT} = 0.8V to 2.0V			5	ns
TDC	Duty cycle		45	50	55	%
TJCC	Jitter, cycle to cycle	CPU = 50 MHz		150		ps
TFT	Frequency transition time	8 – 80 MHz with 0.1 µF LF capacitor		10		ms
TPU	Power up time	From OFF to 100 MHz with 0.1 µF LF capacitor		15		ms
TPLH, TPHL	Propagation delay (Bin to Bout)			5		ns
TSKEW	Buffer out skew				0.7	ns

5

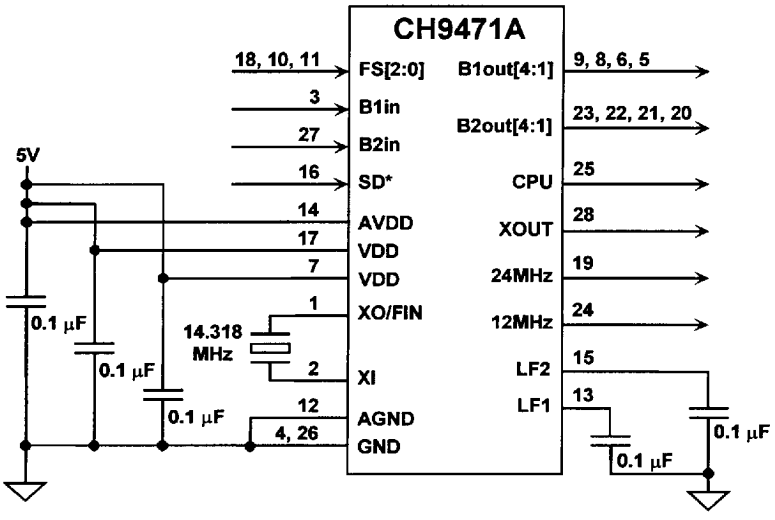

Figure 3: Application Schematic

ORDERING INFORMATION			
Part number	Package type	Number of pins	Voltage supply
CH9471A-M	209 mil SSOP	28	5V
CH9471A-M-L	209 mil SSOP	28	3.3V