ADE–207–028

HA19217MP
High-speed 8-bit A/D Converter with Analog Multiplexer

HITACHI

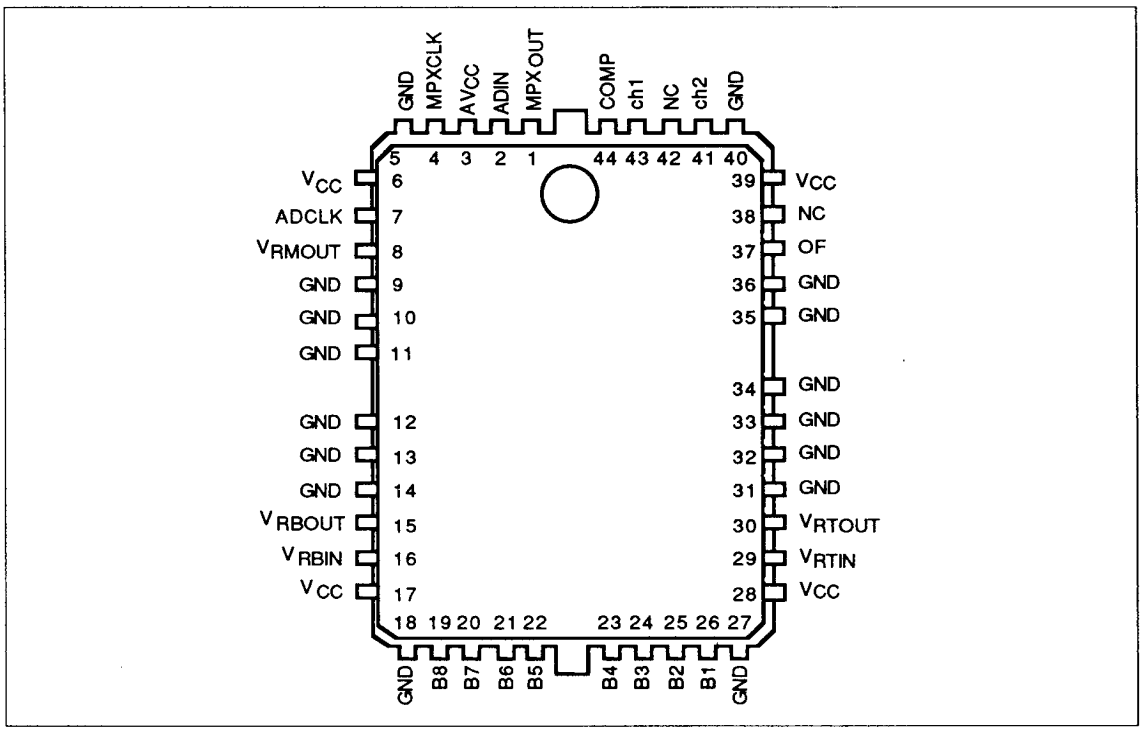
Rev. 0
June 1989
Preliminary

The HA19217 is a monolithic bipolar LSI featuring an on-chip 2-channel analog multiplexer, and is designed for applications that require an 8-bit A/D converter. A parallel type A/D converter means that no sample-and-hold circuit is required for analog input. The digital output level is LS-TTL compatible, while the block input level is TTL, CMOS compatible. The HA19217 is the perfect answer in applications that call for high-speed image processing of video signals.

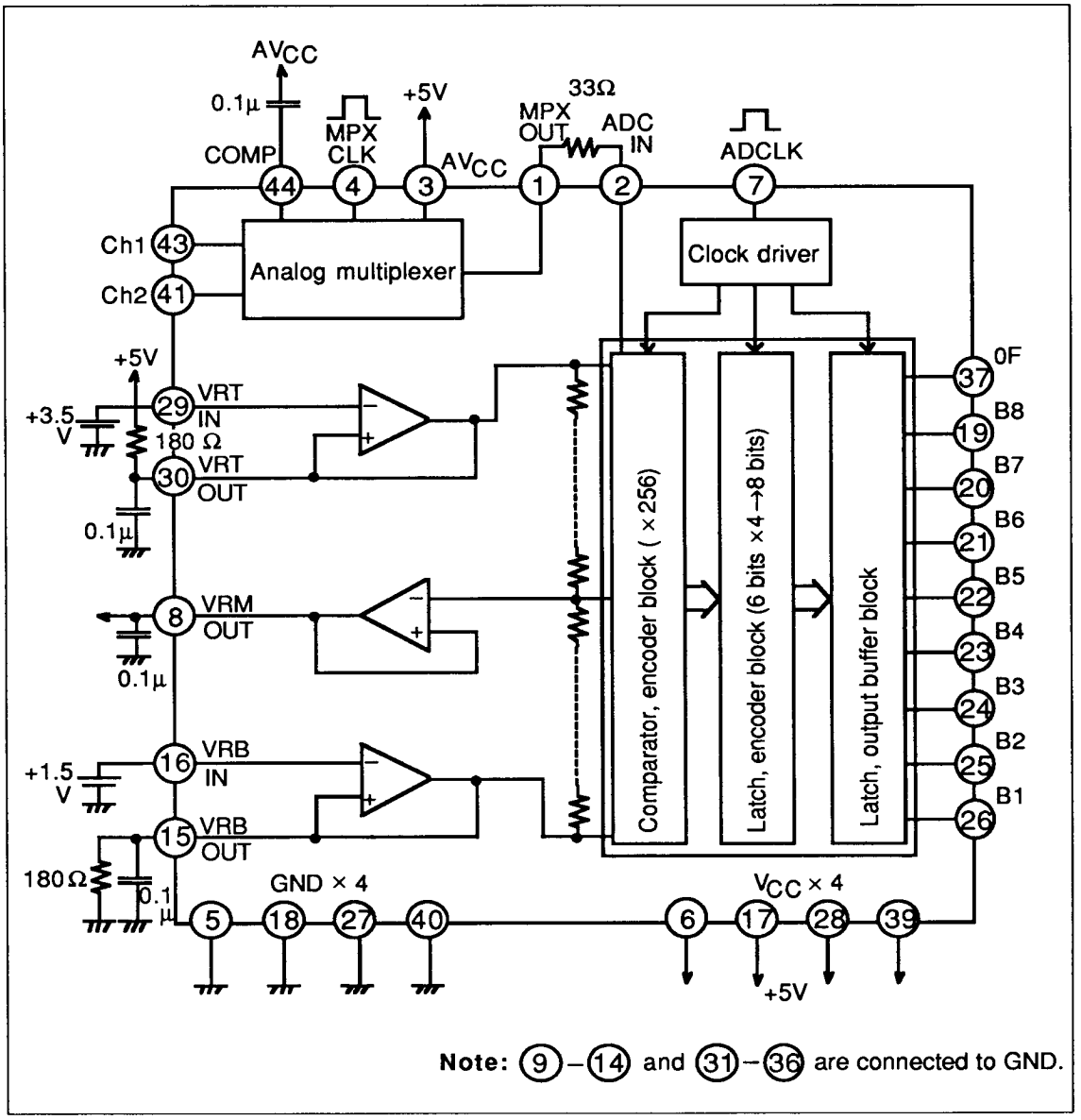
Features

- Resolution 8 bits (with overflow)
- Maximum conversion speed 40Msps (Typ)
- On-chip 2-channel analog multiplexer
- On-chip operational amplifier for reference voltage
- Operating supply voltage +5V single
- Clock input level LS-TTL, CMOS compatible
- Digital output level LS-TTL compatible

Pin Configuration



Block Diagram



Note: (9)–(14) and (31)–(36) are connected to GND.

Absolute Maximum Ratings (Ta = 25°C unless otherwise noted)

Item	Symbol	Rated Value	Unit
Supply voltage	V_{CC}	+7.0	V
Supply current	I_{CC}	TBD	mA
Power dissipation	P_T	TBD	mW
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	–55 to +125	°C

Electrical Characteristics

• ADC (Ta = 25°C, Vcc = 5.0V, V_{RTIN} = 3.5V, V_{RBIN} = 1.5V, unless otherwise noted)

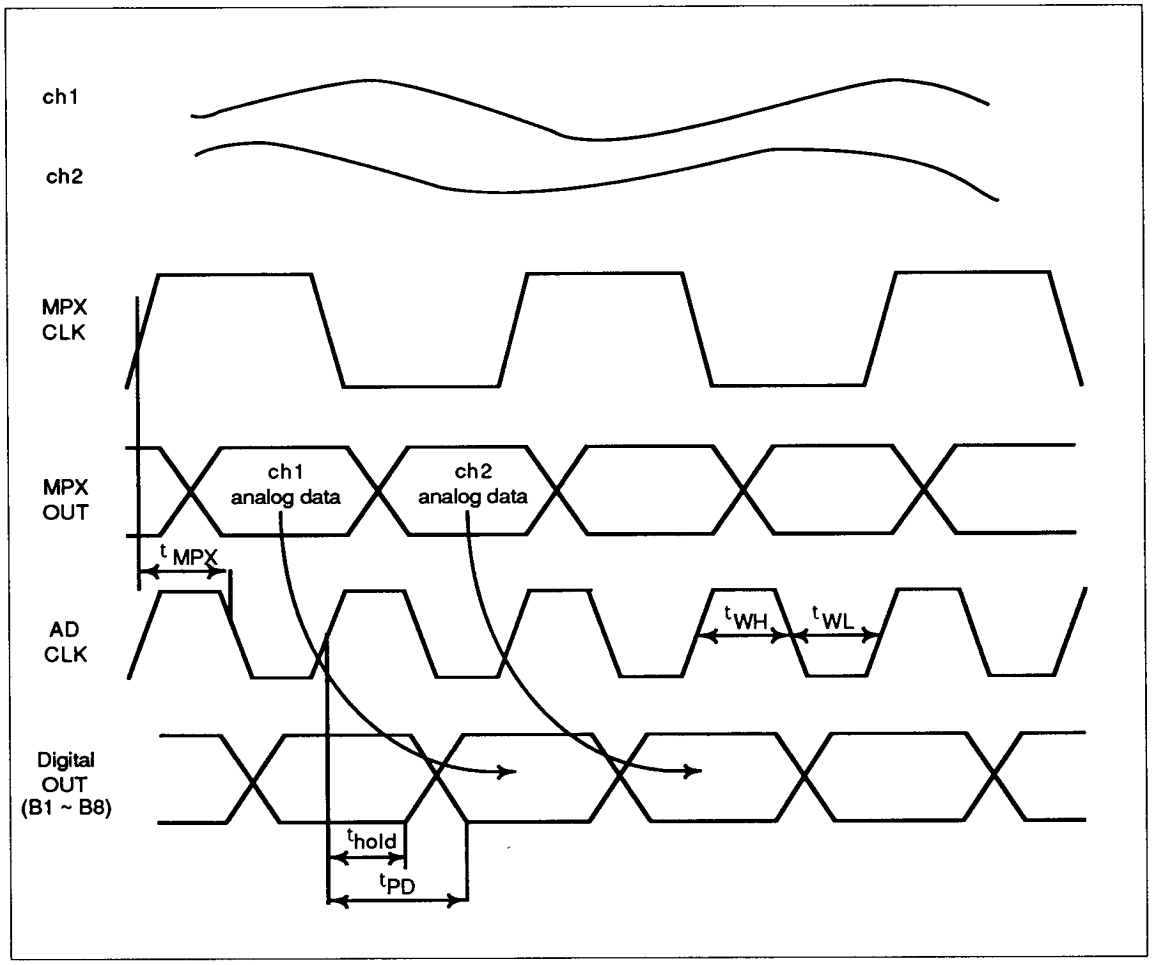
Item		Symbol	Min	Typ	Max	Unit	Test Condition
Resolution		RES	8	8	8	Bit	
Supply voltage range		V_{CC}	4.5	5.0	5.5	V	
Reference terminal input voltage range	RT	V_{RTIN}	—	3.5	—	V	
	RB	V_{RBIN}	—	1.5	—	V	
Input signal voltage range		V_{IN} (ADC)	V_{RBIN} − 0.1	—	V_{RTIN} + 0.1	V	
Input dynamic range		V_{RTIN} − V_{RBIN}	—	2.0	—	V	
Supply current		I_{CC}(ADC)	—	92	—	mA	
Reference terminal input current	RT	I_{RTIN}	−20	—	+20	μA	
	RB	I_{RBIN}	−20	—	+20	μA	
Operational amplifier	RT	ΔV_{RT} (OUT − IN)	−15	—	+15	mV	
	RB	ΔV_{RM} (OUT − IN)	−15	—	+15	mV	
Reference strings resistor		Rstr	—	180	—	Ω	
ADC analog input current		I_{IN} (ADC)	—	70	—	μA	
ADC clock input voltage	H	V_{IH} (ADC)	2.0	—	V_{CC}	V	
	L	V_{IL} (ADC)	0	—	0.8	V	
ADC clock input current	H	I_{IH} (ADC)	—	—	0.4	mA	V_{IH} = 2.7V
	L	I_{IL} (ADC)	−0.4	—	—	mA	V_{IL} = 0.4V
Digital output voltage	H	V_{OH}	2.7	—	—	V	I_{OH} = −400μA
	L	V_{OL}	—	—	0.5	V	I_{OL} = 4mA
Midpoint reference voltage level		V_{RM}	−15	—	+15	mV	Offset from V_{RTOUT} + V_{RBOUT}
Midpoint reference voltage variation		ΔV_{RM}	−5	—	+5	mV	Output current = ±50μA

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Static nonlinearity	Differential	DNL	—	±0.5	—	LSB	
	Integral	INL	—	±0.5	—	LSB	
Maximum conversion speed		f_{CLK}	30	40	—	Msps	
ADC clock pulse width	H	t_{WH}	15	—	—	ns	
	L	t_{WL}	15	—	—	ns	
Digital output delay time		t_{PD}	—	—	20	ns	
Digital output hold time		t_{HOLD}	5	—	—	ns	

• Multiplexer
(Ta = 25°C, AVcc = Vcc = 5.0V, V_{RTIN} = 3.5V, V_{RBIN} = 1.5V, 33Ω between MPX_{OUT} and ADC_{IN}, unless otherwise noted)

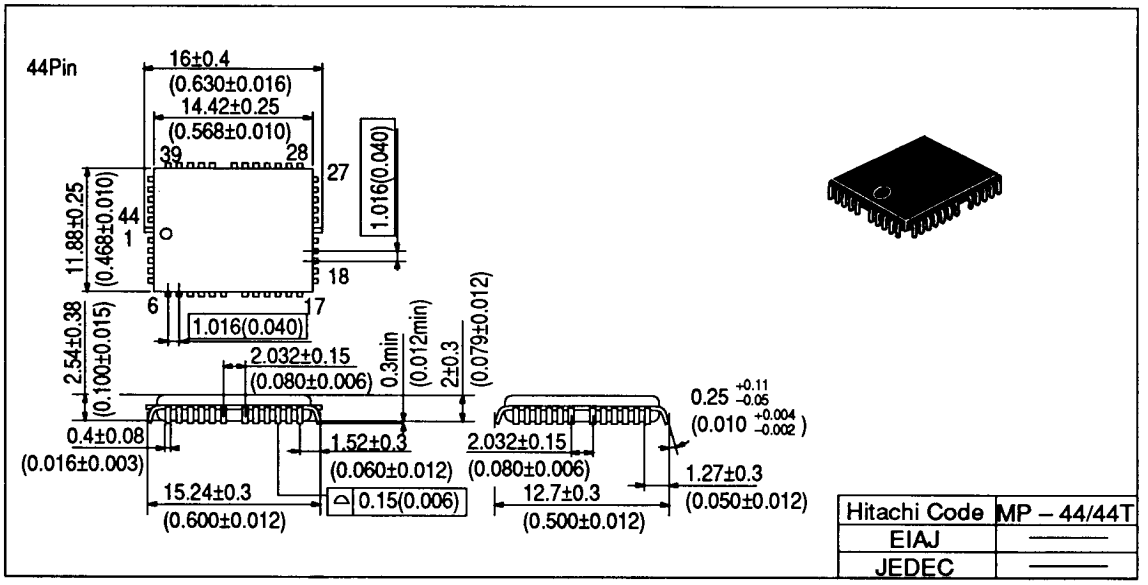
Item		Symbol	Min	Typ	Max	Unit	Test Condition
Supply voltage range		V_{CC}	4.5	5.0	5.5	V	
Input signal voltage range		V_{IN} (MPX)	1.5	—	3.5	V	
Supply current		I_{CC} (MPX)	—	28	—	mA	
MPX analog input current		I_{IN} (MPX)	—	—	100	μA	
Channel-to-channel offset		V_{ofs} (MPX)	−15	—	+15	mV	Ch1 = Ch2 = 1.5 to 3.5V
MPX output voltage	H	V_{OUT} (1.5V)	—	3.5	—	V	Ch1 or Ch2 = 1.5V
	L	V_{OUT} (3.5V)	—	1.5	—	V	Ch1 or Ch2 = 3.5V
DC gain		Gain	—	0	—	dB	
MPX clock input voltage	H	V_{IH} (MPX)	2.0	—	V_{CC}	V	
	L	V_{IL} (MPX)	0	—	0.8	V	
MPX clock input current	H	I_{IH} (MPX)	—	—	0.4	mA	V_{IH} = 2.7V
	L	I_{IL} (MPX)	−0.4	—	—	mA	V_{IL} = 0.4V
Frequency response		f_{res}	−1.0	—	+1.0	dB	V_{in} = $2V_{p-p}$ f_{in} =10MHz (excluding DC gain)
Switching time		t_{MPX}	—	—	25	ns	

Timing Chart



Pachage Outline

Unit: mm (inch)



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HITACHI

Hitachi, Ltd.
New Marunouchi Bldg., 5-1, Marunouchi 1 chome, Chiyoda-ku, Tokyo 100, Japan
Tel: Tokyo (03) 212-1111
Telex: J22395, J22432, J24491, J26375 (HITACHY)
Cable: HITACHY TOKYO

For further information write to:

Hitachi America, Ltd.
Semiconductor & IC Div.
2000 Sierra Point Parkway
Brisbane, CA. 94005-1819,
U S A
Tel: 415-589-8300
Fax: 415-583-4207

Hitachi Europe GmbH
Electronic Components Div.
Central Europe Headquarters
Hans-Pinsel-Straße 10A,
8013 Haar bei München,
West Germany
Tel: 089-46140
Fax: 089-463068

Hitachi Europe Ltd.
Electronic Components Div.
Northern Europe Headquarters
21 Upton Road,
Watford, Herts WD1 7TB,
United Kingdom
Tel: 0923-246488
Fax: 0923-224422

Hitachi Asia (Hong Kong) Ltd.
Unit 512-513, North Tower,
World Finance Centre,
Harbour City, Canton Road,
Tsimshatsui, Kowloon,
Hong Kong
Tel: 852-3-7359218
Fax: 852-3-7306071

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