HT1370
Camera Date/Time LCD Driver

Features

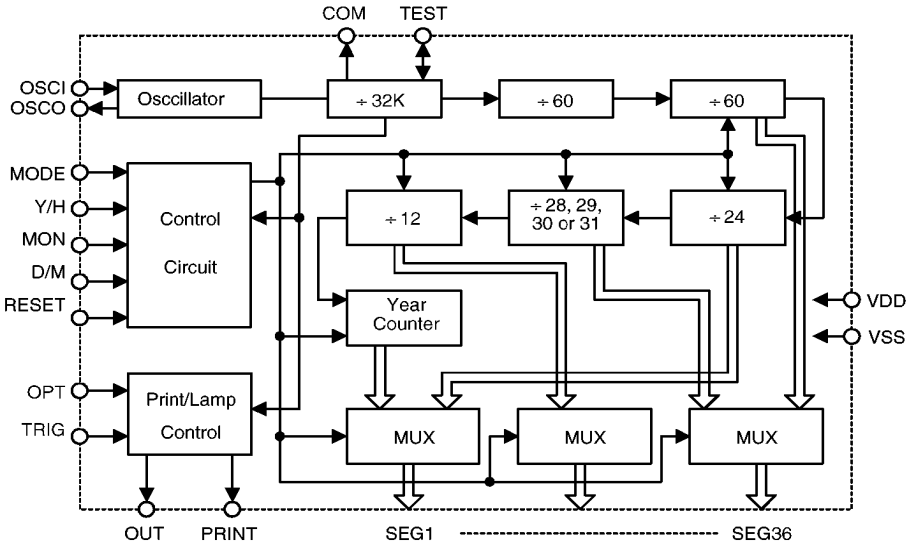
- Operating voltage: 2.4V~3.6V
- Low power consumption: <5μA at 3V
- Dual LCD driving (Single common)
- A calendar dated from 1990.10.01 to 2029.12.31
- Three-mode automatic real time display
- Lamp driver output
- A PRINT indicator

General Description

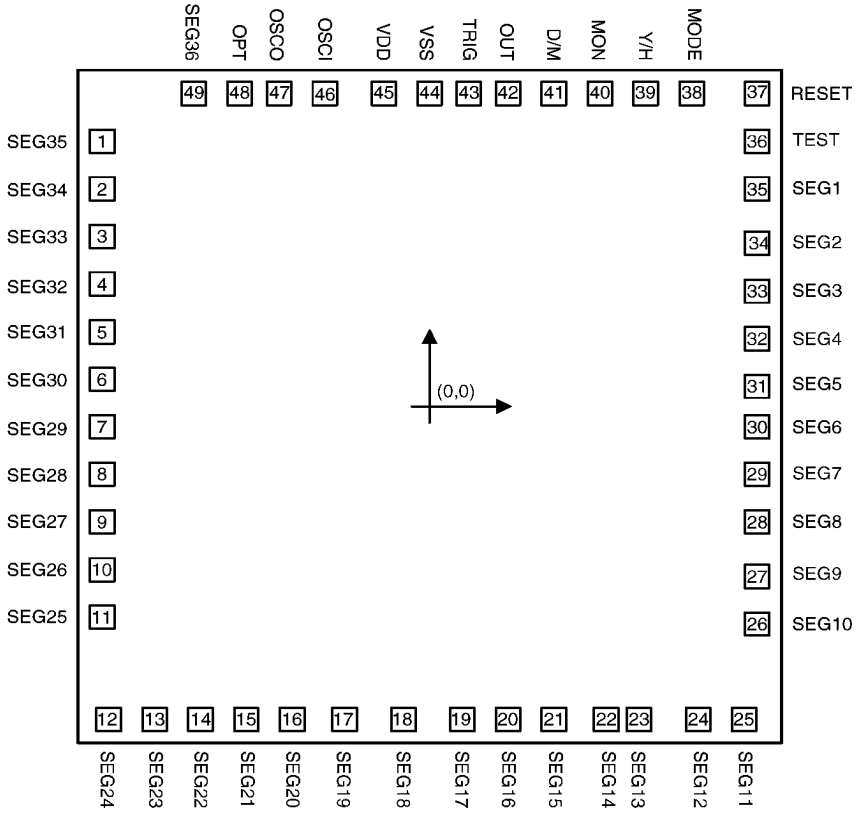
The HT1370 is a CMOS LSI chip designed for use in camera date/time stamp products. It's capable of driving 2 LCDs simultaneously. Of the 2 driven LCDs, one LCD is displayed in the normal mode for date/time recognition, while the other is displayed in the reverse mode for film exposure. The LSI contains internal circuitry which is synchronized to the camera shutter trigger for driving an incandescent lamp required for date/time film exposure.

Its "print" function provides the user with a visual LCD indication of date/time film exposure. The real-time/date function includes 3 display modes and can be powered by 2 button cells for low power applications. The LSI is offered in a dice form with a wafer thickness of about 12 mil.

Block Diagram



Pad Coordinates



Chip size: 114×105 (mil)^2

* The IC substrate should be connected to VDD in the PCB layout artwork.

Unit: mil

Pad No.	X	Y	Pad No.	X	Y
1	–50.85	39.78	26	50.68	–32.17
2	–50.85	32.64	27	50.85	–25.03
3	–50.85	25.50	28	50.68	–17.89
4	–50.85	18.36	29	50.85	–10.75
5	–50.85	11.22	30	50.85	–3.61
6	–50.85	4.08	31	50.68	3.53
7	–50.85	–3.06	32	50.68	10.67
8	–50.85	–10.20	33	50.68	17.81
9	–50.85	–17.34	34	50.68	24.95
10	–50.85	–24.48	35	50.68	32.09

Pad No.	X	Y	Pad No.	X	Y
11	–50.85	–31.62	36	50.85	39.82
12	–49.66	–46.92	37	50.85	46.45
13	–42.52	–46.92	38	40.23	46.92
14	–35.38	–46.92	39	33.17	46.92
15	–28.24	–46.92	40	26.54	46.92
16	–21.1	–46.92	41	19.57	46.92
17	–13.96	–46.92	42	12.94	46.92
18	–4.27	–46.92	43	6.31	46.92
19	5.67	–46.92	44	–0.66	46.92
20	12.81	–46.92	45	–7.71	46.92
21	19.95	–46.92	46	–16.47	46.92
22	27.09	–46.92	47	–23.18	46.92
23	32.23	–46.92	48	–29.98	46.92
24	41.37	–46.92	49	–36.61	46.92
25	48.73	–46.92			

Pad Description

Pad No.	Pad Name	I/O	Internal Connection	Description
1	SEG35	O	CMOS	LCD segment (6f) drive output
2	SEG34	O	CMOS	LCD segment (6g) drive output
3	SEG33	O	CMOS	LCD segment (5b) drive output
4	SEG32	O	CMOS	LCD segment (5a & 5d) drive output
5	SEG31	O	CMOS	LCD segment (5f) drive output
6	SEG30	O	CMOS	LCD segment (5g) drive output
7	SEG29	O	CMOS	LCD segment (PRINT)* drive output
8	SEG28	O	CMOS	LCD segment (4b) drive output
9	SEG27	O	CMOS	LCD segment (4a) drive output
10	SEG26	O	CMOS	LCD segment (4f) drive output
11	SEG25	O	CMOS	LCD segment (4g) drive output
12	SEG24	O	CMOS	LCD segment (2b) drive output
13	SEG23	O	CMOS	LCD segment (2a) drive output
14	SEG22	O	CMOS	LCD segment (2f) drive output
15	SEG21	O	CMOS	LCD segment (2g) drive output
16	SEG20	O	CMOS	LCD segment (1b) drive output

Pad No.	Pad Name	I/O	Internal Connection	Description
17	SEG19	O	CMOS	LCD segment (1f) drive output
18	SEG18	O	CMOS	LCD common drive output
19	SEG17	O	CMOS	LCD segment (1g) drive output
20	SEG16	O	CMOS	LCD segment (1e) drive output
21	SEG15	O	CMOS	LCD segment (1a & 1d) drive output
22	SEG14	O	CMOS	LCD segment (1c) drive output
23	SEG13	O	CMOS	LCD segment (2e) drive output
24	SEG12	O	CMOS	LCD segment (2d) drive output
25	SEG11	O	CMOS	LCD segment (2c) drive output
26	SEG10	O	CMOS	LCD segment (3b & 3c) drive output
27	SEG9	O	CMOS	LCD segment (4e) drive output
28	SEG8	O	CMOS	LCD segment (4d) drive output
29	SEG7	O	CMOS	LCD segment (4c) drive output
30	SEG6	O	CMOS	LCD segment (5e) drive output
31	SEG5	O	CMOS	LCD segment (5c) drive output
32	SEG4	O	CMOS	LCD segment (6e) drive output
33	SEG3	O	CMOS	LCD segment (6d) drive output
34	SEG2	O	CMOS	LCD segment (6c) drive output
35	SEG1	O	CMOS	LCD segment (6b) drive output
36	TEST	I/O	CMOS Bi-directional	For IC test only
37	RESET	I	Pull-Low	All the LCD segments are turned on for examining purposes by triggering the RESET pin. Once this pin is released, the display will be reset to 90. 10. 1. High active
38	MODE	I	Pull-Low	Triggering the MODE pin displays Date → Time → ——- cyclically. When the LCD displays —-, the "OUT" output turns out to be disabled. High active
39	Y/H	I	Pull-Low	When date is on the display, triggering the Y/H pin adjusts the year digits (1990~2029). The first two year digits (19 or 20) are omitted. When real time is on the display, triggering the Y/H pin adjusts the hour digit (0~23). It's high active. If the input high duration is greater than 2 seconds, the adjustment rate will be 8Hz.

Pad No.	Pad Name	I/O	Internal Connection	Description
40	MON	I	Pull-Low	When date is on the display, triggering the MON pin adjusts the month digits (1~12). It's high active. If the input high duration is greater than 2 seconds, the adjustment will be at an 8Hz rate.
41	D/M	I	Pull-Low	When date is on the display, triggering the D/M pin adjusts the day digits (0~31). When real time is on the display, triggering the D/M pin adjusts the minute digits (0~59). It's high active. If the input high duration is greater than 2 seconds, the adjustment rate will be 8Hz.
42	OUT	O	CMOS	Lamp drive output, normally low, active high The output high duration depends upon the OPT status. The output should be connected to an NPN transistor to drive the lamp
43	TRIG	I	Pull-Low	Trigger input for lamp flash, high active The flash duration depends upon the OPT status. For a valid trigger, the input high duration should be greater than 1ms.
44	VSS	—	—	Negative power supply
45	VDD	—	—	Positive power supply
46	OSCI	I	CMOS	System oscillator input (32768Hz crystal)
47	OSCO	O	CMOS	System oscillator output
48	OPT	I	Pull-Low	Lamp flash duration option Floating: 100ms duration VDD: 33ms duration
49	SEG36	O	CMOS	LCD segment (6a) driving output

* If the date/time is exposed on to the film, the LCD segments will be active 2~3 seconds giving the user an indication.

Absolute Maximum Ratings*

Supply Voltage ..... –0.3V to 5V
Storage Temperature ..... –50°C to 125°C
Input Voltage ..... V_{SS}–0.3V to V_{DD}+0.3V
Operating Temperature ..... 0°C to 70°C

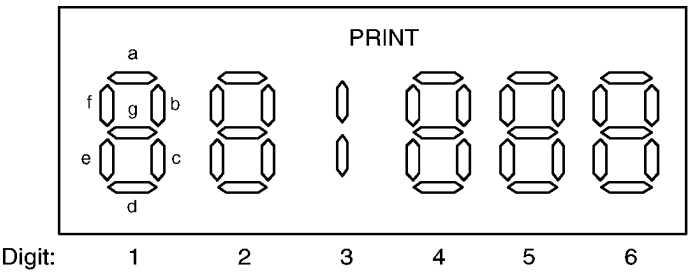
*Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extened periods may affect device reliability.

Electrical Characteristics

(Ta=25°C)

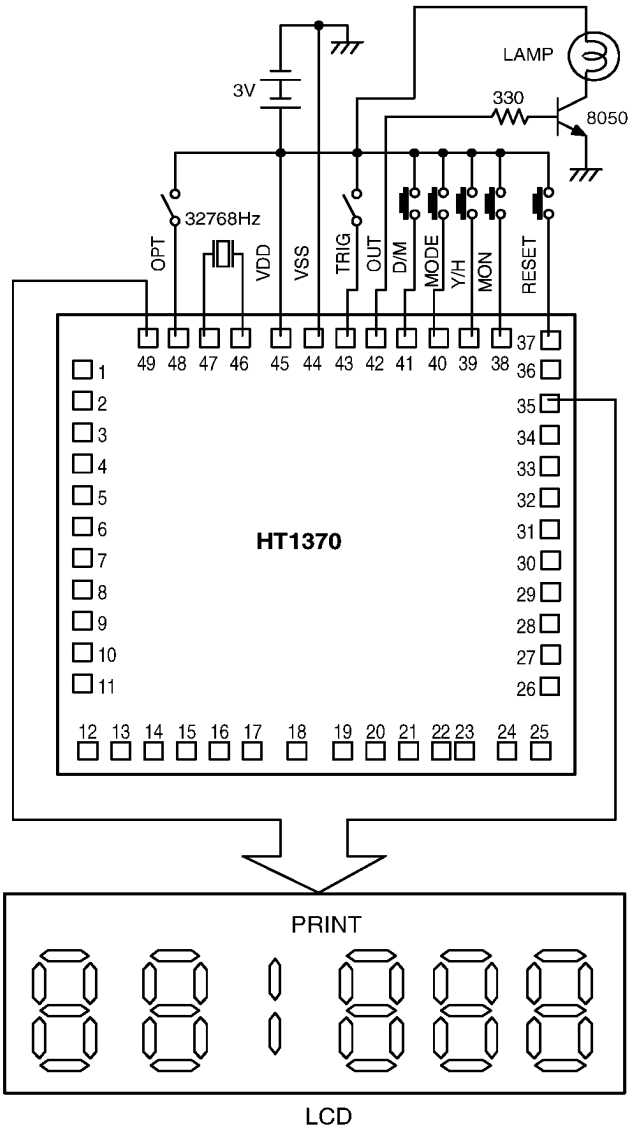
Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating Voltage	—	—	2.4	3	3.6	V
I_{DD}	Operating Current	3V	No load	—	2.5	5	μA
V_{IH}	"H" Input Voltage	—	—	$0.8V_{DD}$	—	—	V
V_{IL}	"L" Input Voltage	3V	—	—	—	$0.2V_{DD}$	V
fosc	Oscillator Frequency	3V	—	—	32768	—	Hz
I_{IH1}	Input Current (TRIG,OPT, MODE,Y/H,MON,D/M)	3V	V_{IH}=3V	7.5	15	30	μA
I_{IH2}	Input Current (RESET)	3V	V_{OL}=0.3V	13.5	27	54	μA
I_{OL1}	Output Sink Current (SEG1~SEG36)	3V	V_{OL}=0.3V	25	80	—	μA
I_{OL2}	Output Sink Current (COM)	3V	V_{OL}=0.3V	0.5	2	—	mA
I_{OL3}	Output Sink Current (OUT)	3V	V_{OL}=0.3V	100	200	—	μA
I_{OH1}	Output Source Current (SEG1~SEG36)	3V	V_{OH}=2.7V	–2.5	–80	—	μA
I_{OH2}	Output Source Current (COM)	3V	V_{OH}=2.7V	–0.25	–1	—	mA
I_{OH3}	Output Source Current (OUT)	3V	V_{OH}=2.7V	–50	–120	—	μA

LCD Pattern



Segment	LCD	segment	LCD
SEG1	6b	SEG19	1f
SEG2	6c	SEG20	1b
SEG3	6d	SEG21	2g
SEG4	6e	SEG22	2f
SEG5	5c	SEG23	2a
SEG6	5e	SEG24	2b
SEG7	4c	SEG25	4g
SEG8	4d	SEG26	4f
SEG9	4e	SEG27	4a
SEG10	3bc	SEG28	4b
SEG11	2c	SEG29	PRINT
SEG12	2d	SEG30	5g
SEG13	2e	SEG31	5f
SEG14	1c	SEG32	5ad
SEG15	1ad	SEG33	5b
SEG16	1e	SEG34	6g
SEG17	1g	SEG35	6f
COM	COM	SEG36	6a

Application Circuit



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