ANALOG DEVICES

Dual/Quad Low Power, High Speed JFET Operational Amplifier

OP-282/OP-482

2

FEATURES

High Slew Rate: 9 V/μs
Wide Bandwidth: 4 MHz
Low Supply Current: 250 μA/Amplifier
Low Offset Voltage: 3 mV
Low Bias Current: 100 pA
Fast Settling Time
Common-Mode Range Includes V+
Unity Gain Stable

APPLICATIONS

Active Filters
Fast Amplifiers
Integrators
Supply Current Monitoring

GENERAL DESCRIPTION

The OP-282/OP-482 dual and quad operational amplifiers feature excellent speed at exceptionally low supply currents. Slew rate exceeds 7 V/μs with supply current under 250 μA per amplifier. These unity gain stable amplifiers have a typical gain-bandwidth of 4 MHz.

The JFET input stage of the OP-282/OP-482 insures bias current is typically a few picoamps and below 500 pA over the full temperature range. Offset voltage is under 3 mV for the dual and under 4 mV for the quad.

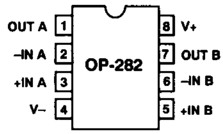
With a wide output swing, within 1.5 volts of each supply, low power consumption and high slew rate, the OP-282/OP-482 are ideal for battery-powered systems or power restricted applications. An input common-mode range that includes the positive supply makes the OP-282/OP-482 an excellent choice for high-side signal conditioning.

The OP-282/OP-482 are specified over the extended industrial temperature range. Both dual and quad amplifiers are available in plastic and ceramic DIP plus SOIC surface mount packages.

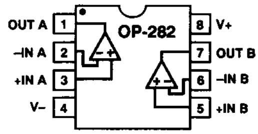
Contact your local sales office for MIL-STD-883 data sheet and availability.

PIN CONNECTIONS

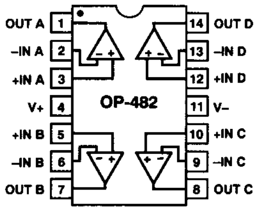
8-Lead Narrow-Body SOIC
(S Suffix)



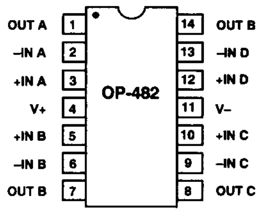
8-Lead Epoxy DIP
(P Suffix)



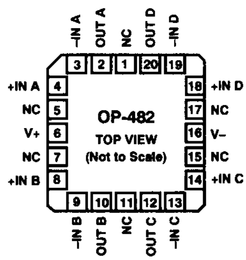
14-Lead Epoxy DIP
(P Suffix)



14-Lead Narrow-Body SOIC
(S Suffix)



20-Position Chip Carrier
(RC Suffix)



NC = NO CONNECT

OP-282/OP-482—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±15.0 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	OP-282		0.2	3	mV
		OP-282, $-40 \le T_A \le +85°C$			4.5	mV
Offset Voltage	V_{OS}	OP-482		0.2	4	mV
		OP-482, $-40 \le T_A \le +85°C$			6	mV
Input Bias Current	I_B	V_{CM} = 0 V		3	100	pA
		V_{CM} = 0 V, Note 1			500	pA
Input Offset Current	I_{OS}	V_{CM} = 0 V		1	50	pA
		V_{CM} = 0 V, Note 1			250	pA
Input Voltage Range			−11		+15	V
Common-Mode Rejection	CMR	$-11V \le V_{CM} \le +15$ V, $-40 \le T_A \le +85°C$	70	90		dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ	20			V/mV
		R_L = 10 kΩ, $-40 \le T_A \le +85°C$	15			V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			10		μV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			8		pA/°C
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V_O	R_L = 10 kΩ	−13.5	±13.9	13.5	V
Short Circuit Limit	I_{SC}	Source	3	10		mA
		Sink	−8	−12		mA
Open-Loop Output Impedance	Z_{OUT}	f = 1 MHz		200		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±4.5 V to ±18 V, $-40 \le T_A \le +85°C$		25	316	μV/V
Supply Current/Amplifier	I_{SY}	V_O = 0 V, $40 \le T_A \le +85°C$		210	250	μA
Supply Voltage Range	V_S		±4.5		±18	V
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ	7	9		V/μs
Full-Power Bandwidth	BW_P	1% Distortion		125		kHz
Settling Time	t_S	To 0.01%		1.6		μs
Gain Bandwidth Product	GBP			4		MHz
Phase Margin	$\varnothing o$			55		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		1.3		μVp-p
Voltage Noise Density	e_n	f = 1 kHz		36		$nV/\sqrt{Hz}$
Current Noise Density	i_n			0.01		$pA/\sqrt{Hz}$

NOTE
[1]The input bias and offset currents are tested at $T_A = T_J = +85°C$. Bias and offset currents are guaranteed but not tested at −40°C.
Specifications subject to change without notice.

WAFER TEST LIMITS (@ V_S = ±15.0 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Limit	Units
Offset Voltage	V_{OS}	OP-282	3	mV max
Offset Voltage	V_{OS}	OP-482	4	mV max
Input Bias Current	I_B	V_{CM} = 0 V	100	pA max
Input Offset Current	I_{OS}	V_{CM} = 0 V	50	pA max
Input Voltage Range[1]			−11, +15	V min/max
Common-Mode Rejection	CMRR	$-11V \le V_{CM} \le +15$ V	70	dB min
Power Supply Rejection Ratio	PSRR	V = ±4.5 V to ±18 V	316	μV/V
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ	20	V/mV min
Output Voltage Range	V_O	R_L = 10 kΩ	±13.5	V min
Supply Current/Amplifier	I_{SY}	V_O = 0 V, $R_L = \infty$	250	μA max

NOTES
Electrical tests and wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.
[1]Guaranteed by CMR test.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply voltage . . . . ±18 V
Input Voltage[2] . . . . ±18 V
Differential Input Voltage[2] . . . . 36 V
Output Short-Circuit Duration . . . . Indefinite
Storage Temperature Range
  Y, Z, RC Package . . . . −65°C to +175°C
  P, S Package . . . . −65°C to +150°C
Operating Temperature Range
  OP-282A, OP-482A . . . . −55°C to +125°C
  OP-282G, OP-482G . . . . −40°C to +85°C
Junction Temperature Range
  Y, Z, RC Package . . . . −65°C to +125°C
  P, S Package . . . . −65°C to +125°C
Lead Temperature Range (Soldering, 60 Sec) . . . . +300°C

Package Type	θ_{JA}[3]	θ_{JC}	Units
8-Pin Cerdip (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SOIC (S)	158	43	°C/W
14-Pin Cerdip (Y)	108	16	°C/W
14-Pin Plastic DIP (P)	83	39	°C/W
14-Pin SOIC (S)	120	36	°C/W
20-Contact LCC (RC)	98	38	°C/W

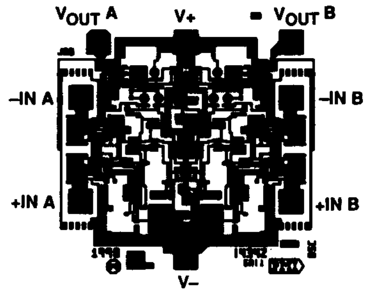
NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.
[3]θ_{JA} is specified for the worst case conditions, i.e., θ_{JA} is specified for device in socket for cerdip, P-DIP, and LCC packages; θ_{JA} is specified for device soldered in circuit board for SOIC package.

ORDERING GUIDE

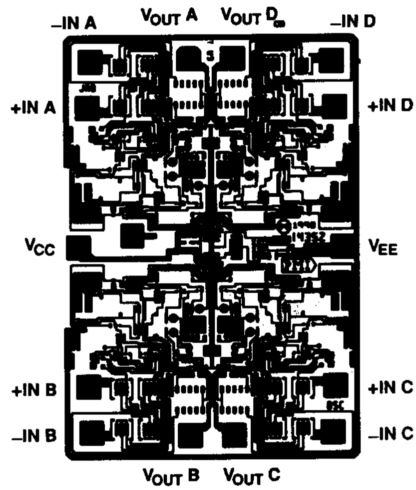
Model	Temperature Range	Package Option*
OP282AZ/883	−55°C to +125°C	14-Pin Cerdip
OP482AY/883	−55°C to +125°C	14-Pin Cerdip
OP482ARC/883	−55°C to +125°C	20-Contact LCC
OP282GP	−40°C to +85°C	8-Pin Plastic DIP
OP282GS	−40°C to +85°C	8-Pin SOIC
OP482GP	−40°C to +85°C	14-Pin Plastic DIP
OP482GS	−40°C to +85°C	14-Pin SOIC
OP282GBC	+25°C	DICE
OP482GBC	+25°C	DICE

*For outline information see Package Information section.

DICE CHARACTERISTICS



OP-282 Die Size 0.063 × 0.060 Inch, 3,780 Sq. Mils



OP-482 Die Size 0.070 × 0.098 Inch, 6,860 Sq. Mils

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APPLICATIONS INFORMATION

The OP-282 and OP-482 are single and dual JFET op amps that have been optimized for high speed at low power. This combination makes these amplifiers excellent choices for battery powered or low power applications requiring above average performance. Applications benefiting from this performance combination include telecom, geophysical exploration, portable medical equipment and navigational instrumentation.

HIGH SIDE SIGNAL CONDITIONING

There are many applications that require the sensing of signals near the positive rail. OP-282s and OP-482s have been tested and guaranteed over a common-mode range ($-11\ V \leq V_{CM} \leq +15\ V$) that includes the positive supply.

One application where this is commonly used is in the sensing of power supply currents. This enables it to be used in current sensing applications such as the partial circuit shown in Figure 1. In this circuit, the voltage drop across a low value resistor, such as the 0.1 Ω shown here, is amplified and compared to 7.5 volts. The output can then be used for current limiting.

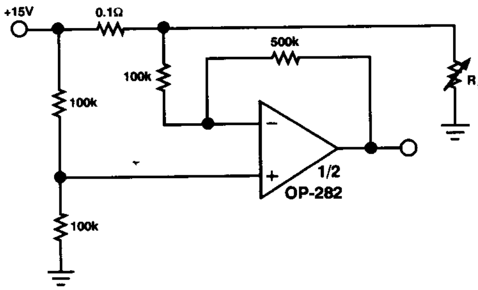

Figure 1. Phase Inversion

PHASE INVERSION

Most JFET-input amplifiers will invert the phase of the input signal if either input exceeds the input common-mode range. For the OP-282 and OP-482 negative signals in excess of approximately 14 volts will cause phase inversion. The cause of this effect is saturation of the input stage leading to the forward-biasing of a drain-gate diode. A simple fix for this in non-inverting applications is to place a resistor in series with the noninverting input. This limits the amount of current through the forward-biased diode and prevents the shutting down of the output stage. For the OP-282/OP-482, a value of 200 kΩ has been found to work. However, this adds a significant amount of noise.

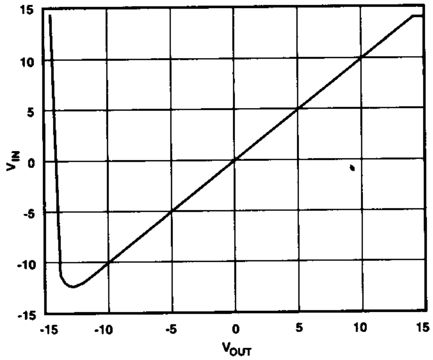

Figure 2. OP-282 Phase Reversal

ACTIVE FILTERS

The OP-282 and OP-482's wide bandwidth and high slew rates make either an excellent choice for many filter applications.

There are many types of active filter configurations, but the four most popular configurations are Butterworth, elliptical, Bessel, and Chebyshev. Each type has a response that is optimized for a given characteristic as shown in Table I.

Table I.

Type	Selectivity	Overshoot	Phase	Amplitude (Pass Band)	Amplitude (Stop Band)
Butterworth	Moderate	Good		Max Flat	
Chebyshev	Good	Moderate	Nonlinear	Equal Ripple	
Elliptical	Best	Poor		Equal Ripple	Equal Ripple
Bessel (Thompson)	Poor	Best	Linear		

PROGRAMMABLE STATE–VARIABLE FILTER

The circuit shown in Figure 3 can be used to accurately program the "Q," the cutoff frequency f_C, and the gain of a two-pole state-variable filter. OP-482s have been used in this design because of their high bandwidths, low power and low noise. This circuit takes only three packages to build because of the quad configuration of the op amps and DACs.

The DACs shown are all used in the voltage mode so all values are dependent only on the accuracy of the DAC and not on the absolute values of the DAC's resistive ladders. This make this circuit unusually accurate for a programmable filter.

Adjusting DAC 1 changes the signal amplitude across R1; therefore, the DAC attenuation times R1 determines the amount of signal current that charges the integrating capacitor, C1. This cutoff frequency can now be expressed as:

$$f_C = \frac{1}{2\pi R_1 C_1}\left(\frac{D_1}{256}\right)$$

where D_1 is the digital code for the DAC.

Gain of this circuit is set by adjusting D3. The gain equation is:

$$Gain = \frac{R_4}{R_5}\left(\frac{D_3}{256}\right)$$

DAC 2 is used to set the "Q" of the circuit. Adjusting this DAC controls the amount of feedback from the bandpass node to the input summing node. Note that the digital value of the DAC is in the numerator, therefore zero code is not a valid operating point.

$$Q = \frac{R_2}{R_3}\left(\frac{256}{D_2}\right)$$

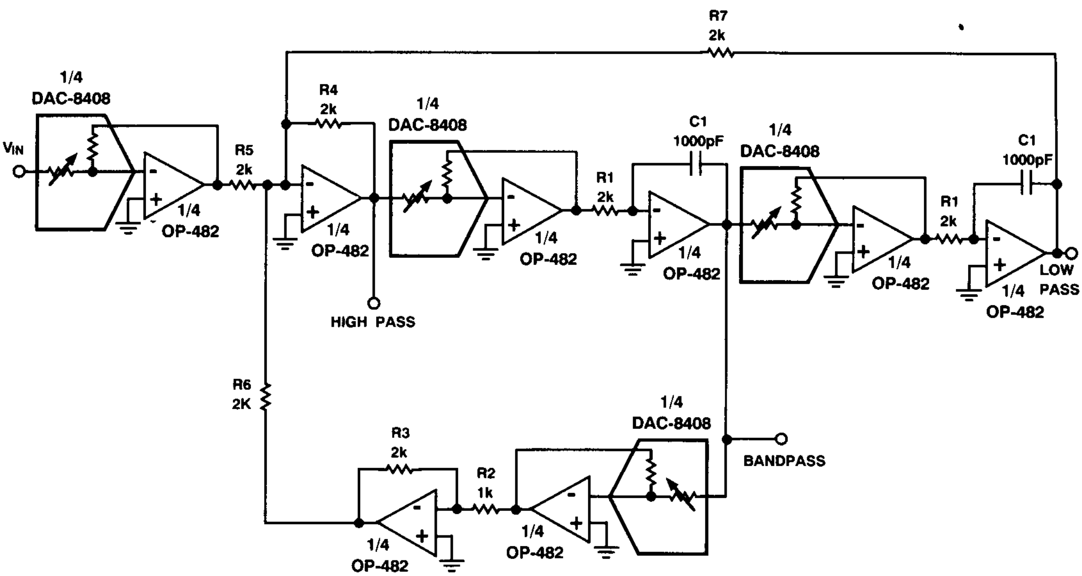

Figure 3.

OP-282/OP-482 SPICE MACRO MODEL

Figure 4 shows the OP-282 SPICE macro model. The model for the OP-482 is similar to that of the OP-282, but there are some minor changes in the circuit values. Contact ADI for a copy of the latest SPICE model diskette for both listings.

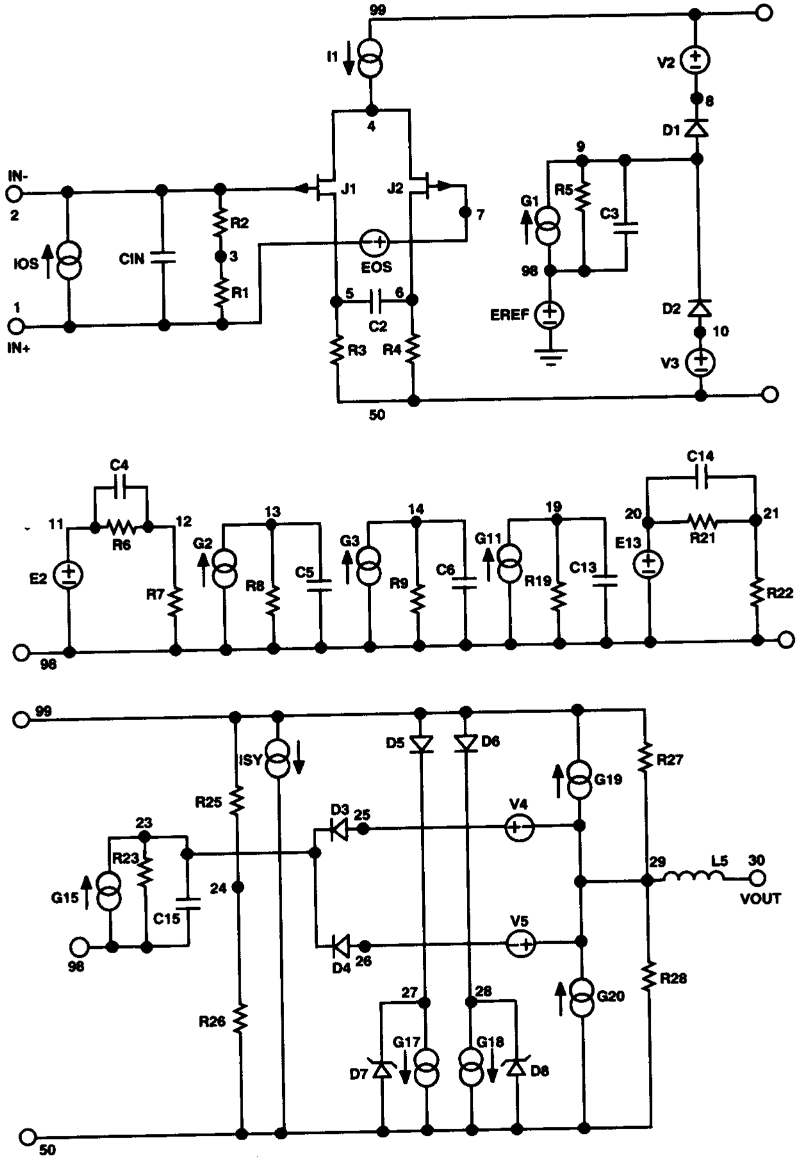

Figure 4.

OP-282 SPICE MACRO MODEL

```
* Node assignments
*                    noninverting input
*                    |  inverting input
*                    |  |  positive supply
*                    |  |  |  negative supply
*                    |  |  |  |  output
*                    |  |  |  |  |
.SUBCKT OP282        1  2  99 50 30
*
* INPUT STAGE & POLE AT 15 MHZ
*
R1     1   3   5E11
R2     2   3   5E11
R3     5   50  3871.3
R4     6   50  3871.3
CIN    1   2   5E-12
C2     5   6   1.37E-12
I1     99  4   0.1E-3
IOS    1   2   5E-13
EOS    7   1   POLY(1) 21 24 200E-6 1
J1     5   2   4        JX
J2     6   7   4        JX
*
EREF   98  0   24       0 1
*
* GAIN STAGE & POLE AT 124 HZ
*
R5     9   98  1.16E8
C3     9   98  1.11E-11
G1     98  9   5 6      2.58E-4
V2     99  8   1.2
V3     10  50  1.2
D1     9   8   DX
D2     10  9   DX
*
* NEGATIVE ZERO AT 4 MHZ
*
R6     11  12  1E6
R7     12  98  1
C4     11  12  39.8E-15
E2     11  98  9        24 1E6
*
* POLE AT 15 MHZ
*
R8     13  98  1E6
C5     13  98  10.6E-15
G2     98  13  12       24 1E-6
*
* POLE AT 15 MHZ
*
R9     14  98  1E6
C6     14  98  10.6E-15
G3     98  14  13       24 1E-6
*
* POLE AT 15 MHZ
*
R19    19  98  1E6
C13    19  98  10.6E-15
G11    98  19  14       24 1E-6
*
* COMMON-MODE GAIN NETWORK
WITH ZERO AT 11 KHZ
*
R21    20  21  1E6
R22    21  98  1
C14    20  21  14.38E-12
E13    98  20  3        24 31.62
*
* POLE AT 15 MHZ
*
R23    23  98  1E6
C15    23  98  10.6E-15
G15    98  23  19       24 1E-6
*
* OUTPUT STAGE
*
R25    24  99  5E6
R26    24  50  5E6
ISY    99  50  107E-6
R27    29  99  700
R28    29  50  700
L5     29  30  1E-8
G17    27  50  23       29 1.43E-3
G18    28  50  29       23 1.43E-3
G19    29  99  99       23 1.43E-3
G20    50  29  23       50 1.43E-3
V4     25  29  2.8
V5     29  26  3.5
D3     23  25  DX
D4     26  23  DX
D5     99  27  DX
D6     99  28  DX
D7     50  27  DY
D8     50  28  DY
*
* MODELS USED
*
.MODEL JX PJF(BETA = 3.34E-4
VTO = -2.000 IS = 3E-12)
.MODEL DX D(IS = 1E-15)
.MODEL DY D(IS = 1E-15 BV = 50)
.ENDS OP282
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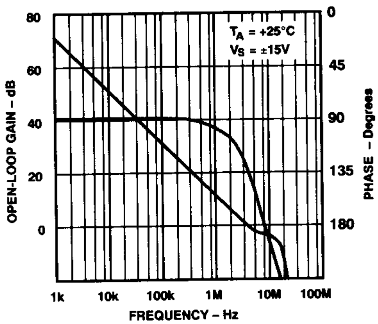

Figure 5. Open-Loop Gain, Phase vs. Frequency

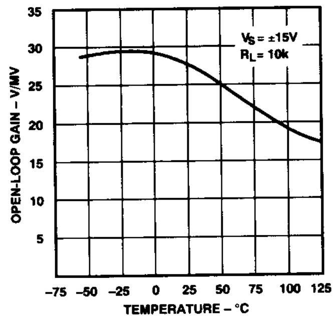

Figure 8. Open-Loop Gain (V/mV)

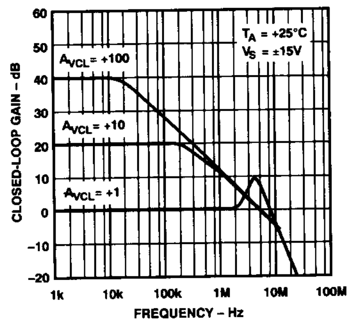

Figure 6. Closed-Loop Gain vs. Frequency

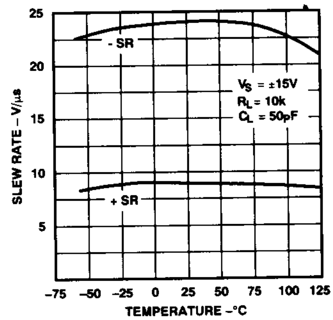

Figure 9. OP-282/OP-482 Slew Rate vs. Temperature

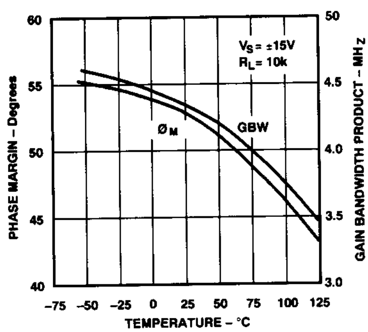

Figure 7. OP-482 Phase Margin and Gain Bandwidth Product vs. Temperature

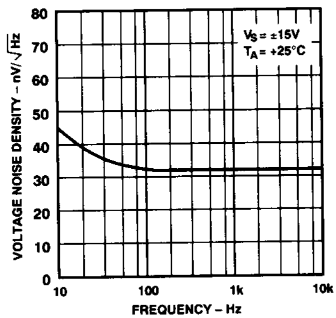

Figure 10. Voltage Noise Density vs. Frequency

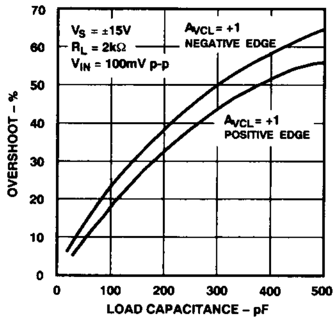

Figure 11. Small Signal Overshoot vs. Load Capacitance

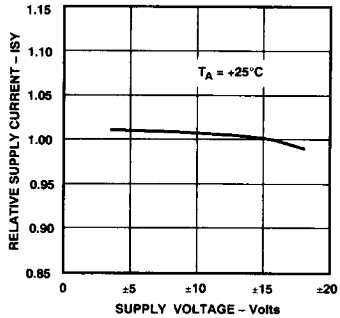

Figure 14. Relative Supply Current vs. Supply Voltage

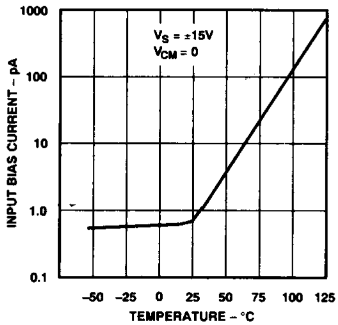

Figure 12. OP-282 Input Bias Current vs. Temperature

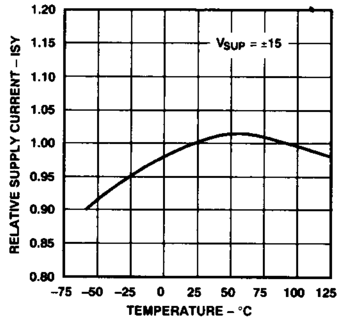

Figure 15. Relative Supply Current vs. Temperature

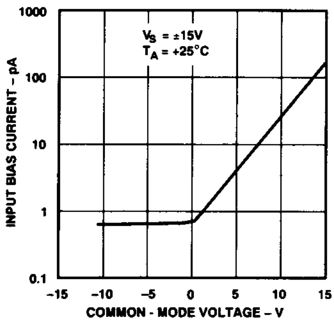

Figure 13. OP-282 Input Bias Current vs. Common-Mode Voltage

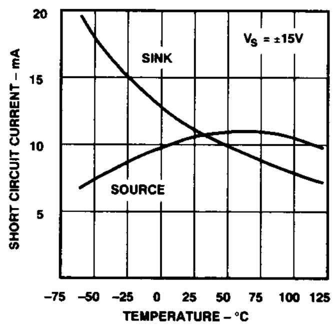

Figure 16. OP-282/OP-482 Short Circuit Current vs. Temperature

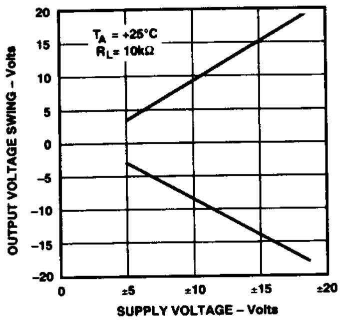

Figure 17. Output Voltage Swing vs. Supply Voltage

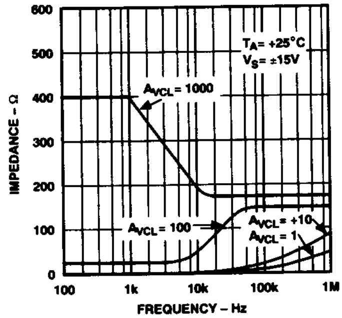

Figure 20. OP-482 Closed-Loop Output Impedance vs. Frequency

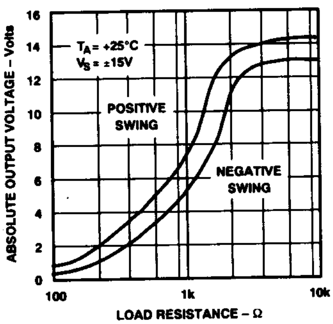

Figure 18. Maximum Output Voltage vs. Load Resistance

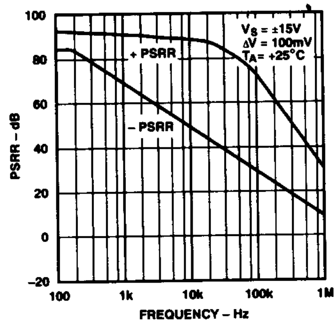

Figure 21. OP-282 Power Supply Rejection Ratio (PSRR) vs. Frequency

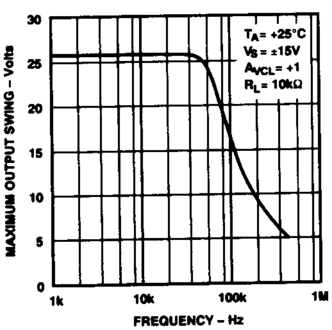

Figure 19. Maximum Output Swing vs. Frequency

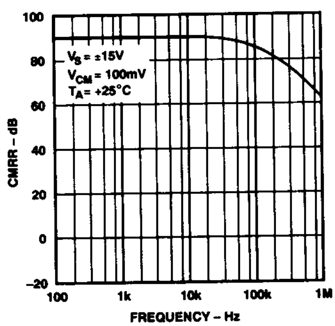

Figure 22. OP-282 Common-Mode Rejection Ratio (CMRR) vs. Frequency

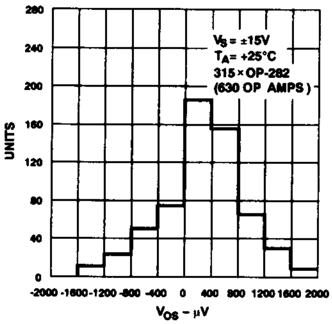

Figure 23. V_{OS} Distribution "P" Package

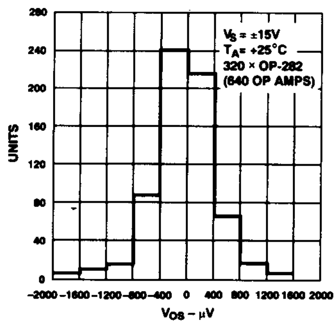

Figure 24. V_{OS} Distribution "Z" Package

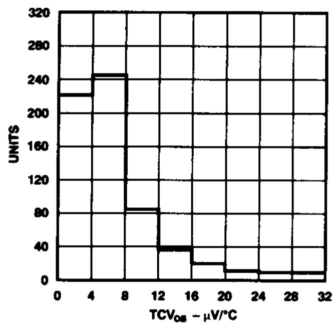

Figure 25. OP-282 TCV_{OS} (µV/°C) Distribution "P" Package

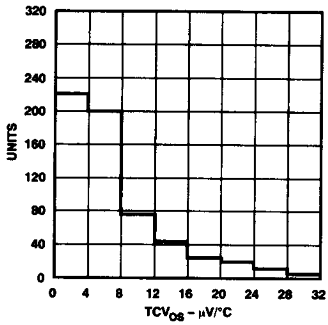

Figure 26. OP-282 TCV_{OS} (µV/°C) Distribution "Z" Package

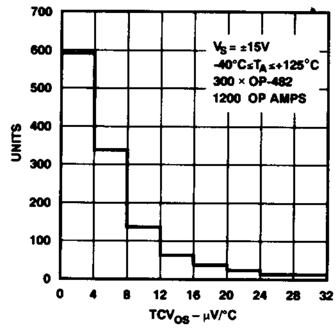

Figure 27. OP-482 TCV_{OS} Distribution "Z" Package

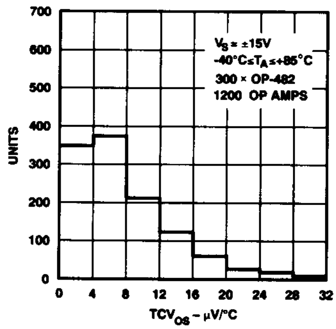

Figure 28. TCV_{OS} Distribution "P" Package

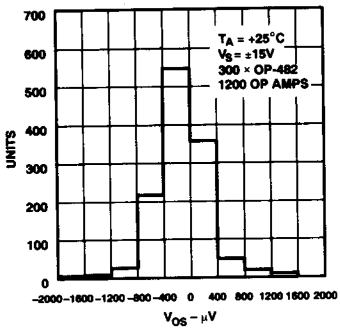

Figure 29. OP-482 V_{OS} Distribution "Z" Package

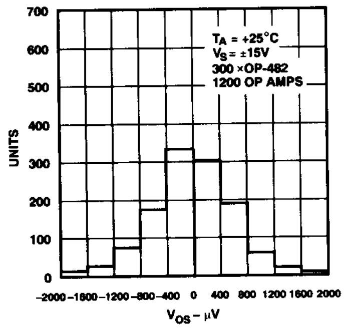

Figure 30. OP-482 V_{OS} Distribution "P" Package